Chapter 3

Development and evaluation of the TL/OSL system

3.1 Introduction

Thermoluminescence (TL) is the phenomena of emission of light due to the thermal stimulation of material which has been irradiated with ionizing radiations and if the emission of light is caused due to optical stimulation then it is known as Optically Stimulated Luminescence (OSL). Thus in order to perform TL/OSL, a system needs to be developed which is able to provide user-defined thermal/optical stimulation and which is equipped with a light detector to capture the emitted luminescence. All of these components are required to work in synchronization. Such a system with an EMCCD camera for spatially resolved luminescence studies and FPGA based control system has not been reported in the literature. The development of such a system is described in this chapter.

Basically this system comprises of a thermal and optical stimulation system, a detection system with its associated optics, sample housing, system control and data processing system. The target parameters for TL were to provide thermal stimulation at a linearly variable heating rate ranging from 0.1 ˚C/s to 10 ˚C/s up to a maximum of 500 ˚C with the ability to maintain this temperature up to an hour and measure the emitted luminescence by a suitable detector. The target parameters for OSL were to provide optical stimulation at a linearly increasing rate, known as Linearly Modulated OSL (LM-OSL), ranging from 0.1 %/s to 2 %/s up to the maximum intensity which corresponds to 20 mA current passing through the blue light emitting diodes and to provide optical stimulation at a constant intensity, known as Constant Wave OSL (CW-OSL). OSL could be done at any temperature ranging from room temperature to 500 ˚C.

3.2 System description

The block diagram of the entire system is shown in figure 1. The system consists of a TL stimulation unit, OSL stimulation unit, photon detection unit, Field Programmable Gate Array (FPGA) based control unit, and a user friendly Graphic User Interface (GUI)

developed using LabVIEW (Laboratory Virtual Instrument Engineering Workbench), from M/s National Instrumentation. Stimulation of a sample is done thermally by means of a heater plate in case of TL and optically by a source of light as LEDs in case of OSL. To measure the spatially resolved luminescence EMCCD camera has been used. In order to maintain the required thermal or optical stimulation, feedback circuitry has been used in which temperature or light intensity is measured by temperature sensor as thermocouple and light sensor as photodiode respectively. Sensor outputs are amplified, digitalised and compared with the reference signal generated by the FPGA and fed to respective drivers of the heater plate or LEDs.

The user can enter all the parameters of TL/OSL like the required heating rate, final temperature, the hold time for that temperature, the light intensity in percentage of maximum intensity and the mode of OSL in the GUI. Using RS-232 communication these parameters are transferred to the FPGA from the computer. The FPGA then simultaneously controls the TL and the OSL driving circuit accordingly. The emitted light is detected by the EMCCD and transferred to the computer for image analysis. FPGA synchronizes with the EMCCD so that the correspondence between the intensity of the image and the temperature or light intensity can be accurately recorded. The different parts of the block diagram are explained in detail in the subsequent sections.

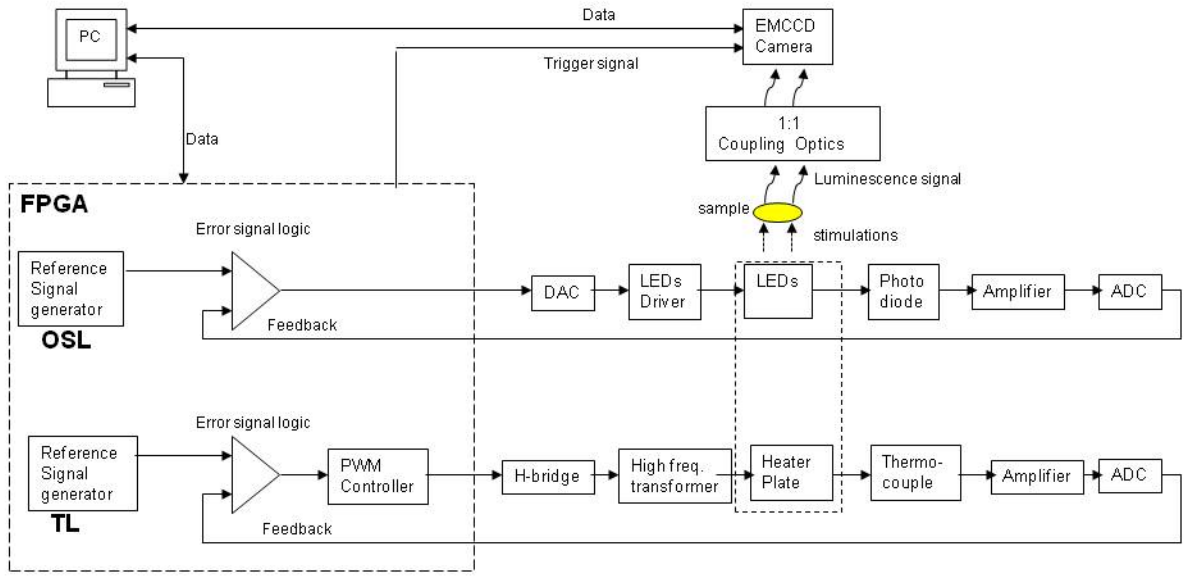

Figure 1. Block diagram of the TL/OSL system

3.3 Thermoluminescence (TL)

Thermoluminescence (TL) or Thermally Stimulated Luminescence (TSL) is observed by heating a sample at a constant rate to about 500 ˚C and recording the luminescence emitted as a function of temperature. The required thermal stimulation for TL is provided by the TL part of the system. Kanthal heating system along with the temperature sensing for feedback control is used for thermal stimulation. The FPGA produces a driving signal for the heater as per the parameters set in the GUI. This driving signal and the feedback by thermocouple control the width of the Pulse Width Modulation (PWM) signals which controls the power given to the transformer and thus its temperature. An optimised algorithm to control the width of the PWM is implemented in FPGA. This algorithm takes into account the heating rate, the sampling rate of analogue-to-digital convertor (ADC), and the error produced in order to have a tight control over the temperature profile. An un-optimised algorithm would show lagging, over-shoot, under-shoot in the temperature profile and performance variations based on the heating rate. The system provides stable temperature profile with average error in temperature being less than 0.5 °C. Figure 2 shows the performance of the heating system.

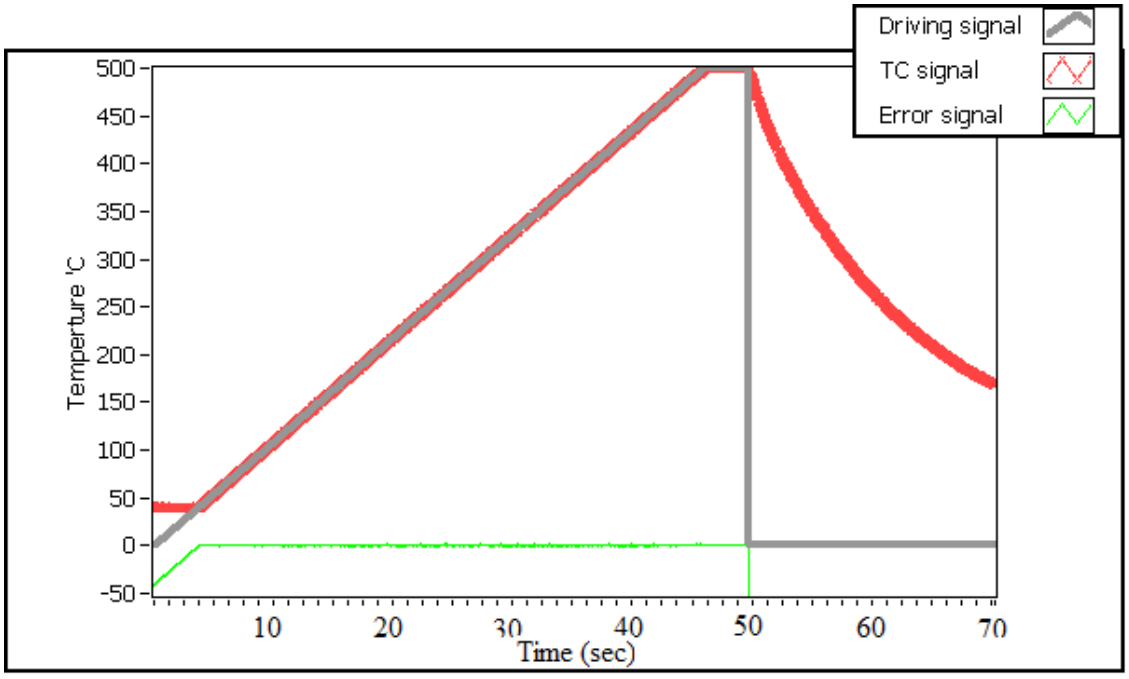

Figure 2. Driving signal, Temperature signal and Error signal graph for the heater unit

The TL heater assembly consists of a low mass heater plate, a thermocouple which is spot-welded below the heater plate, a thermocouple output amplifier circuit, a ADC circuit, a transformer, transformer driving circuit and a FPGA. These components of the TL system are described below:

3.3.1 Heater Plate

High resistivity ‘Kanthal’ heating plate is used as it is superior to ‘Nicrothal’ [1]. It is the trademark of Sandvik, Sweden which owns its intellectual property rights. Kanthal is an alloy of iron, chromium, and aluminium. It also contains Carbon, Manganese, and Silicon in a very small proportion. Nikrothal is an alloy of Nickel and Chromium along with Carbon, Manganese, and Silicon in smaller proportions. Kanthal is magnetic whereas Nikrothal is non-magnetic. The size of the ‘Kanthal’ plate is kept as small as possible. Due to a smaller heater plate area the black body radiation is minimal and it will also require lesser power. The amount of power required can be calculated using the specific heat, weight and resistance of the material which depends on its dimensions.

A thin Kanthal heater plate of 0.3 mm thickness is used as it has high resistivity and low mass. Both these characteristics are conducive for the heating process because the current required for it decreases with the increase in resistivity and with the decrease in the mass of the heater plate. More resistivity implies less current will be required to heat it. Higher amount of current will require a bulkier transformer for the heating element. It will also limit the maximum frequency of the transformer due to skin effect. Higher the frequency of the transformer, smaller will be its size. However, with the increase in the frequency the amount of current that can flow through a wire decreases. Thus an optimization has to be made between frequency and amount of current

3.3.2 Thermocouple

Thermocouple works on the principle of Seebeck effect which was discovered by Thomas Seebeck in the year 1821. According to this principle when two dissimilar metals are joined at both ends and a temperature difference is created between the two ends then a current will flow in the loop formed by these two metal wires. If the loop is broken, a voltage could be measured which depends on the difference of temperature between the two ends. This voltage

is called Seebeck Voltage. Usually 0 ˚C is taken as the reference temperature which used to be provided by an ice-bath. Since this is not a very practical method, the ice point reference is eliminated by adding a voltage which is opposite to that of the reference junction.

A thermocouple can be formed by the combination of various metals. The properties of the thermocouple like its temperature range, linearity and sensitivity depend on the metals constituting the thermocouple. These combinations have been characterized and classified by the National Institute of Standards and Technology (NIST). The various thermocouples are thermocouple B formed by Platinum and Rhodium; thermocouple E formed by Chromel and Constantan; thermocouple J formed by Iron and Constantan; thermocouple k formed by Chromel and Alumel; thermocouple N formed by Nicrosil and Nisil; and thermocouple T formed by Copper and Constantan.

A k type thermocouple is used here. K type thermocouple provides the most linear response beyond 0 ˚C and is one of the most widely used thermocouple. It is spot welded under the heater plate. The output of the thermocouple is amplified and converted into digital form and transferred to the FPGA. The temperature range of a thermocouple depends on its size. As its size increases, its range and life increases but its sensitivity decreases. Thus where sensitivity is critical, a thicker thermocouple than required should not be used. Here a thermocouple of 0.127 mm thickness is used. It has a temperature range up to 500 °C. For a temperature range up to 700 °C a thermocouple of 0.5 mm thickness would be required [2].

Some precautions need to be taken while designing a thermocouple circuit. The common-mode voltages should not exceed the range of the amplifier used to amplify the thermocouple output. Proper extension wires have to be used. If the thermocouple is thin, then the extension wires should be thick in order to decrease the resistance. The thermocouple wire should be shielded and twisted to avoid Electro-Magnetic Interference (EMI) and proper grounding should be done to avoid any ground loops.

3.3.3 Thermocouple amplifier

The output of the k type thermocouple is only 41 μV/˚C. Since this value is too small to be directly converted into digital form by the ADC, it is amplified by an amplifier AD8495 with a gain of 122.4 to produce 5 mV/˚C. AD8495 is a precision instrumentation amplifier with thermocouple cold junction compensators on the integrated circuit so that no external

compensation circuit is required. It can be used as standalone thermometers or switched output setpoint controllers using a fixed or remote setpoint control. Either a single supply ranging from 2.7 V to 36 V or a dual supply ranging from ±2.7 V to ±18 V can be used to power it. Temperatures below 0 °C can be measured by offsetting the reference input. It is laser trimmed to match the characteristics of k type thermocouples. The inputs can endure 4 kV of electrostatic discharge and provides over-voltage protection up to Vs ± 25 V. Its differential inputs reject common-mode noise on the thermocouple leads [3].

Since a high frequency PWM is used, it causes EMI problems for the thermocouple which is very susceptible to it due to the very low level voltages (41 μV/°C) associated with it. A filter circuit is used at the input of the thermocouple amplifier IC to filter out the EMI noise as shown in figure 3. In this circuit the thermocouple output are connected with the low pass filter formed by the resistors R1 and R2 and the capacitors C1, C2 and C3. R3 is recommended for the proper functioning of the circuit. The filter outputs are connected to the input of the amplifier AD8495. C4 and C5 are used to filter the power supply.

The output voltage of this amplifier is converted into a digital form using an ADC kit (Pmod AD1 from M/s Digilent, USA having AD7476A IC) and is then transferred to the FPGA. The FPGA handles the inherent non-linearity of the thermocouple using a look-up table approach.

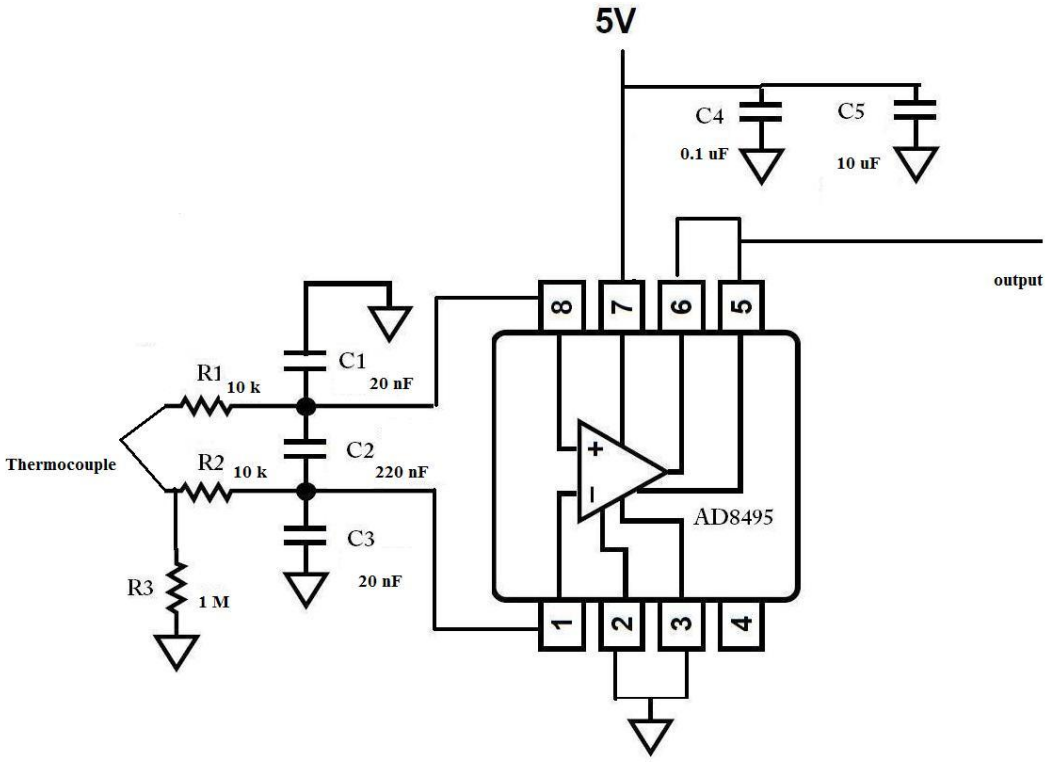

Figure 3. Thermocouple filter and amplifier circuit

3.3.4 Trigger circuit

In order to establish a proper correspondence between the temperature and the image acquired by the EMCCD, a trigger pulse at a definite temperature is given to the EMCCD camera which starts image acquisition once it is received. In the circuit shown in figure 4 the trigger output of the FPGA is given to optocoupler 4N35. This device consists of a gallium-arsenide infrared-emitting diode optically coupled to an npn silicon phototransistor. It has high-voltage electrical isolation of 3.55 kV and high speed switching with a typical rise and fall time of 7 μs [4].

The output of this optocoupler is given to MC74HCT245AN transceiver which is utilized as a buffer in this circuit. The output from MC74HCT245AN is connected to the trigger pin of EMCCD using a BNC connector.

The MC74HCT245A is a 3–state non-inverting transceiver that is used for 2–way asynchronous communication between data buses. The device has an active–low Output Enable pin, which is used to place the I/O ports into high–impedance states and is permanently grounded. The Direction control pin which is connected to Vcc, determines the data flow direction or in other words determines which pins functions as the input and which pins functions as the output. The unused input pins are permanently connected to Vcc by a series resistor of 10k and the unused output pins are left unconnected [5].

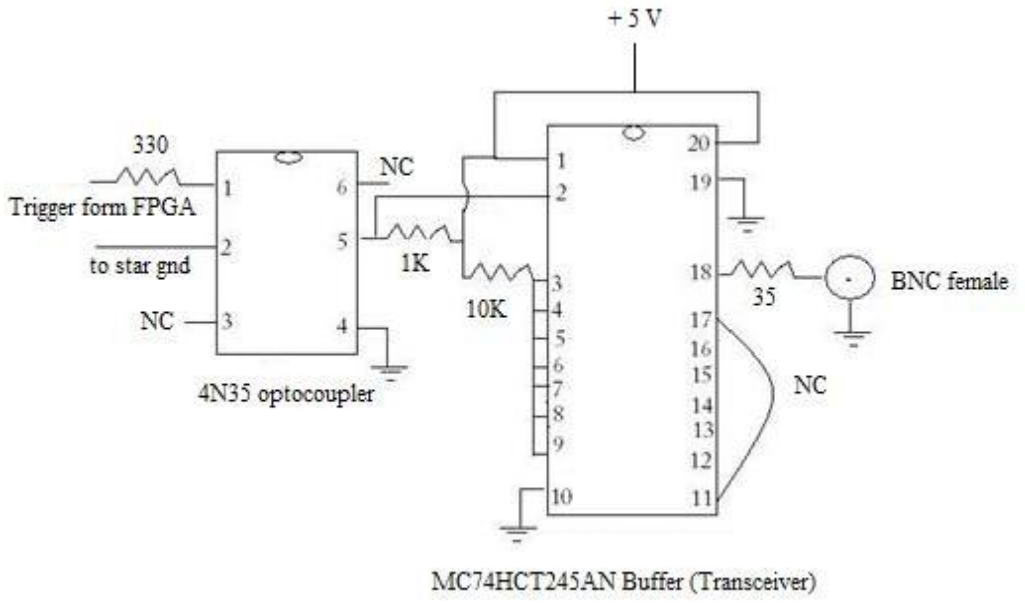

Figure 4. Trigger circuit for EMCCD

This circuit, consisting of the optocoupler and buffer, provides complete electrical isolation between the EMCCD trigger input and the other circuit. This isolation is needed to prevent any false triggering due to noise caused by the PWM or by any other noise in the system.

3.3.5 FPGA logic for TL

Coding for FPGA was done using the VHDL programming language. In order to generate the driving signal a ramp-counter is synthesised in the FPGA whose output is taken as the driving signal. The final count of this ramp-counter corresponds to the final temperature of the heater

set by the user in the GUI. The rate at which the driving signal increases is determined by the frequency of the clock of the ramp counter. This clock is generated by another counter: the rate-counter. When the rate-counter rolls over, a flip-flop toggles which is used as the clock for the ramp-counter. The frequency of this clock depends on the final count of the rate-counter which is decided by the 'rate' entered by the user in the GUI. Once the ramp-counter reaches its final value, it holds this final value till the hold-time is over. The hold-time counter keeps incrementing with the clock pulses, till it reaches the hold-time value, where it resets the ramp-counter.

Two PWM signals are generated by the FPGA: one for each input of the H-bridge. An H bridge is an electronic circuit that enables a voltage to be applied across a load in either direction. The amount of time that each of the PWM signals remains high, i.e. its duty cycle, is determined by the value of a variable in the FPGA. The value of this variable depends upon the error signal. Thus the error signal controls the duty cycle of the PWM which in turn controls the temperature profile. This error signal which is produced in the FPGA is a function of the ramp rate, sampling frequency and the driving signal. In order to generate the error signal a comparison is done between the driving and feedback signal on the clock of the rate counter and on the clock of the sampling frequency. The gain in the error signal by the comparison done on the rate counter is more than the gain in the error signal by the comparison done on the sampling frequency. A non-optimised gain at this stage would cause either over-shoot or lagging in the temperature with respect to the driving signal at different temperatures.

3.4 Optically stimulated luminescence

Optically Stimulated Luminescence (OSL) arises from the recombination of charge which has been optically released from electron traps within the crystal. The population of the traps is the result of irradiation of the material, and thus OSL intensity is related to absorbed radiation dose. The optical stimulation of the sample is provided by a set of LEDs whose light output is controlled. A feedback servo system is used to stabilise the current through the LEDs. A photodiode measures the light intensity, which is then compared with the reference signal generated by FPGA. The reference signal is produced as per the parameters set in the GUI. The controlling signal produced by the FPGA is in a digital form. This is given to a

digital-to-analogue convertor (DAC) whose analogue output is used to control the output of the LED driver circuit as shown in figure 5. Since the intensity of the LEDs is dependent on the amount of current through them, the op-amp driver circuit is required to regulate the intensity by regulating the amount of current passing through the LEDs. Feedback is needed for light intensity control because the relation between current passing through the LEDs and its intensity is not linear. Feedback corrects this inherent non-linearity.

3.4.1 Optical stimulation unit for OSL

The light stimulation unit consist of blue light emitting diodes (NSPB-500S). The spectral emission characteristics of these diodes have peak intensity at ~470 nm with FWHM of ~15 nm. The field-of-view is kept at ~15^{o} with suitable mechanical arrangement. Its maximum specification for forward current and power dissipation are 30 mA and 120 mW respectively. The intensity of the diodes can be varied from 0-100% of the total power corresponding to a maximum of 20 mA current through each diode, and can be ramped at variable rates linearly. A cluster of 30 LEDs are arranged on a circular ring structure. The LEDs are located at such an angle that they together provide a uniform intensity at the centre location where the sample is placed on the heater position as shown in figure 6. The circular ring structure in which the LEDs are housed is of aluminium make, which also acts as a heat sink and maintains the LEDs at room temperature ensuring that their emission wavelength does not change. The LEDs gets heated up as some of the applied voltage is converted into heat. This causes a decrease in light intensity [6-7]. This is prevented by the use of the heat absorbing aluminium make LED holder.

The circuit of the stimulation unit is given in figure 5. Its working is as follows: a total of thirty LEDs are used for the stimulation. However one of these LEDs is dedicated to provide feedback. Its light is focused on photodiode S1133-14. Since the output of the photodiode is in current form it is amplified by a current-to-voltage circuit using the op-amp OP27. The output of this amplifier is converted into digital form by the ADC and given to the FPGA. In the FPGA, this feedback signal is compared with the internally generated driving signal. An error signal is generated by it using appropriate error signal generation logic. This error signal is converted into analogue form by a DAC and given as the input to the op-amp current driving circuit which controls the amount of current passing thorough the LEDs and thus controls its intensity. There are five such driver circuits, each connected with five LEDs.

Figure 7 shows the setup of the system. In the insert pictures are shown the EMCCD camera, optical ray diagram and the LEDs in the aluminium holder.

The system provides stable optical profile with average error in light intensity being less than 0.1%. Figure 8 shows the performance of the optical stimulating system.

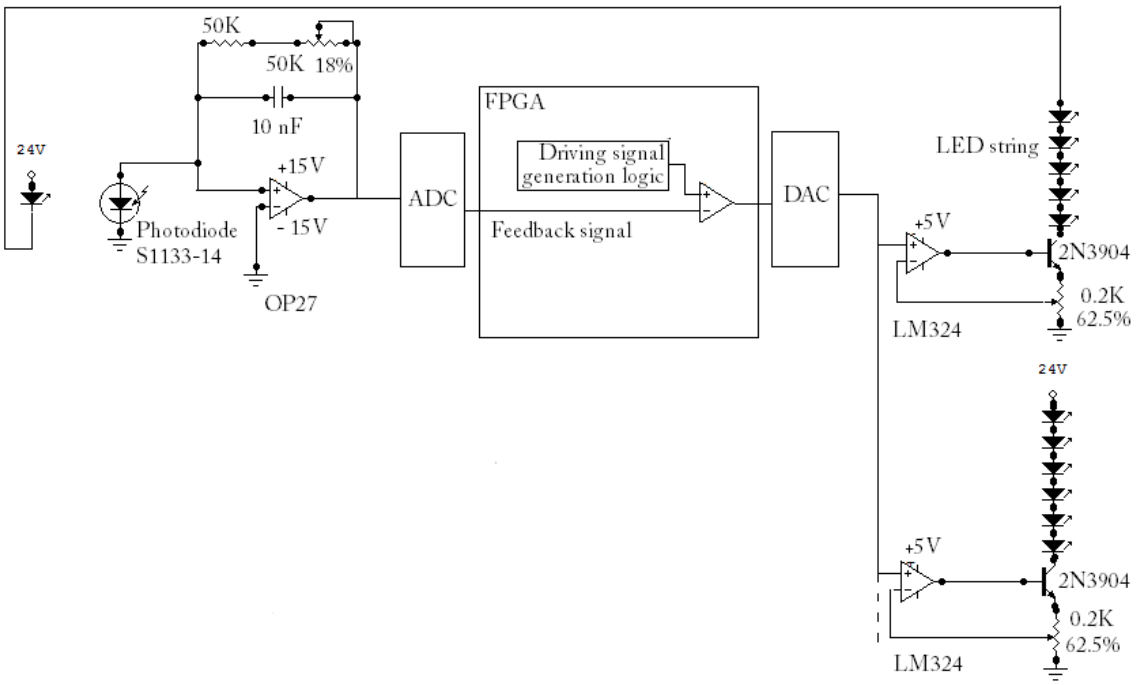

Figure 5. OSL feedback and LED driver circuit

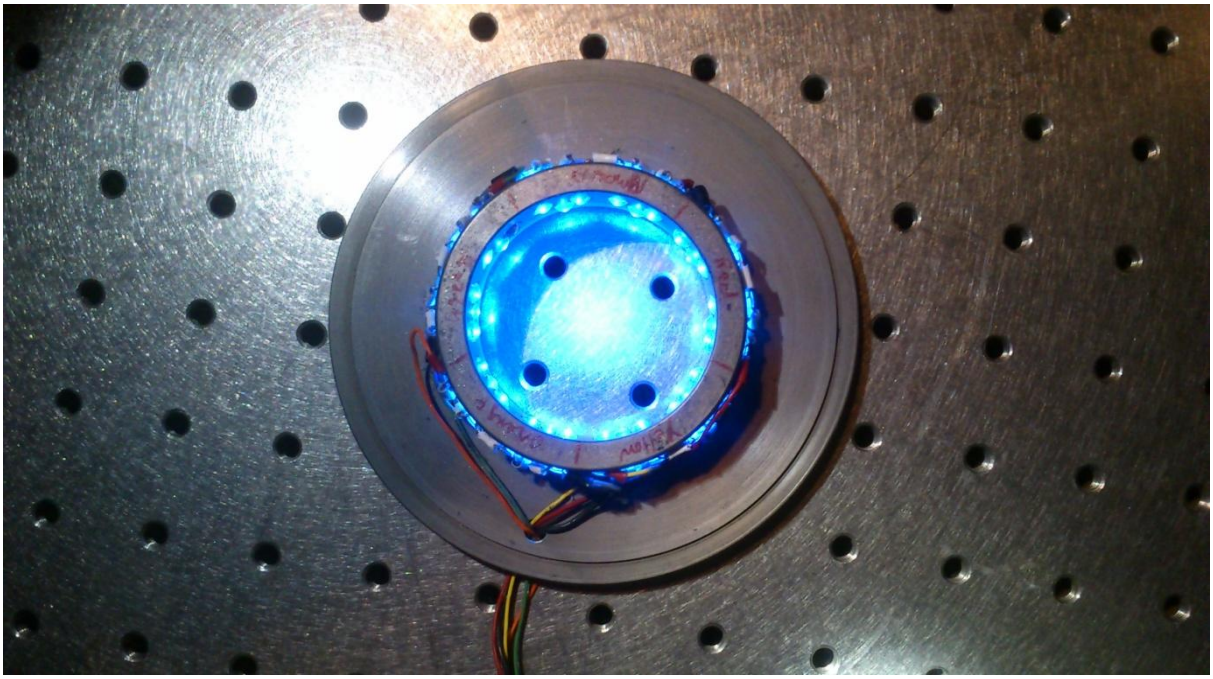

Figure 6. Aluminium LED Holder focussing the light on the centre.

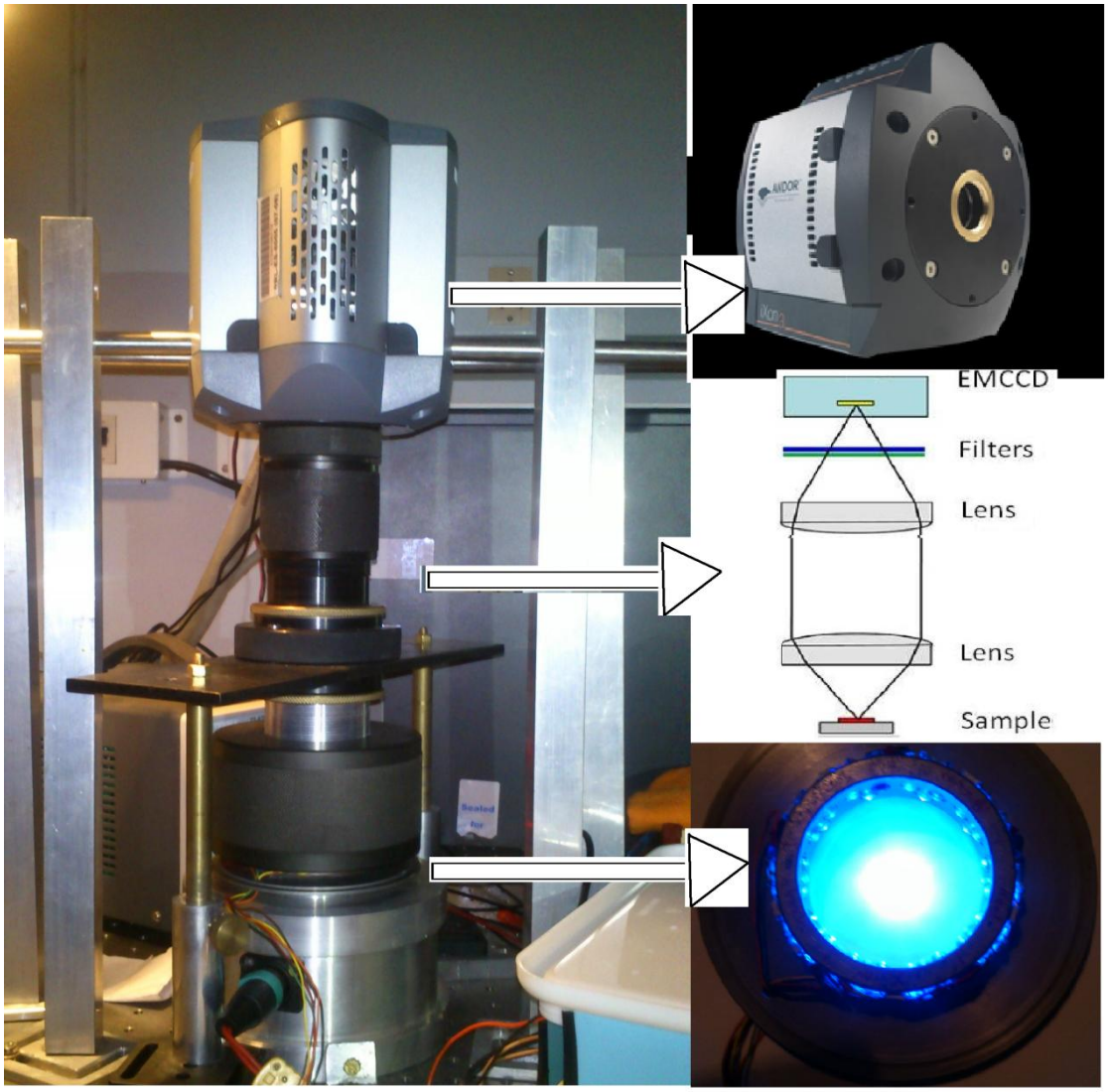

Figure 7. Set-up of the system; insert showing the aluminum ring for OSL, optical arrangement and EMCCD camera

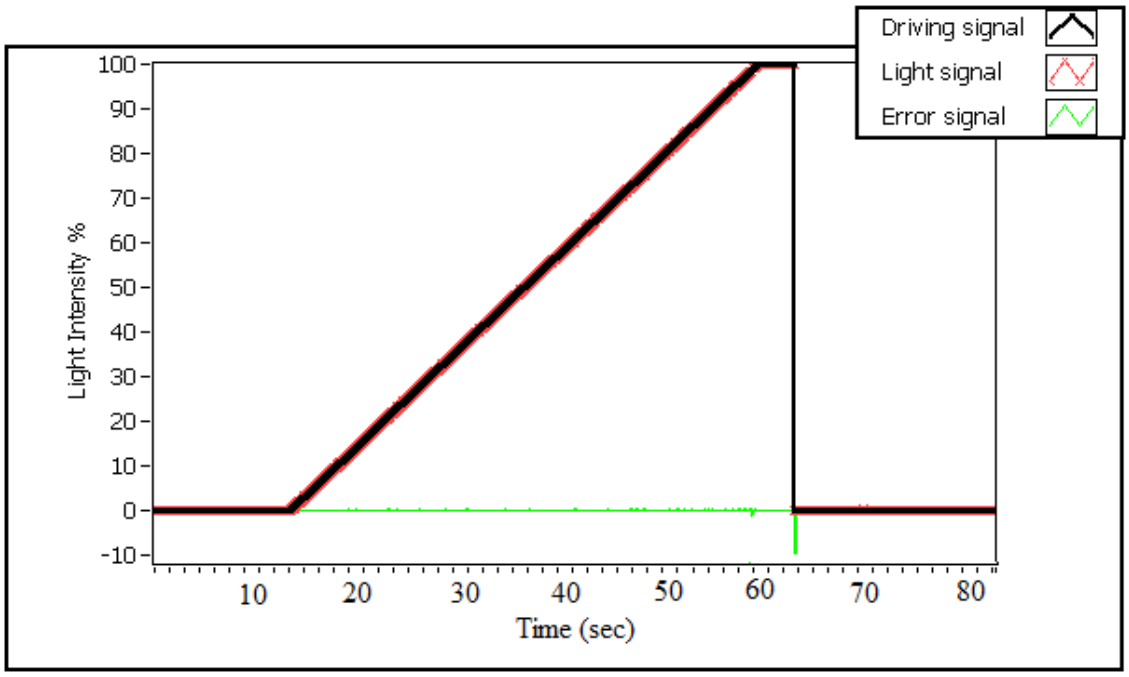

Figure.8 Driving signal, Temperature signal and Error signal graph for the OSL unit

3.4.2 FPGA logic for OSL

The logic for the generation of the ramp signal for OSL, with its required rate and hold-time is similar to the TL logic described above but the control logic for OSL is different. For optical stimulations, the change in the driving signal is immediately reflected in the intensity of light, whereas for thermal stimulation, there is a delay between the change in the driving signal and its corresponding effect in the temperature due to thermal response of the heater plate.

The error signal produced by the FPGA generated ramp signal and the feedback signal is used to generate a signal depending on the intensity rate and the OSL mode—LM-OSL or CW-OSL. The analogue form of this signal is used to drive the LED driver circuit.

3.5 FPGA

In the present study, FPGA was used as a main tool to control TL/OSL parameters. FPGAs are programmable digital logic chips that are based around a matrix of configurable logic blocks connected through programmable interconnect. The emergence of FPGA bridges the gap between the processing power of hardware and the flexibility of software. Almost any

digital circuit can be formed in an FPGA by writing the appropriate code for it. FPGAs allow designers to change their designs very late in the design cycle – even after the end product has been manufactured and deployed in the field. The major companies producing FPGA are Xilinx and Altera.

FPGAs operate at a higher clock rate than most micro-controllers used in similar systems [8] which implies that a faster corrective action based on the feedback is possible. Due to this a more precise control over the heating rate and light power delivery to the sample is possible. FPGA also makes it possible for the driving signals, i.e. the temperature and light ramp signal, to have higher resolution which is limited only by the resolution of the accompanying ADC and DAC.

The basic objective in using FPGA was to increase the processing speed by executing the operations in parallel at the hardware level. Since the program written for FPGA creates the corresponding digital hardware circuit in the FPGA IC, perfect parallelism can be achieved. Different hardware, completely independent of each other, can be fabricated in the same FPGA IC. So unlike the sequential execution in a processor, concurrent or parallel execution occurs in FPGA. Due to this the different processes of the system can run independently of each other without causing any interference. The use of such technology based on a single microchip has helped in making a reliable control system.

FPGA can be configured by the user with a hardware description language (HDL). An HDL is used to describe any digital hardware design. It can be simulated to check for its behaviour. A bit file can then be generated by which the FPGA will be configured. VHDL and Verilog are the most commonly used languages for FPGA. VHDL stands for VHSIC Hardware Description Language where VHSIC stands for Very High Speed Integrated Circuit. VHDL is based on Ada programming language. It was developed by the department of defence of US in 1981. In 1986 the rights were given to Institute of Electrical and Electronics Engineer (IEEE). VHDL employs a top-down approach where the design is partitioned into smaller blocks.

Verilog was developed by Gateway Design Automation in 1980. Cadence Design later acquired it and made it public in 1990. IEEE standardized it in 1995. It is very similar to the C programming language. Thought there are many differences between VHDL and Verilog, the choice of the programming language mainly depends on personal preferences and available tools.

Spartan-6 LX9 Micro Board was chosen for this application because of its compact size (9.5 cm x 3.5 cm); low cost ($89) and USB interface (via USB-to-UART interface). This FPGA kit is manufactured by Avnet using the Spartan-6 LX9 FPGA from Xilinx. Figure 9 shows the Spartan-6 LX9 micro board with the ADC kit and DAC kit attached to it. The ADC kit is *Pmod AD1* from M/s Digilent, USA having AD7476A IC. It is a 12 bit serial ADC with maximum sampling speed of 1 MSPS (million samples per second) [9]. The DAC kit is *Pmod DA2* also from M/s Digilent, USA having DAC121s101 integrated circuit which is a 12 bit serial DAC with the output settling time of 8 µs typically [10].

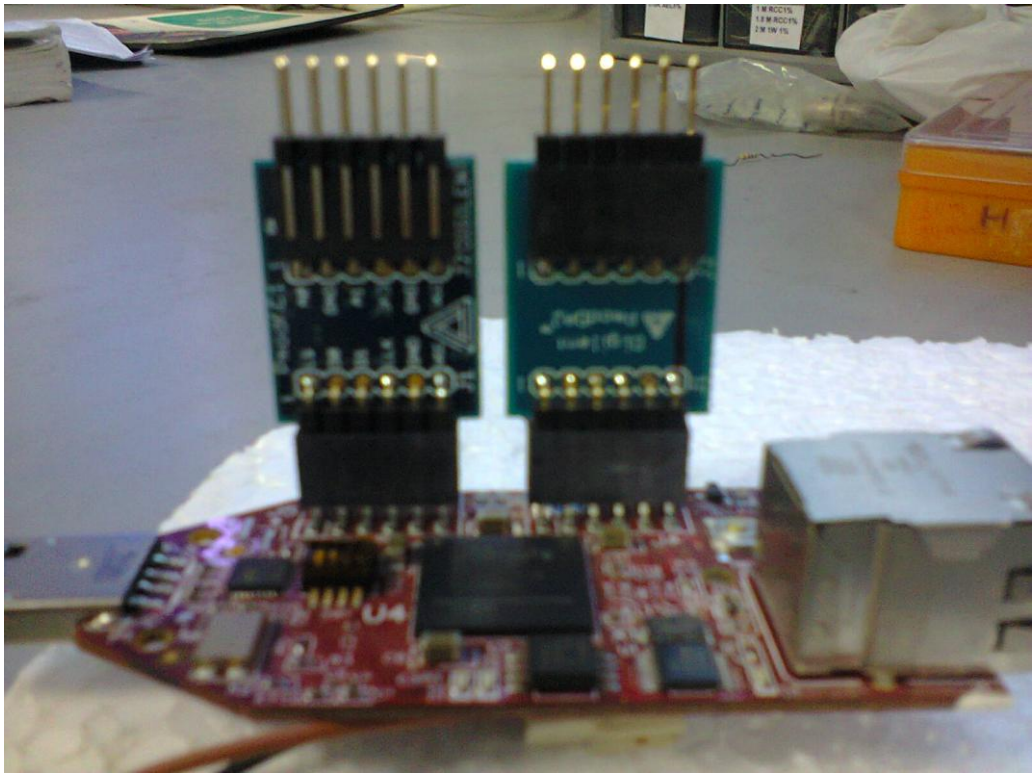

Figure 9 Spartan-6 LX9 micro board with ADC and DAC kits attached to it

3.6 Transformer design

A compact transformer is desirable for the system. Ferrite core transformers are more compact compared to their iron core counterparts. Their drawback is that they require high frequency current which puts a limit to the current carrying capacity of the transformer due to the problem of skin effect at higher frequency. Skin effect is the tendency of the current to flow more and more at the surface of the conductor as its frequency increases. Due to this the

current carrying capacity of the conductor decreases as the inner part of the conductor is not available for current conduction.

This problem of skin effect is overcome by using Litz wires which are able to carry higher level of current at high frequencies. Litz wire consists of many thin wires individually coated with an insulating film and twisted or woven together, following one of several carefully prescribed patterns often involving several levels. The following sections deals with the theoretical considerations in the design of this transformer and enumerates the design of the transformer used here.

3.6.1 Theoretical considerations in the design

The different parameters to be considered in the design of the ferrite core transformer are its size, magnetic flux density, operating voltage, number of primary and secondary turns, frequency and shape of the voltage waveform. All these parameters are inter-related and affect each other as shown in the following formula (adapted from [10]):

$$A_c = \frac{V_p \times 10^8}{P \times F_o \times N_p \times B_{\max}} \quad \text{.....(1)}$$

Where A_c is the effective core area in cm^2, F_o is the input frequency in hertz, N_p is the number of primary turns, V_p is the primary input voltage in volts, B_{max} is the maximum flux density in gauss. Value of B_{max} is given in the datasheet of the core, half of this value is taken for the above formula. The value of P in the above equation depends upon the shape of voltage waveform.

Increasing B_{max}, A_c can be reduced but it will cause higher core loses resulting in higher core temperatures. N_p could be increased to reduce A_c. However, higher N_p will require more space, so A_c could not be reduced. Also higher N_p implies more copper wire will be used, implying higher copper losses. This will cause heating of the windings which will reduce efficiency. F_o could be increased to reduce A_c but higher F_o will cause skin effect and proximity effect to be prominent. This will reduce the current carry capacity of the wires and increase the problem of EMI. Thus an optimized designing of the transformer requires many trade-offs.

Equation (1) clearly states that the size of the transformer is a function of its voltage, shape of the voltage waveform, frequency, number of primary turns, and maximum flux density. Each of these factors is separately considered in order to design an optimal transformer:

A transformer used at a frequency lower than the frequency for which it is designed will lead to saturation of the transformer, as can be seen from the equation below which is a rearranged form of equation (1)

$$B_{\max} = \frac{V_p \times 10^8}{P \times F_0 \times N_p \times A_c}$$

Using the transformer at a higher frequency will also work if it is not used beyond its current capacity.

Along with frequency, the number of primary turns also affects the size of the transformer. From the above formula it is seen that as the number of primary turn increases, the size of the transformer decreases. However, there is a limit to the number of primary turns due to physical constraints.

The shape of the voltage waveform is critical as the value of P in equation (1) depends on it and thus determines the size of the transformer. If the input is a sine wave as shown in figure 10 then the value of P is 4.44 [11]. For symmetrical square wave as shown in figure 11 value of P becomes 4 [11].

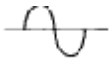

Figure 10 **Figure 11**

The equation (1) gets modified as follows for the wave shapes shown in figures 12 and 13.

$$A_c = \frac{V_p \times t \times 10^8}{P \times N_p \times B_{\max}}$$

Figure 12

Figure 13

For interrupted symmetrical wave form shown in figure 12, the value of P is 2 [11]. For the unidirectional rectangular shaped wave form shown in figure 13, the value of P is 1 [11].

3.6.2 Design of the transformer used in the system

A low voltage high current transformer is designed for this system. Low voltage facilitates better control over the transformer power delivery because a minor change in voltage would cause a major change in current. 1 volt is fixed as the secondary voltage of the transformer. The corresponding current at the secondary would be a maximum of approximately 50 A.

Such a high current causes problems due to skin effect which deteriorates as the frequency is increased. However, the frequency needs to be sufficiently high in order to use a compact ferrite core. Due to this the frequency is fixed at 30 KHz. At this frequency and current, litz wires have to be used. The Litz wire designed for the secondary is such that only one turn is possible due to physical constrains.

The secondary voltage is fixed at 24 V. The size of the transformer is directly proportional to the secondary voltage as can be seen from equation (1). Using the following formula, the number of primary turn is calculated

$$N_p / N_s = V_p/V_s$$

Where,

N_p = number of primary turns

N_s = number of secondary turns

V_p = voltage at the primary of the transformer

V_s = voltage at the secondary of the transformer

$$N_p = \quad N_s (V_p/V_s) = 1 (24/1) = 24$$

The primary will have 24 turns while the secondary will have one turn. The primary voltage will be 24 V and the secondary voltage will be 1 V.

The thickness of the wire for the primary turns can be calculated from the amount of current which will pass through it. In order to determine this current the following equation is used:

$$V_p I_p = V_s I_s$$

Where,

V_p = primary voltage,

I_p = primary current,

V_s = secondary voltage,

I_s = secondary current

$$I_p = (1 \times 50)/24 = 2.08 \text{ A}$$

So three wire of 0.7239 mm thickness, coated with an insulating film, having a current capacity of 1.2 A with 100% skin depth at 33 KHz, are joined at both the ends and are used to made the primary turns. Two thicker wires can be used instead of this if proper litz wire configuration is used.

Though sine wave input would result in the smallest transformer, it is not used here since PWM technique is used for power control. Hence a rectangular shaped wave will be used. If a symmetrical wave (figure 12) is used rather than a unidirectional wave (figure 13) then the size of the transformer becomes half as the value of P is 2 for the former. To get such a waveform an H-bridge is used.

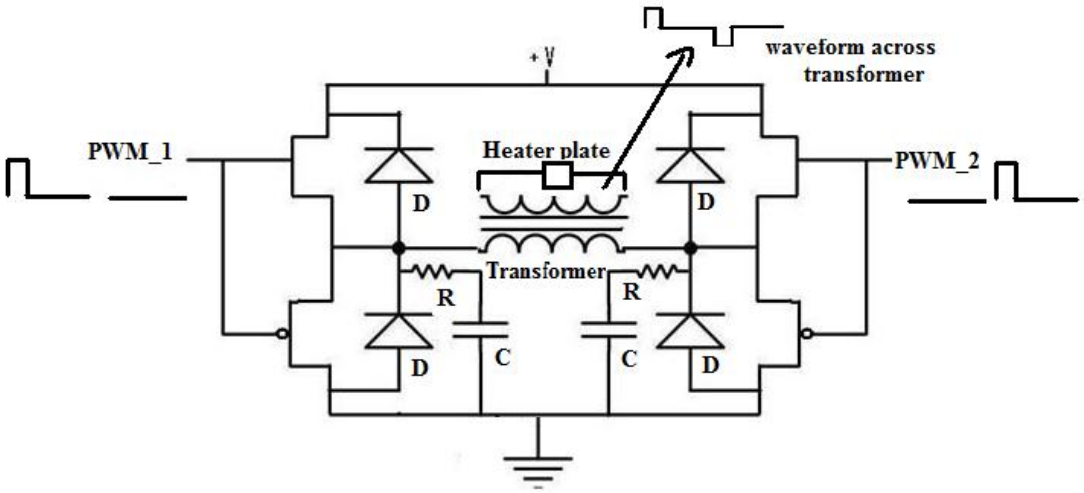

Figure 14. H-bridge circuit. R=33Ω, C = 10nF, D=UF4007

By applying the two PWM inputs as shown in figure 14, we get the required waveform across the primary of the transformer to which this H-bridge is connected. The other advantage of this method is that the duty-cycle of the PWM can range from 0% to 100%. At 100% duty cycle the waveform across the transformer will be like a symmetrical square wave. The pattern of the PWM signal generated in the FPGA is given in figure 14. It also shows the manner in which they are applied at the input of the H-bridge along with the resultant waveform across the transformer due to it.

If some appropriate LC circuit is made at the input of the primary then the shape of the wave could be made more like a sine wave. This would further contribute towards decreasing the size of the transformer and increasing the maximum flux density capacity.

H-bridge circuits are available as ICs. They are mainly used to drive motors in both the directions. In this application it is used to drive the transformer bi-directionally. L6203 H-bridge IC has been used here. It can handle 4 A current and can be used for frequencies up to 100 kHz [12]. External snubber circuits have to be made to limit the high voltage transient during turn-off and to limit the high current transient during turn on.

Appropriate ferrite core has to be selected for this transformer. If the ferrite core of Epcos is considered, then there are different cores having different properties like N27, N87, N97, N48 etc. Their magnetic fluxes at 25 °C, along with their optimal frequency ranges, are 5000 gauss (25 to 150 KHz), 4900 gauss (25 to 500 KHz), 5100 gauss (25 to 500 KHz) and 4200

gauss (0.01 to 0.1 MHz) respectively. N87 material whose flux density is 4900 gauss is selected for this application [13]. For the formula given in equation 1, half of the maximum value of its flux density is considered.

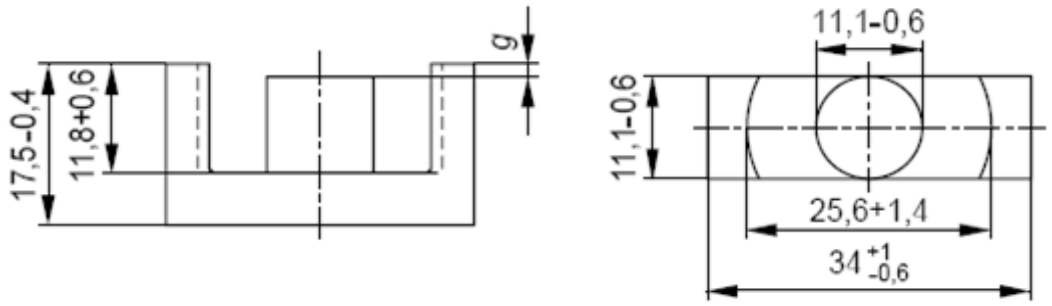

Figure 15. Shape and size of ETD 34/17/11

Since all the terms needed in equation (1) are now obtained above the effective core area is calculated as follows:

$$A_c = \frac{V_p \times 10^8}{P \times F_0 \times N_p \times B_{\max}}$$

$$A_c = (24 \times 10^8)/ 2 \times 30000 \times 24 \times 2450 = 0.68027211 \text{ cm}^2 = 68.02 \text{ mm}^2$$

From the different datasheet of cores of Epcos it is found that ETD 34/17/11 (the numbers indicates its dimensions—length, breath, and thickness) has the area of 91.6 mm^2 minimum. Thus it is suited for the purpose. ETD 34/17/11 is shown in figure 15 [13]. With this the transformer is fabricated with the number of turns and type of wires as described earlier.

3.7 Labview

A user-friendly GUI has been developed (figure 16) using LabVIEW (Laboratory Virtual Instrument Engineering Workbench), from M/s National Instrumentation. LabVIEW is a system-design platform and development environment for creating custom applications including data acquisition, graphical display of data, data analysis, signal processing, automation and instrument control. Labview uses graphical programming language [14].

The GUI provides graphical display of the whole process i.e. driving signal, feedback signal obtained from the thermocouple and photodiode, the error signal for both TL and OSL process. Due to the use of UART-to-USB interface, a USB port suffices for this system. This is advantageous as laptops usually do not provide facility for URAT interface.

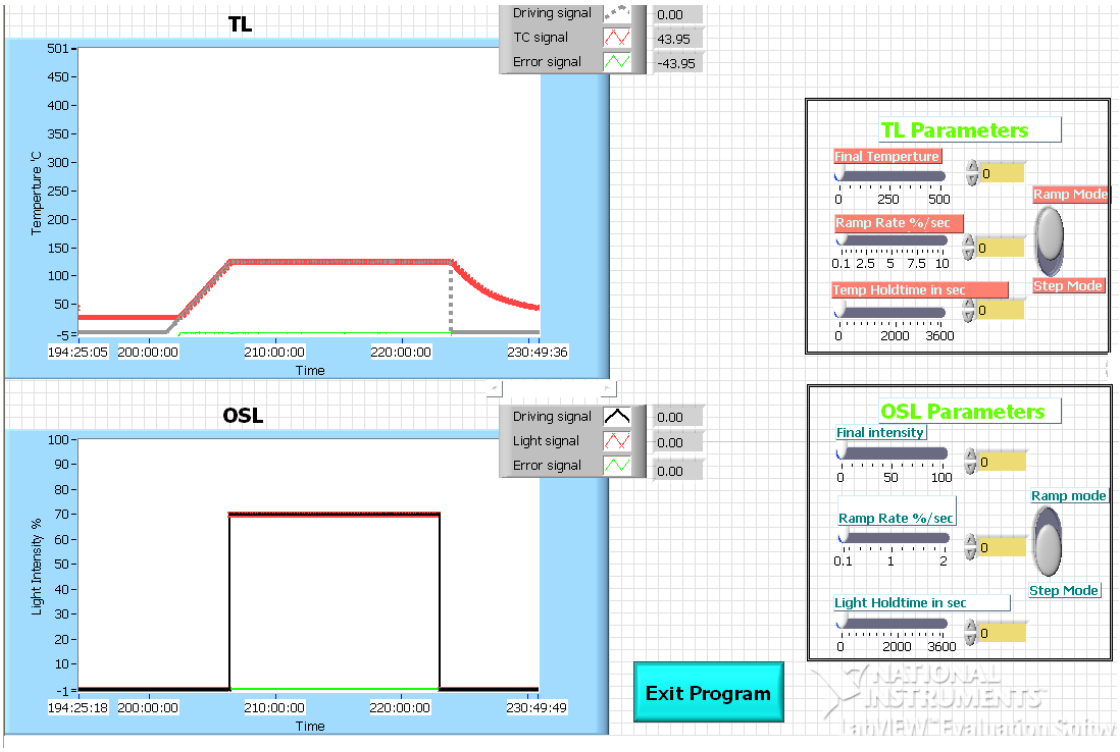

Figure 16. Labview based GUI with the visual display of the stimulation process

3.8 RS232

The RS232 standard specifies signal voltages, signal timing, signal function, a protocol for information exchange and mechanical connectors. The signal transmission is bipolar, requiring two voltages from 5 to 25 volts of opposite polarity. A RS-232 voltage translator IC does the matching of the voltages between the FPGA and the RS-232 requirement. A code for RS-232 protocol from Xilinx is incorporated in the FPGA which manages the data transfer between the computer (GUI) and the FPGA. From the GUI the user parameters are transferred to the FPGA and from FPGA the driving signals and feedback signals of TL and OSL are transferred to the GUI where they are graphically displayed.

3.9 Light detector (EMCCD)

EMCCD is used as a light detector in this system set-up. It is an image sensor that is capable of detecting single photon events without an image intensifier, achievable by way of a unique electron multiplying structure built into the chip. Traditional CCD cameras, often referred to as ‘slow scan’ cameras, offers high sensitivity, with low readout noises but at the expense of slow readout [15]. The fundamental constraint comes from the CCD charge amplifier. To have high speed operation the bandwidth of the charge amplifier needs to be as wide as possible. However the noise increases as the bandwidth of the amplifier increases. Slow scan CCDs have relatively low bandwidth and hence can only be read out at modest speeds typically less than 1 MHz. EMCCD cameras overcomes this fundamental physical constraint by amplifying the charge signal before the charge amplifier and hence maintain unprecedented sensitivity at high speeds. By amplifying the signal the readout noise is effectively by-passed and readout noise is no longer a limit on sensitivity [15].

Figure 17. Andor iXON DU-897 EMCCD camera

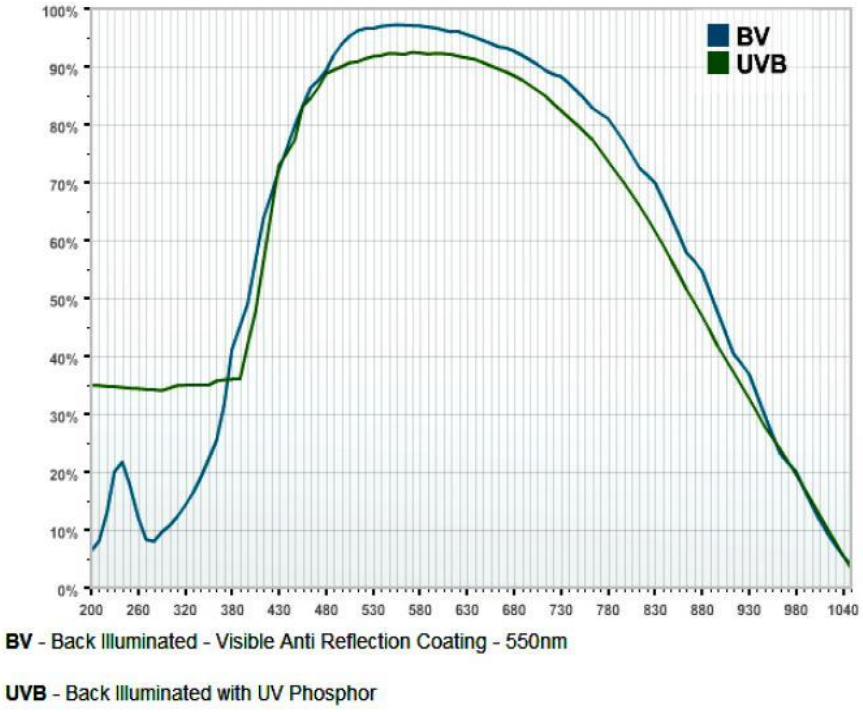

Figure 18. Spectral range of iXON DU-897 EMCCD camera

A high sensitive back illuminated EMCCD camera from Andor is used here. The model of the camera is iXON DU-897 (figure 17). It is a back illuminated EMCCD camera with UVB coating. Its spectral range is from 300 nm to 1000 nm [16]. Figure 18 shows the response of the EMCCD camera with a peak efficiency of 95% at about 550 nm, 80% in blue region (450 nm) and 35% in UV region (380 nm) [16]. It has a pixel array of 512×512 with16 μm x 16 μm each resulting in a chip size of 8.2 mm × 8.2 mm and can function in both frame transfer and conventional mode. At full resolution, it has a maximum frame rate of 35 frames per second. It has single photon counting efficiency and can go up to a gain of 1000 in Electron Multiplying (EM) mode. In EM mode the signal intensity is increased by impact ionization which is similar to PMT and readout noise is <1e per pixel. In addition to EM gain there is conventional gain, which can further enhance the signal intensity. The internal Peltier cooler can cool the EMCCD chip up to -100 °C thus reducing the thermal noise. The integration area can be increased by binning the pixels together. This is done however at the expense of resolution but with improved SNR ratio. The images can be acquired for different times with different readout rates (maximum of 10 MHz, up to a 16-bit dynamic range) and can be accumulated for fixed time period or can also be recorded as a kinetic time series, thus recording the variation of the signal intensity with the time. The system can also do photon

counting of the emitted luminescence. The data acquisition can be initiated both by internal and external triggering. In external triggering, the data acquisition can follow an external clock and can acquire data depending upon the set parameters after receiving the external pulse. Suitable interference filters are used to study the emission in the area of interest.

3.10 Optical set-up

The main criteria of a good optical set-up would be to transfer maximum light to the camera. In order to achieve this, the solid angle of the lens must be very large and the optical aberrations should be at the minimum level possible. In a perfect system all the parallel rays passing through the lens should converge at a single point. However it is not possible to have a completely perfect system. Due to the inherent imperfections of practical optical systems the light passing through the lens does not converge to a single point. This aberration could be chromatic or monochromatic.

Since the behaviour of the optical components is wavelength dependent, the focussing of different wavelength occurs at different focal points, deteriorating the image quality. This type of aberration is called chromatic aberrations. In order to minimize such aberrations, a combination of lens with similar refractive index but opposite signs should be used. The geometrical imperfections of the optical components cause monochromatic aberrations. There are different types of monochromatic aberrations like Chromatic aberration, Astigmatism, Field Curvature, Spherical aberration and Distortions.

The use of a pair of achromatic doublet lens in conjugate mode gave the best results for the optical arrangement of the system. So a pair of achromatic doublet lens of 50 mm diameter and 61.2 mm back focal length, with transmission in 400 to 700 nm range was chosen. Figure 7 (insert) shows the ray diagram of the optical set-up where two achromatic doublet lenses are placed in the conjugate mode such that the plane side of the first lens is towards the sample. This minimizes spherical aberrations. This lens converts the rays of light into parallel beam which is incident on the second lens. The second lens focuses these parallel rays of light on the chip of EMCCD camera. Optical interference filters are placed between the second lens and the EMCCD in order to allow only a particular range of light wavelength to enter the EMCCD.

The optical arrangement is as shown in figure 7. It is housed in a mechanical system which provides the facility for holding the optical components, focusing and easy in change of filters. Figure 19 shows the design of the mechanical housing system for the optics developed in the PRL workshop.

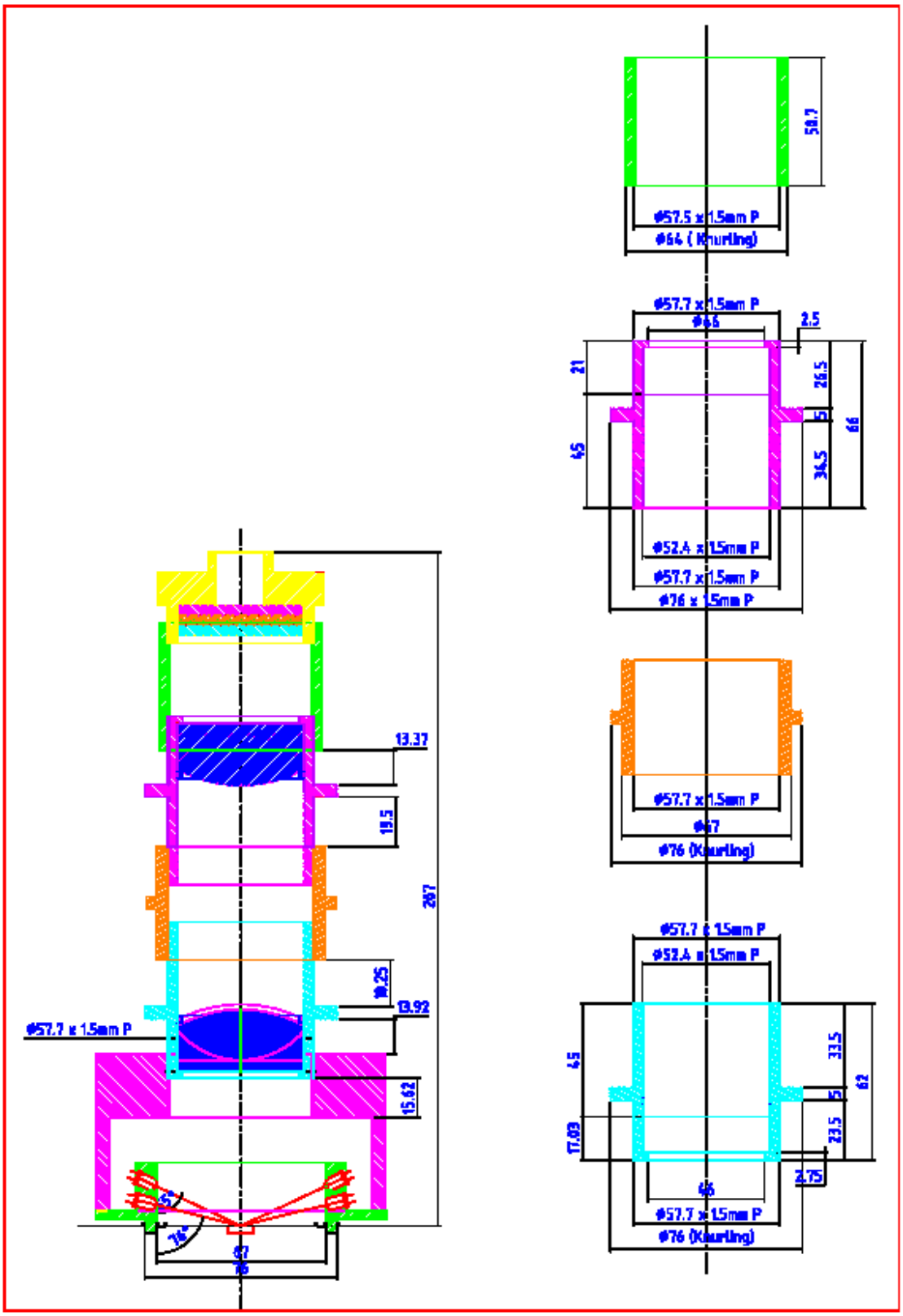

Figure 19. Design of the mechanical housing for the optics

3.11 Performance results

The functioning of the TL and OSL system was tested for dose recovery and in terms of its linearity and errors in thermal and optical stimulation. In order to check more precisely the linearity of the system with respect to time, the timing information was generated in the FPGA itself rather than using the computer timestamp which could be accessed through the Labview software. This timing information was transferred to Labview along with other data. From the timing information, a theoretical ramp was calculated and it was used to check the linearity of the Feedback. Measurements were made for all the rates (0.1 ˚C/s, 0.2 ˚C/s, 0.5 ˚C/s, 1 to 10 ˚C/s in the steps of 1 ˚C). For the OSL system, measurements were made for all the rates from 0.1 %/s to 2 %/s (in the steps of 0.1%).

In the case of TL, it was found that the average standard deviation from linearity was 0.36 ˚C, while the average error was less than 0.35 ˚C. At the hold-time the average variation in temperature is 0.18 ˚C. The correlation between theoretical ramp, ramp generated by the FPGA, and the temperature feedback was found to be 1.

In the case of OSL, it was found that the average of the standard deviation from linearity of all the readings is 0.068%, while the average error was <0.1%. At the hold-time the average variation in light intensity is 0.065%.

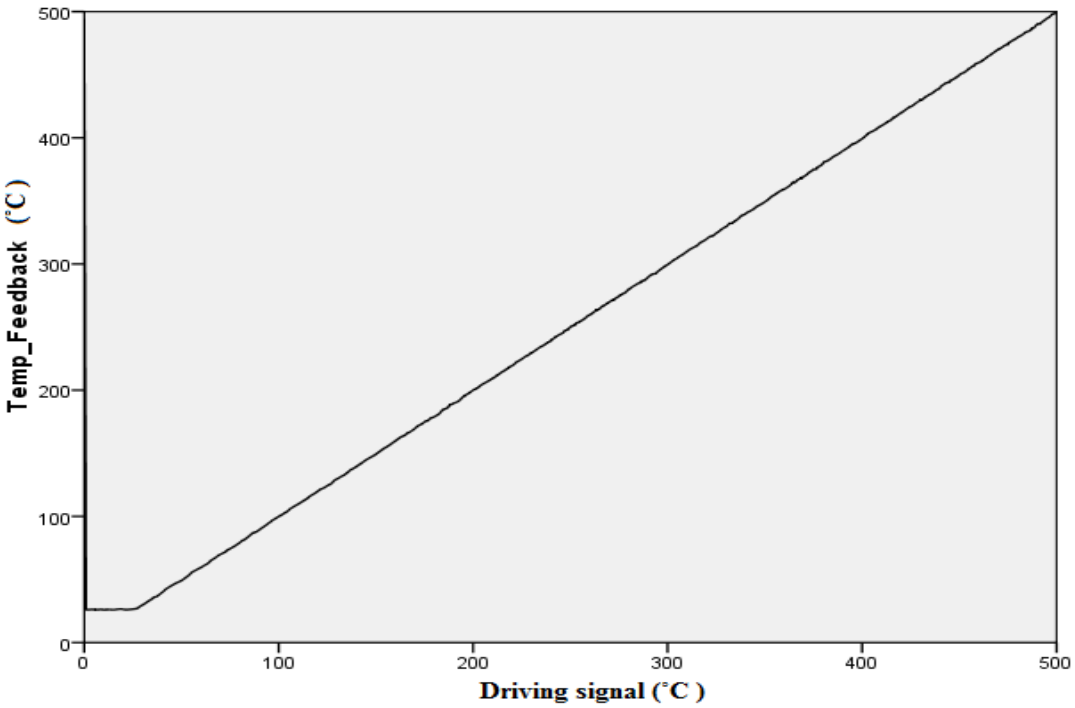

Figure 20. Linearity in thermal stimulation for TL done up to 500 ˚C at 10 ˚C/s with 7 s hold-time

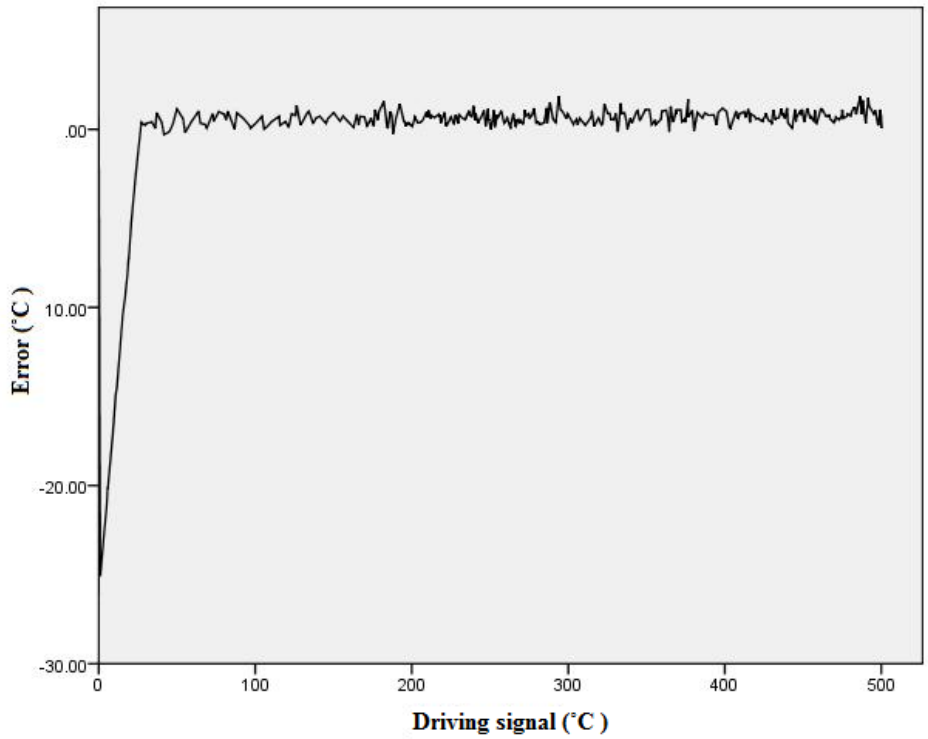

Figure 21. Error in thermal stimulation for TL done up to 500 ˚C at 10 ˚C/s with 7 s hold-time

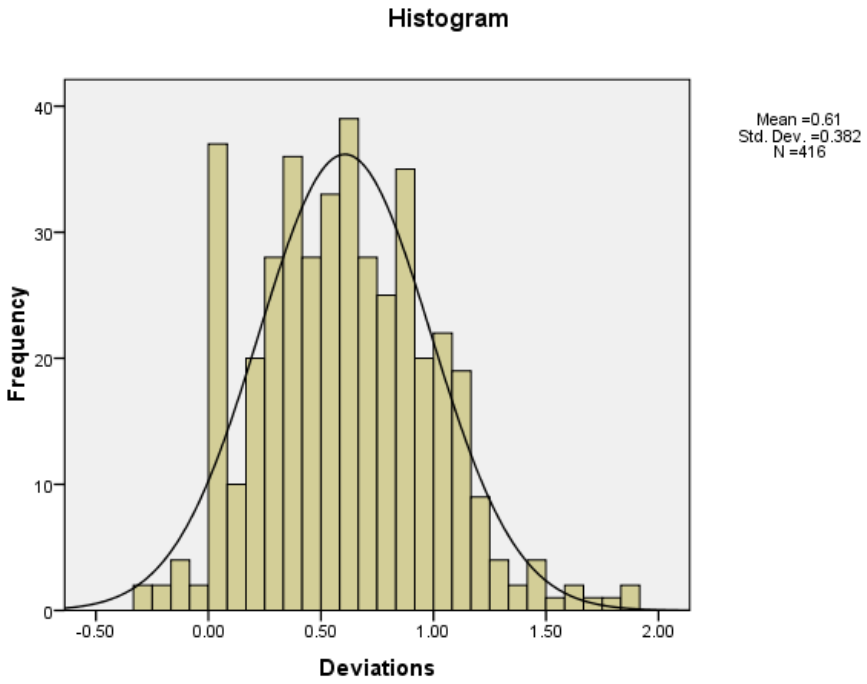

Figure 22. Histogram of deviations from linearity for 500 ˚C at 10˚C/s with 7 s hold-time

Figure 20 to 22 is for TL done up to 500 ˚C at 10 ˚C/s with 7 second hold-time. The linearity of stimulation for this is shown in figure 20. Figure 21 shows the error in this stimulation which is also shown using a histogram in figure 22. The mean error was 0.61 and the standard deviation was 0.382

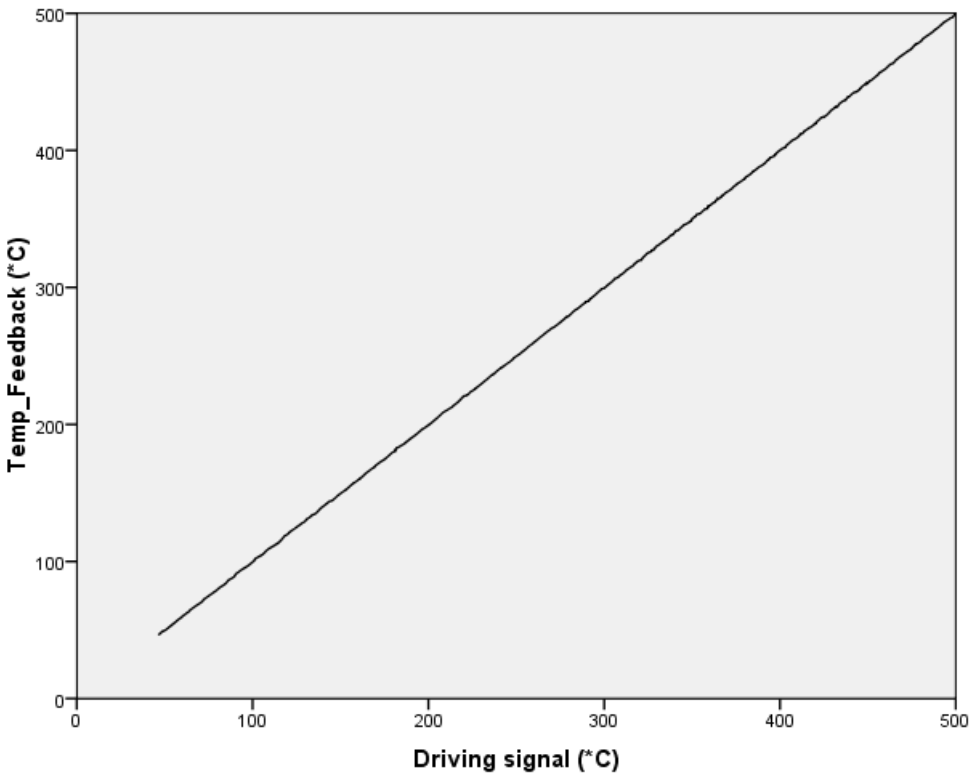

Figure 23. Linearity in thermal stimulation for TL done up to 500 ˚C at 9 ˚C/s with 7 s hold-time

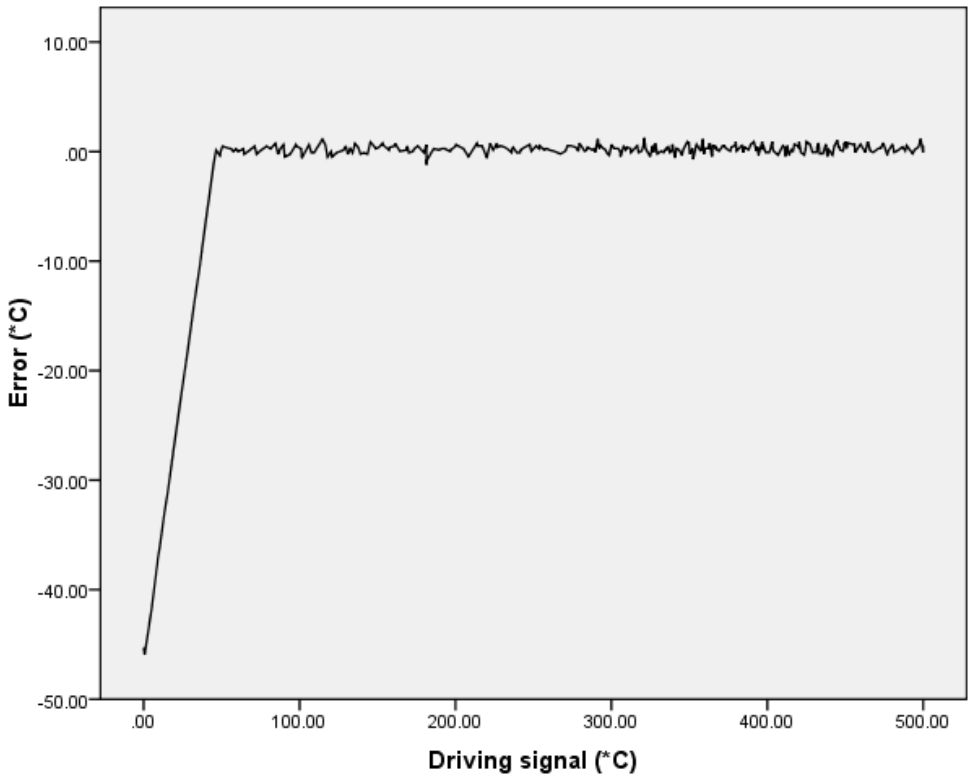

Figure 24. Error in thermal stimulation for TL done up to 500 ˚C at 9 ˚C/s with 7 s hold-time

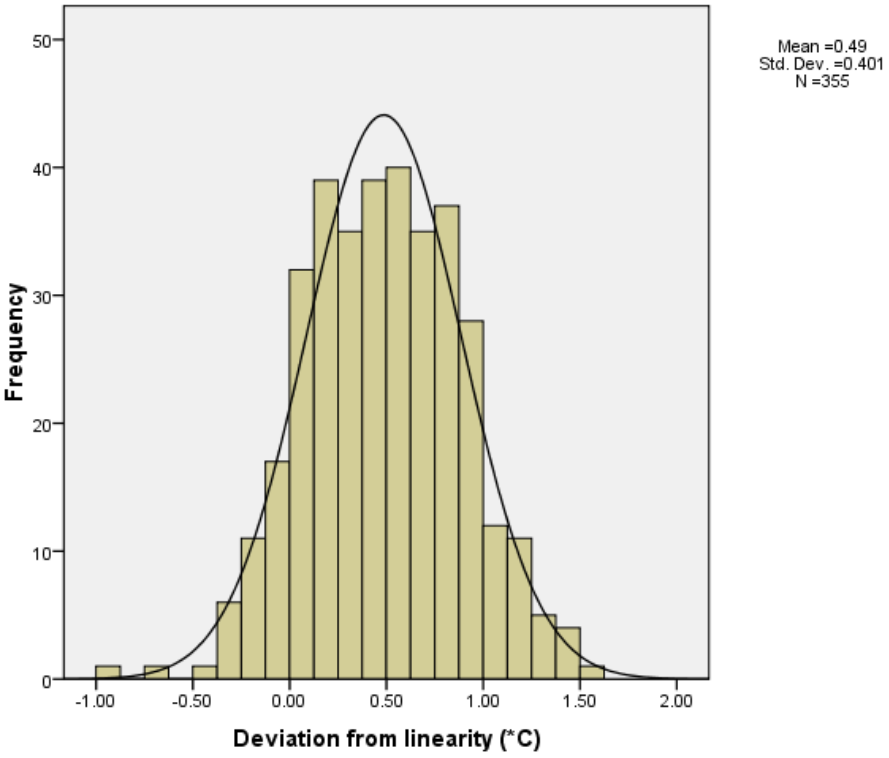

Figure 25. Histogram of deviations from linearity for 500 ˚C at 9 ˚C/s with 7 s hold-time

Figure 23 to 25 is for TL done up to 500 ˚C at 9 ˚C/s with 7 second hold-time. The linearity of stimulation for this is shown in figure 23. Figure 24 shows the error in this stimulation which is also shown using a histogram in figure 25. The mean error was 0.49 and the standard deviation was 0.40

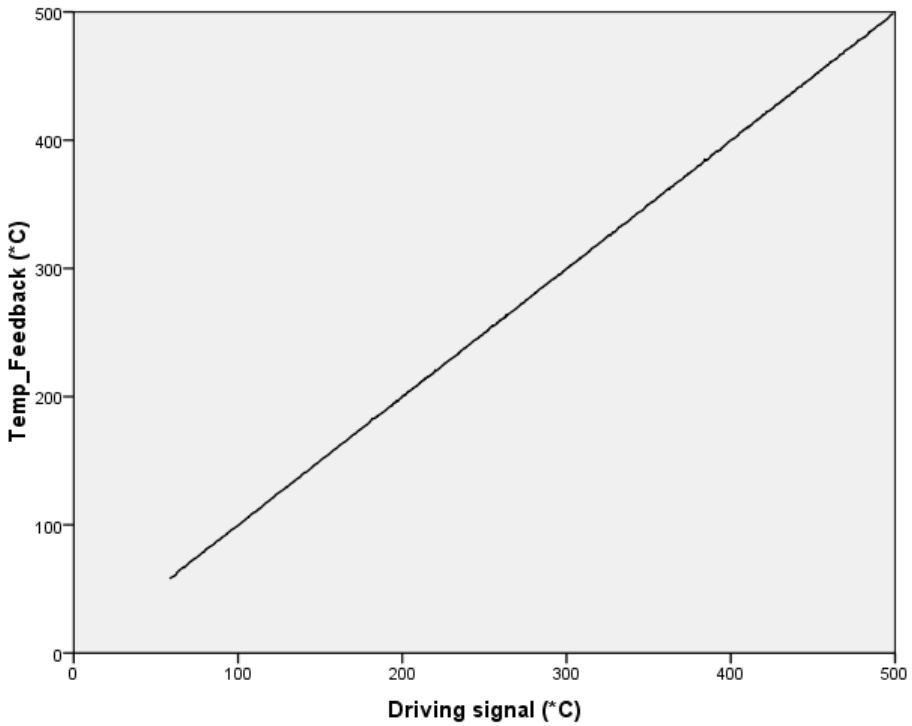

Figure 26. Linearity in thermal stimulation for TL done up to 500 ˚C at 8 ˚C/s heating rate

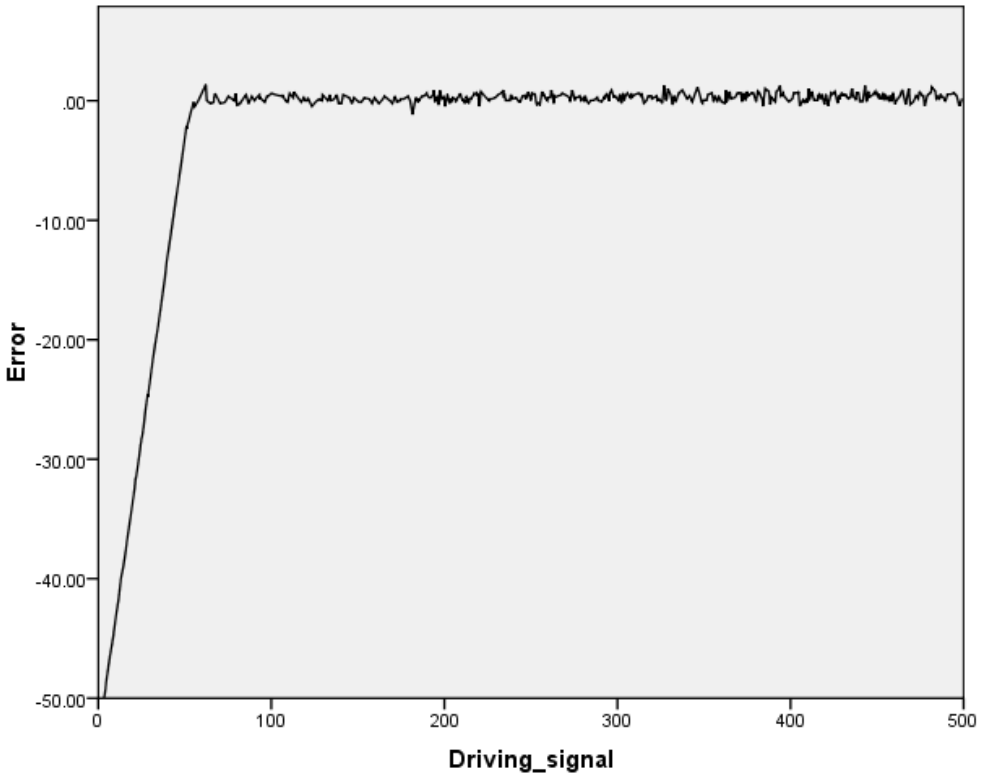

Figure 27. Error in thermal stimulation for TL done up to 500 ˚C at 8 ˚C/s heating rate

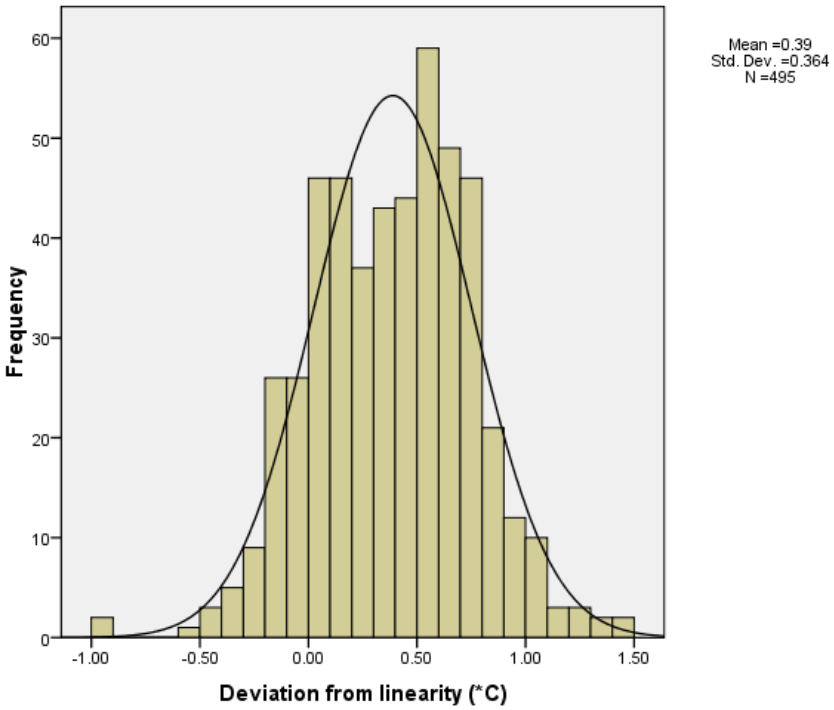

Figure 28. Histogram of deviations from linearity for 500 ˚C at 8 ˚C/s heating rate

Figure 26 to 28 is for TL done up to 500 ˚C at 8 ˚C/s. The linearity of stimulation for this is shown in figure 26. Figure 27 shows the error in this stimulation which is also shown using a histogram in figure 28. The mean error was 0.39 and the standard deviation was 0.364

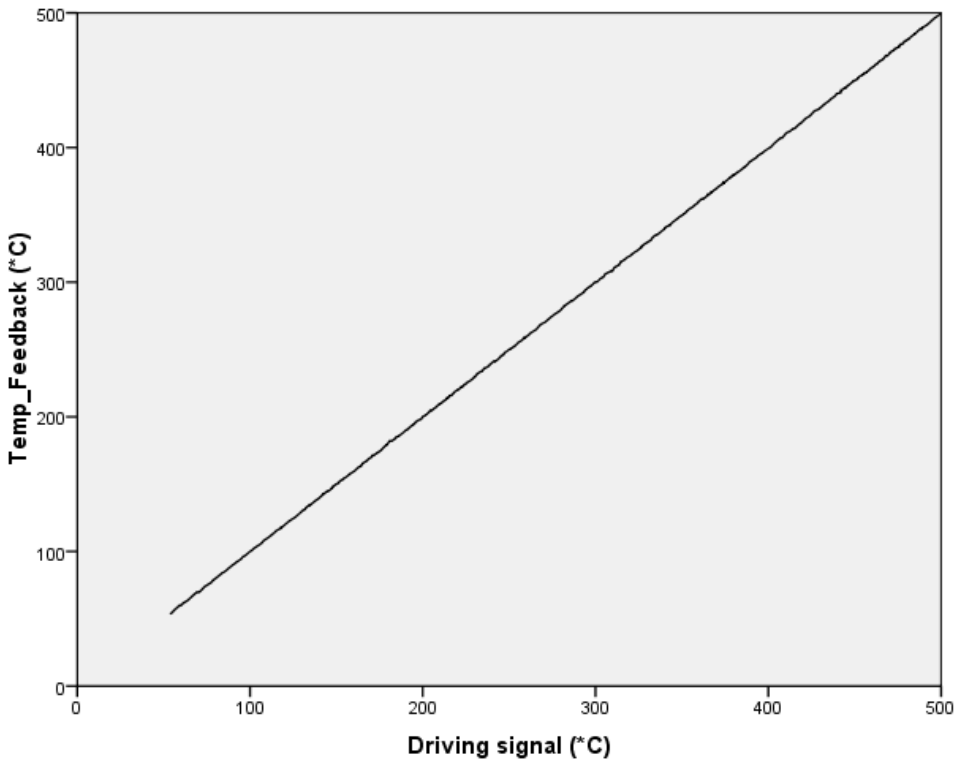

Figure 29. Linearity in thermal stimulation for TL done up to 500 ˚C at 7 ˚C/s with 7 s hold-time

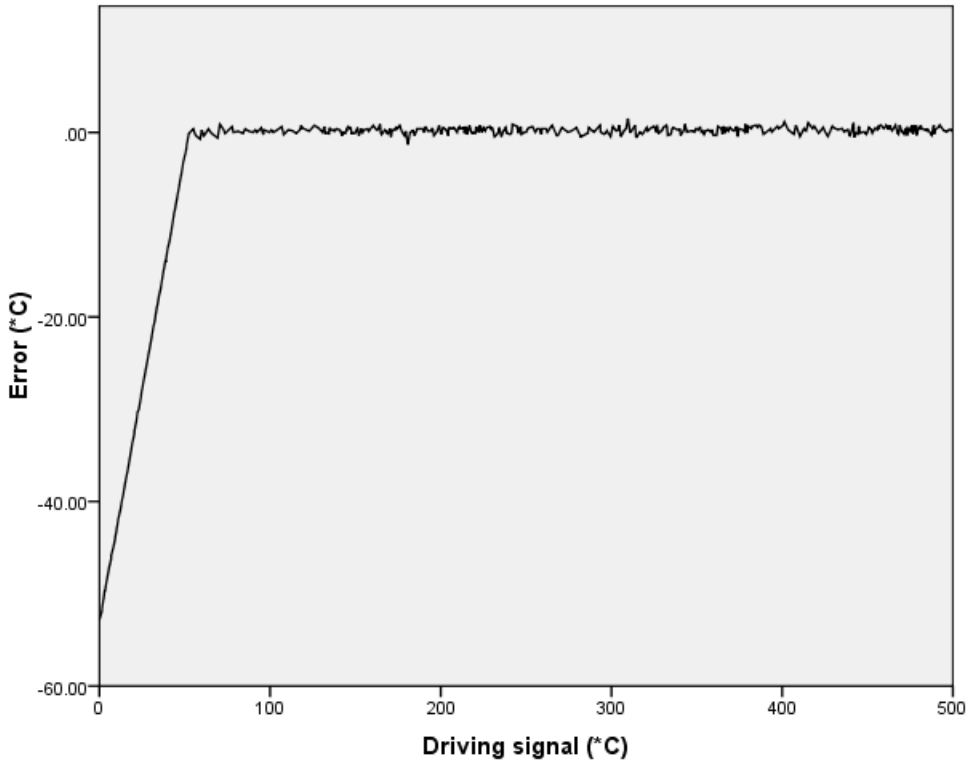

Figure 30. Error in thermal stimulation for TL done up to 500 ˚C at 7 ˚C/s with 7 s hold-time

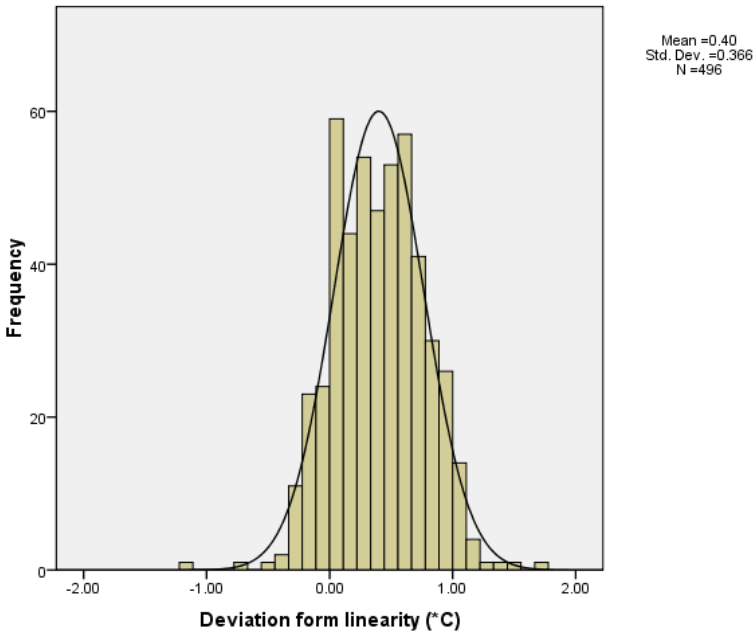

Figure 31. Histogram of deviations from linearity for 500˚C at 7 ˚C/s with 7 s hold-time

Figure 29 to 31 is for TL done up to 500 ˚C at 7 ˚C/s with 7 second hold-time. The linearity of stimulation for this is shown in figure 29. Figure 30 shows the error in this stimulation which is also shown using a histogram in figure 31. The mean error was 0.40 and the standard deviation was 0.366

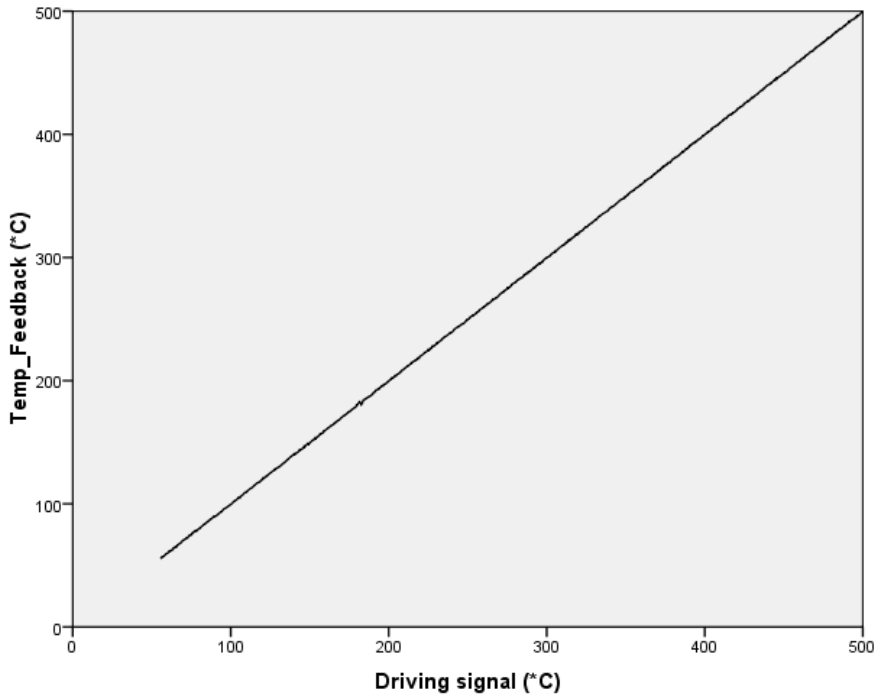

Figure 32. Linearity in thermal stimulation for TL done up to 500 ˚C at 6 ˚C/s with 5 s hold-time

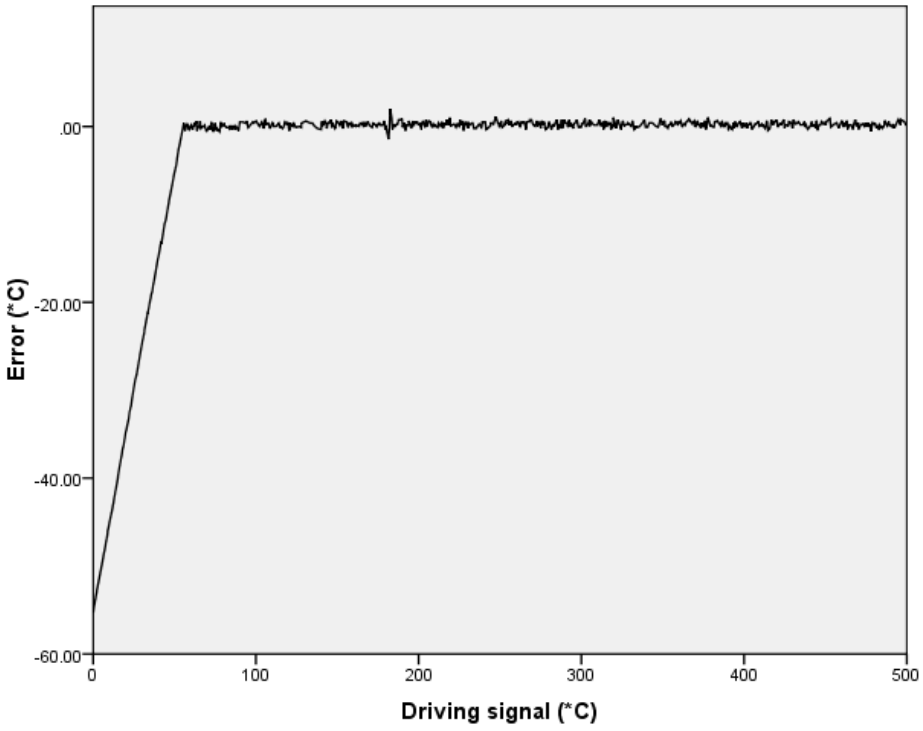

Figure 33. Error in thermal stimulation for TL done up to 500 ˚C at 6 ˚C/s with 5 s hold-time

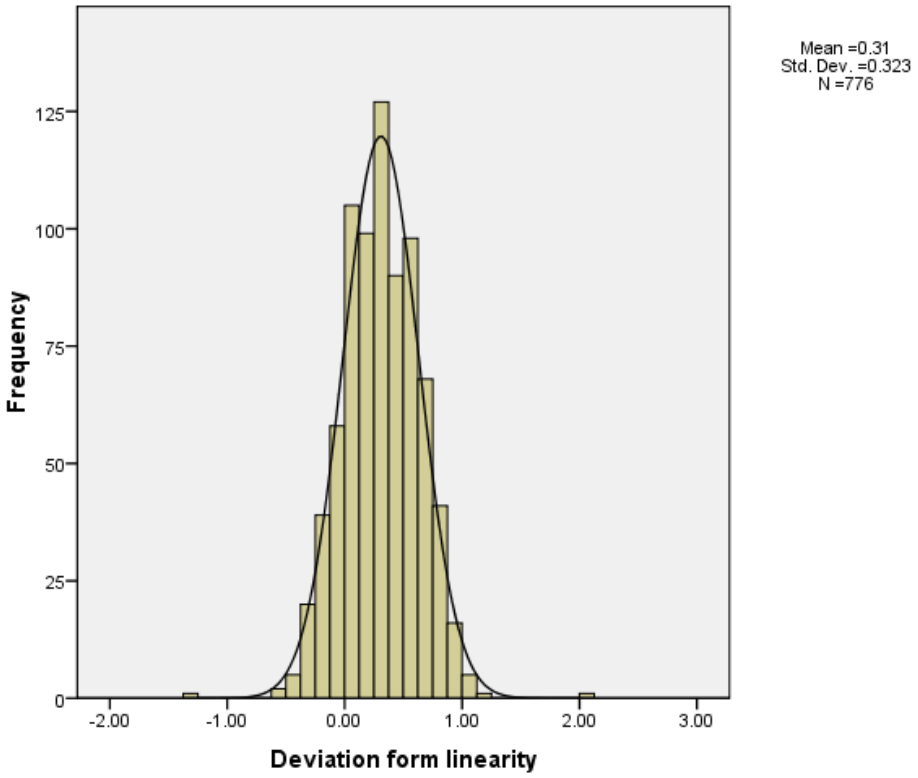

Figure 34. Histogram of deviations from linearity for 500˚C at 6 ˚C/s with 5 s hold-time

Figure 32 to 34 is for TL done up to 500 ˚C at 6 ˚C/s with 7 second hold-time. The linearity of stimulation for this is shown in figure 32. Figure 33 shows the error in this stimulation which is also shown using a histogram in figure 34. The mean error was 0.31 and the standard deviation was 0.323

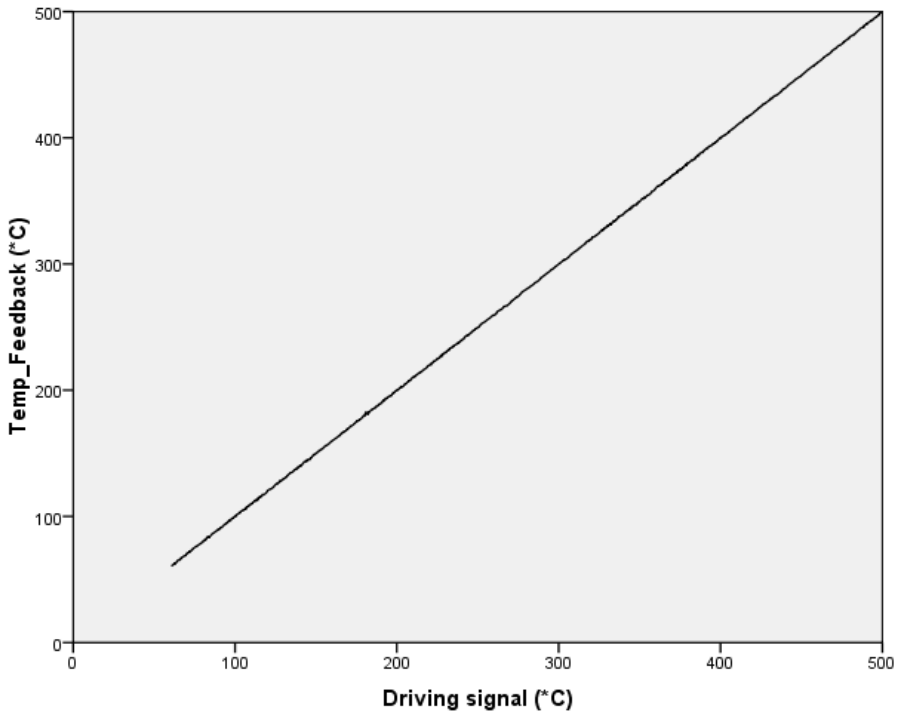

Figure 35. Linearity in thermal stimulation for TL done up to 500 ˚C at 5 ˚C/s with 7 s hold-time

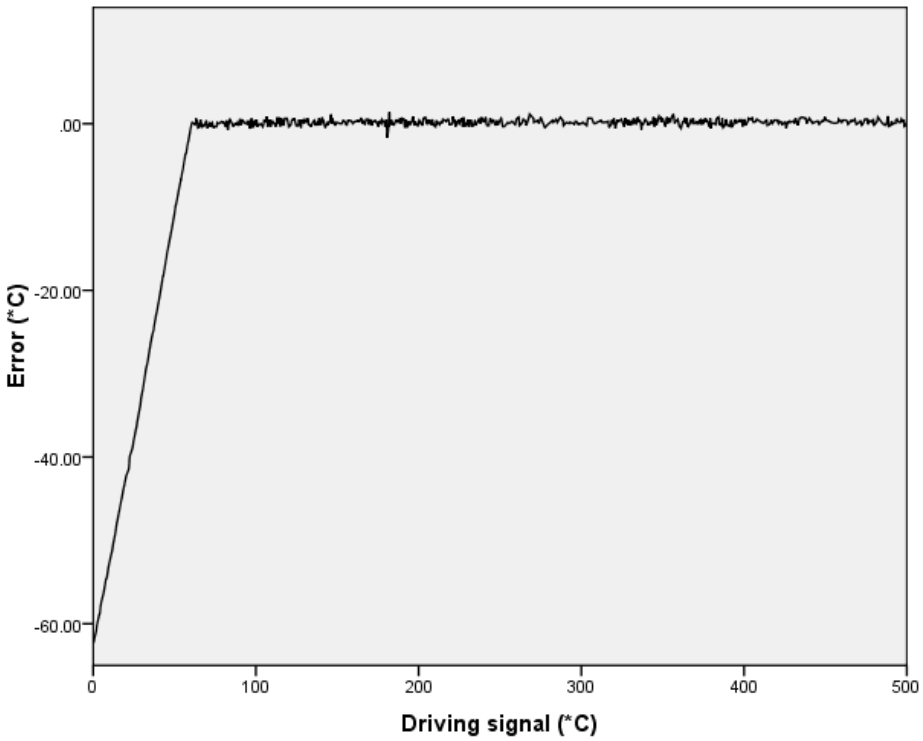

Figure 36. Error in thermal stimulation for TL done up to 500 ˚C at 5 ˚C/s with 7 s hold-time

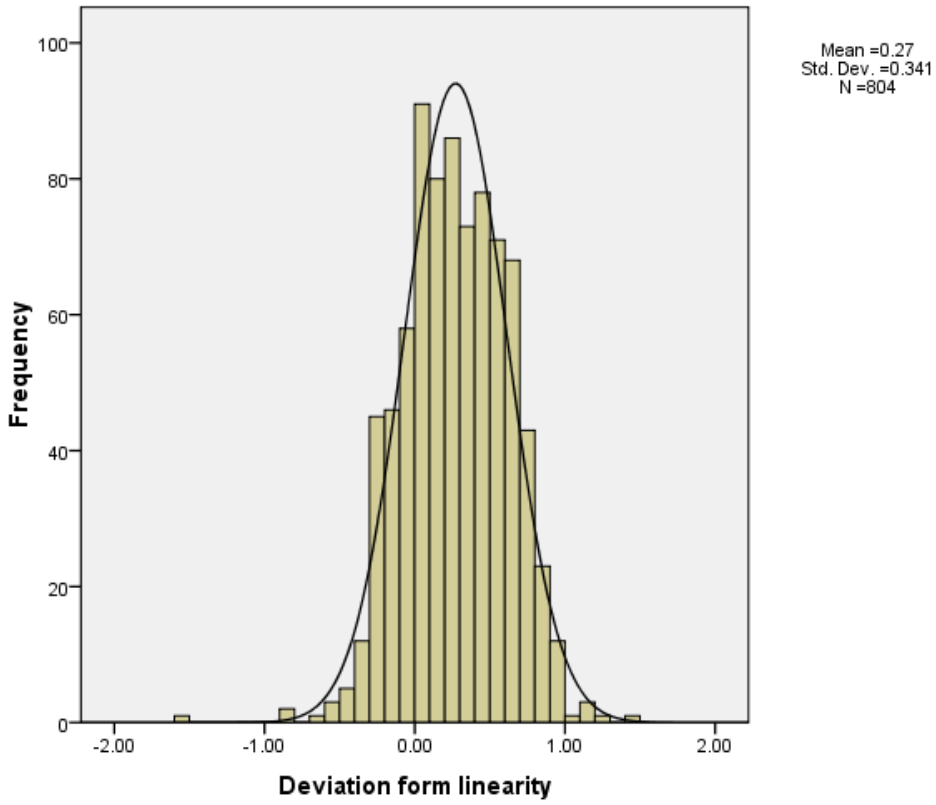

Figure 37. Histogram of deviations from linearity for 500˚C at 5 ˚C/s with 7 s hold-time

Figure 35 to 37 is for TL done up to 500 ˚C at 5 ˚C/s with 7 second hold-time. The linearity of stimulation for this is shown in figure 35. Figure 36 shows the error in this stimulation which is also shown using a histogram in figure 37. The mean error was 0.27 and the standard deviation was 0.341

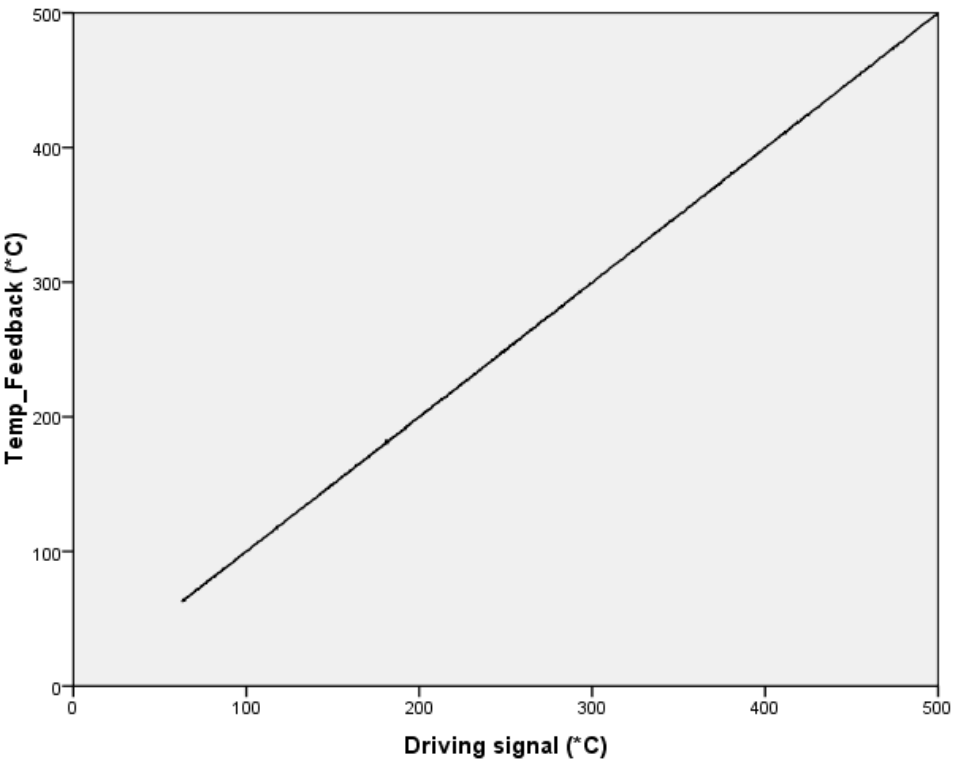

Figure 38. Linearity in thermal stimulation for TL done up to 500 ˚C at 4 ˚C/s with 5 s hold-time

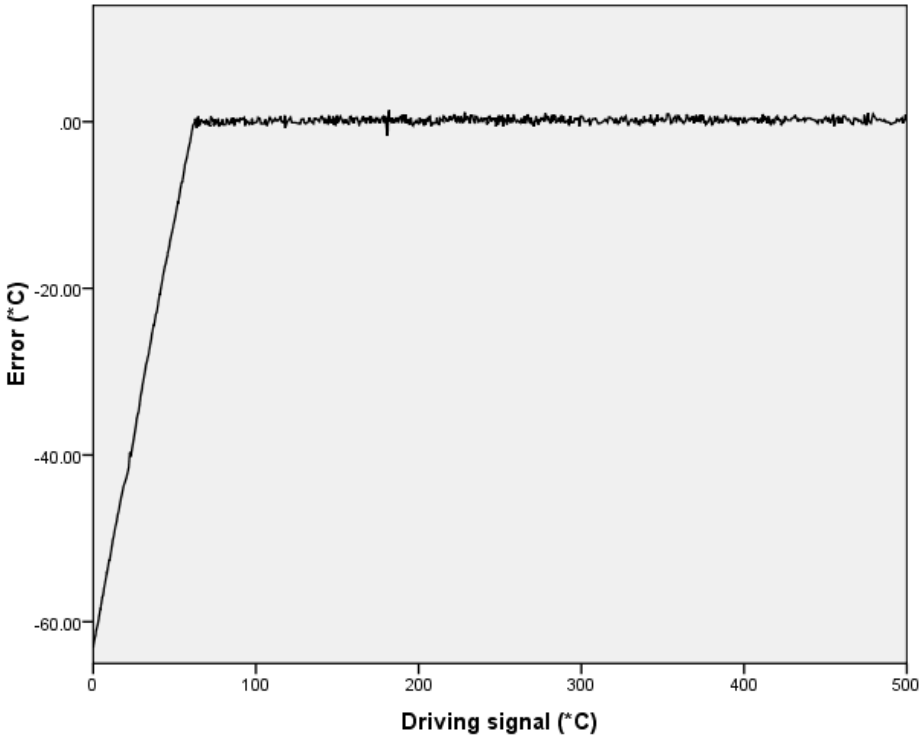

Figure 39. Error in thermal stimulation for TL done up to 500 ˚C at 4 ˚C/s with 5 s hold-time

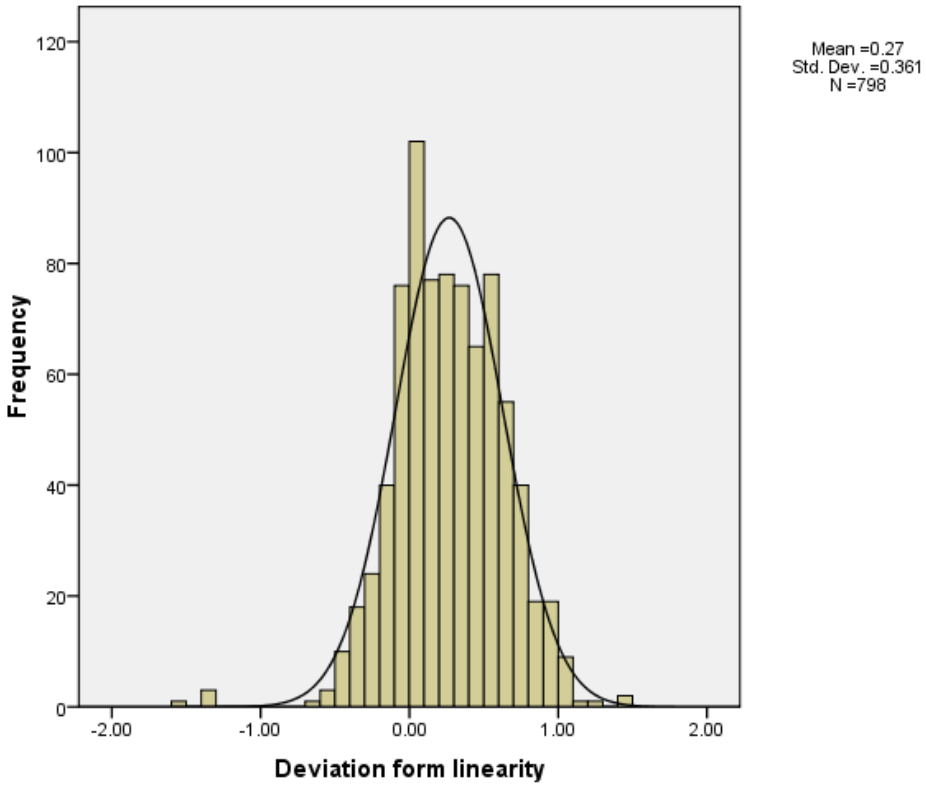

Figure 40. Histogram of deviations from linearity for 500˚C at 4 ˚C/s with 5 s hold-time

Figure 38 to 40 is for TL done up to 500 ˚C at 4 ˚C/s with 5 second hold-time. The linearity of stimulation for this is shown in figure 38. Figure 39 shows the error in this stimulation which is also shown using a histogram in figure 40. The mean error was 0.27 and the standard deviation was 0.361

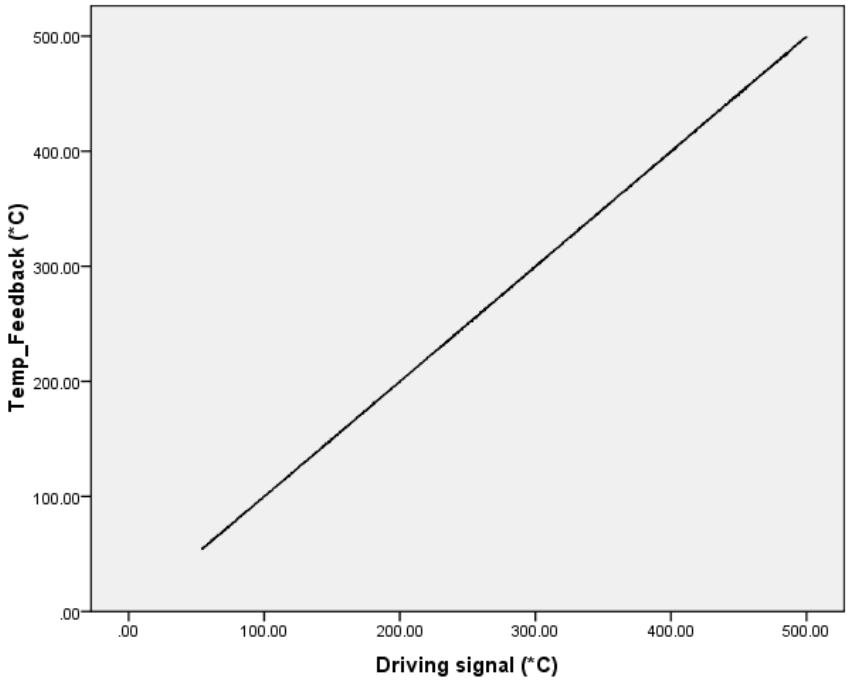

Figure 41. Linearity in thermal stimulation for TL done up to 500 ˚C at 3 ˚C/s with 5 s hold-time

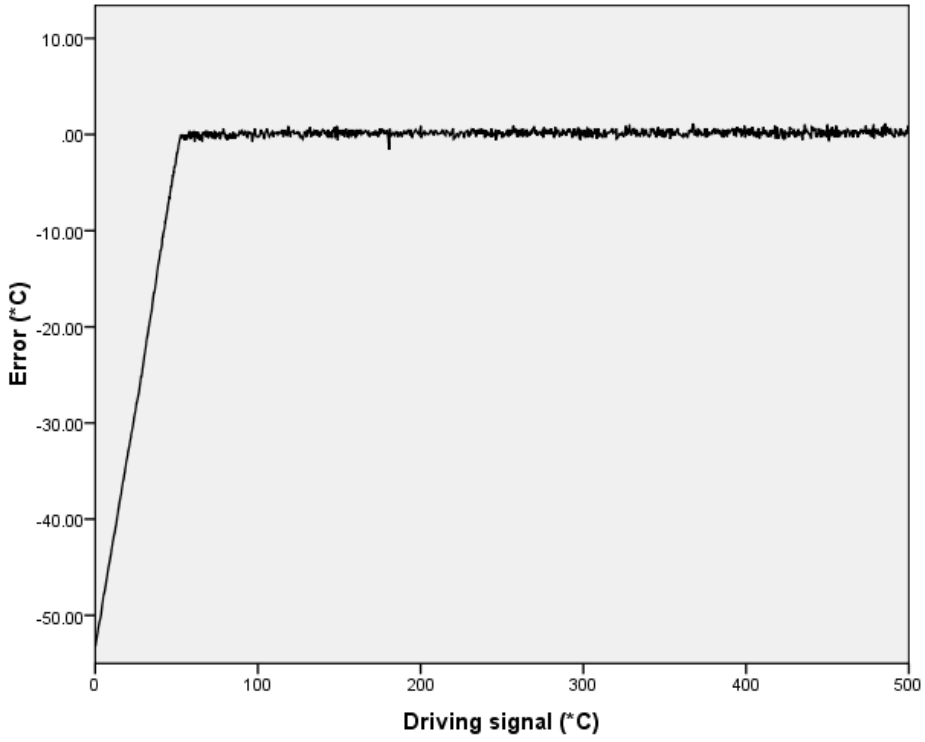

Figure 42. Error in thermal stimulation for TL done up to 500 ˚C at 3 ˚C/s with 5 s hold-time

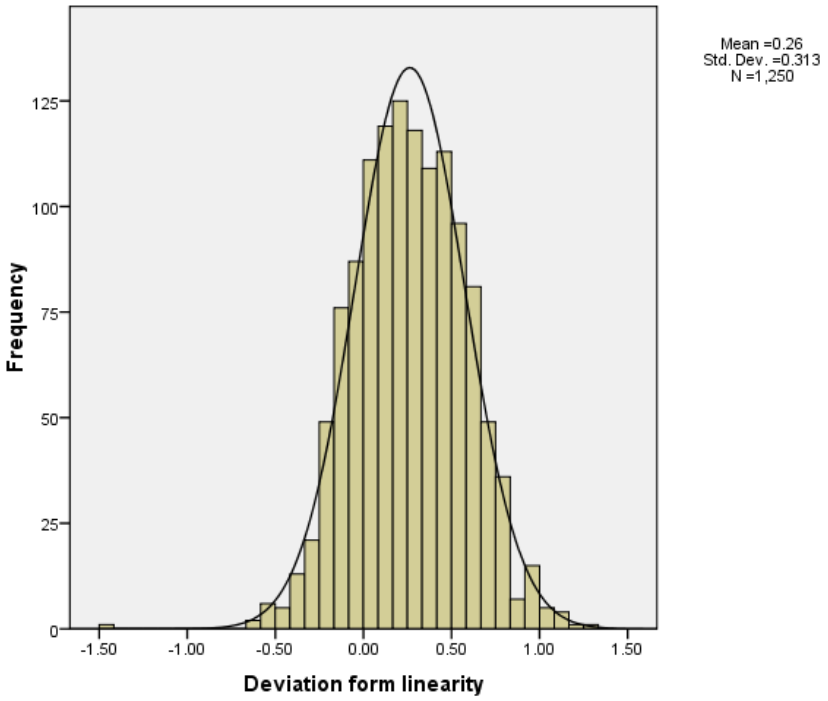

Figure 43. Histogram of deviations from linearity for 500˚C at 3˚C/s with 5 s hold-time

Figure 41 to 43 is for TL done up to 500 ˚C at 3 ˚C/s with 5 second hold-time. The linearity of stimulation for this is shown in figure 41. Figure 42 shows the error in this stimulation which is also shown using a histogram in figure 43. The mean error was 0.26 and the standard deviation was 0.313.

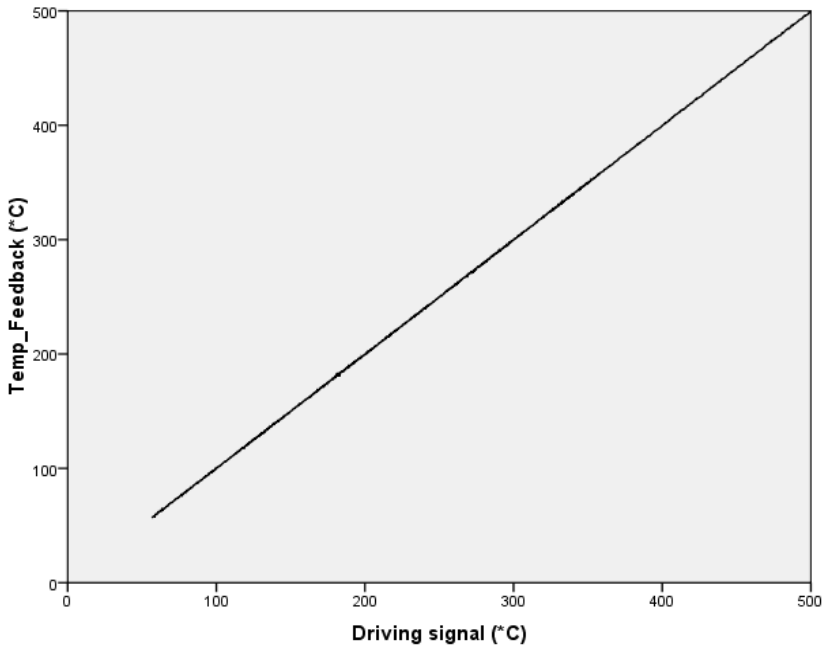

Figure 44. Linearity in thermal stimulation for TL done up to 500 ˚C at 2 ˚C/s with 5 s hold-time

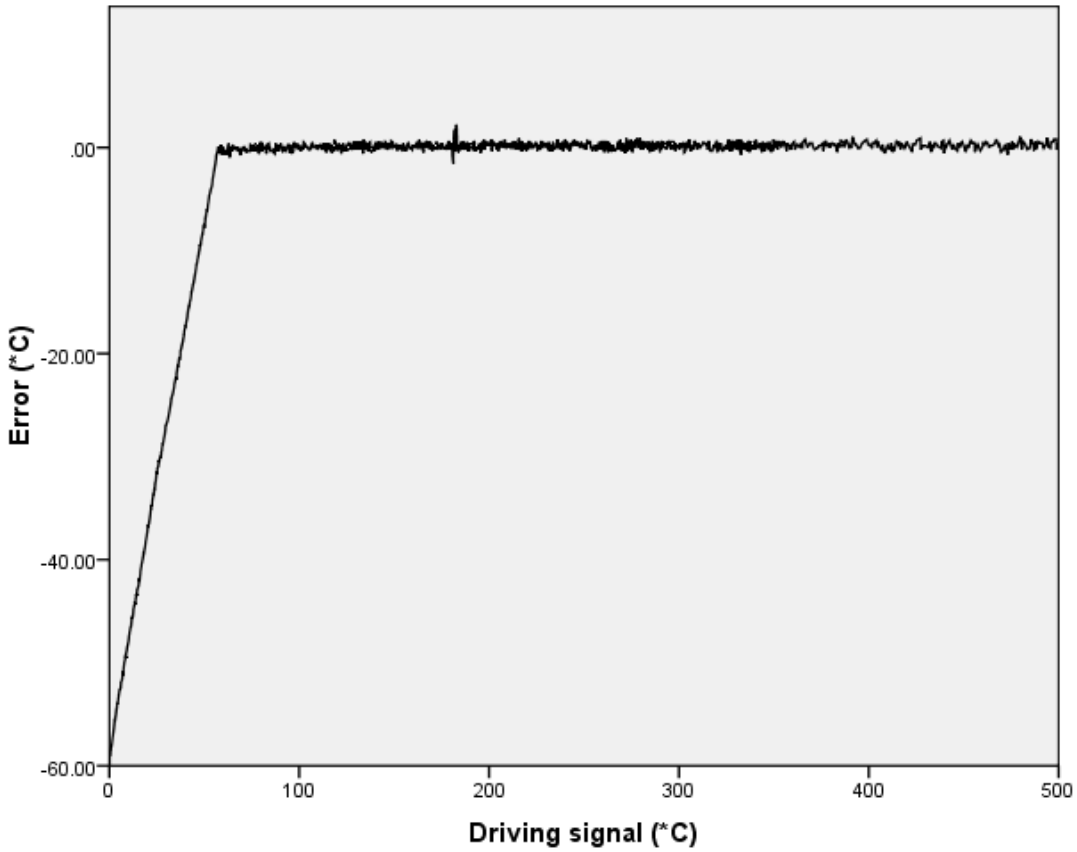

Figure 45. Error in thermal stimulation for TL done up to 500 ˚C at 2 ˚C/s with 5 s hold-time

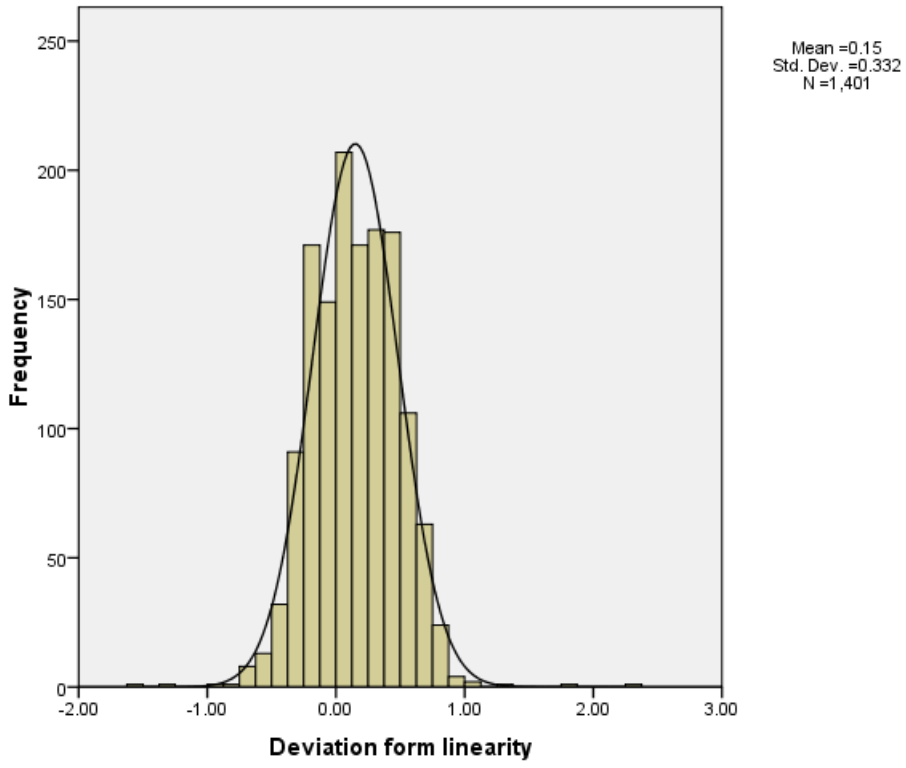

Figure 46. Histogram of deviations from linearity for 500˚C at 2 ˚C/s with 5 s hold-time

Figure 44 to 46 is for TL done up to 500 ˚C at 2 ˚C/s with 5 second hold-time. The linearity of stimulation for this is shown in figure 44. Figure 45 shows the error in this stimulation which is also shown using a histogram in figure 46. The mean error was 0.15 and the standard deviation was 0.332.

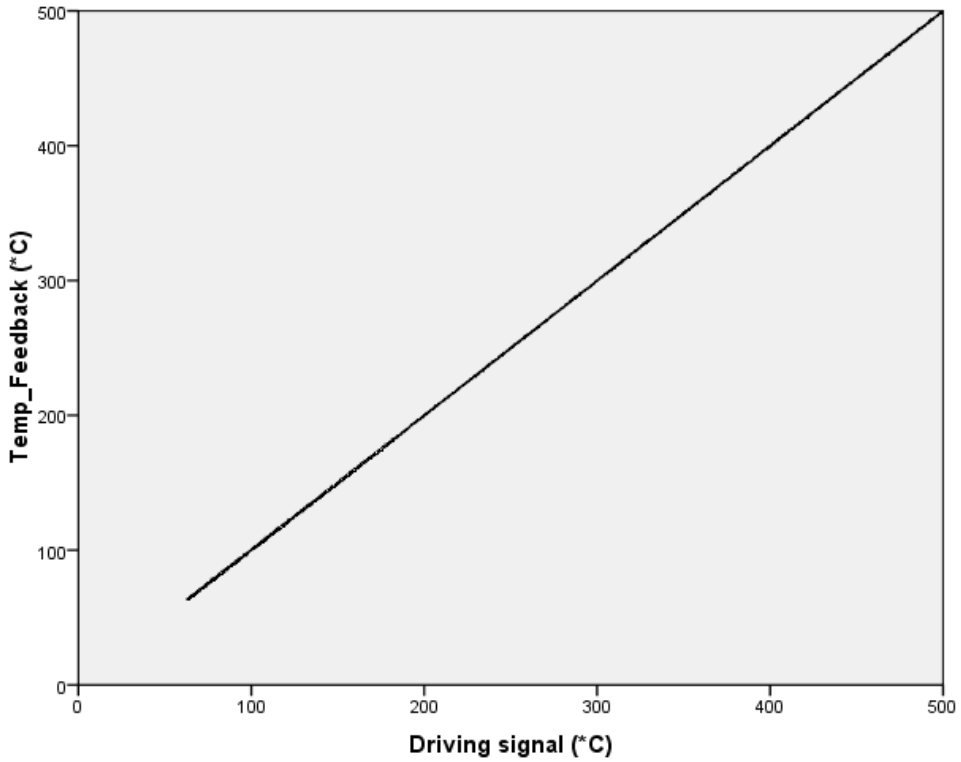

Figure 47. Linearity in thermal stimulation for TL done up to 500 ˚C at 1 ˚C/s with 7 s hold-time

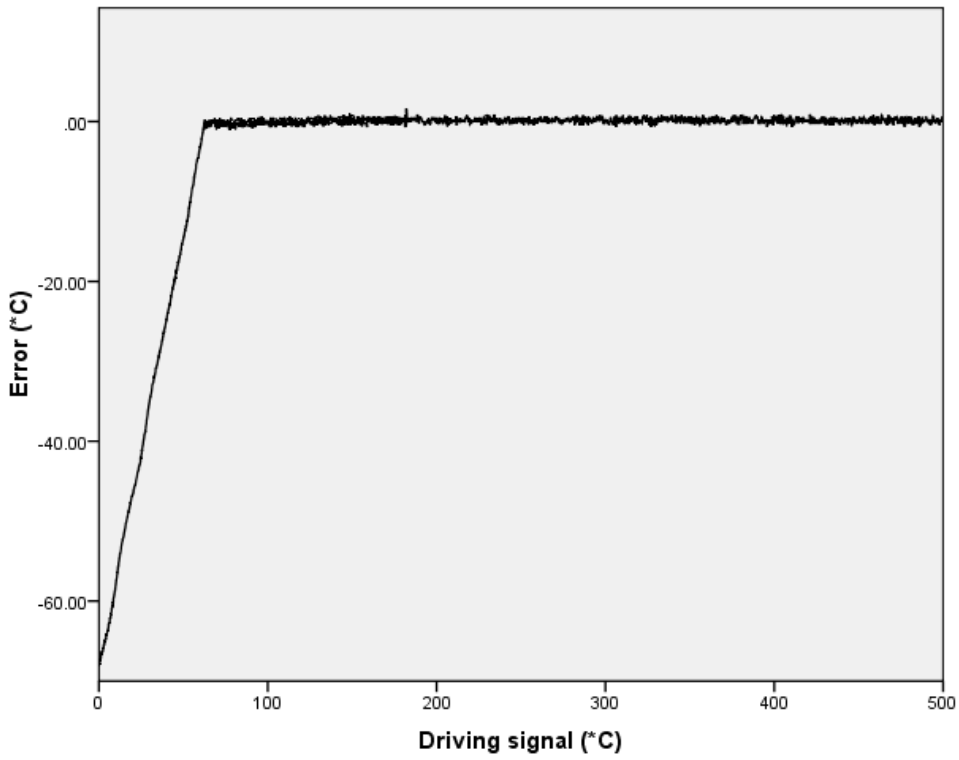

Figure 48. Error in thermal stimulation for TL done up to 500 ˚C at 1 ˚C/s with 7 s hold-time

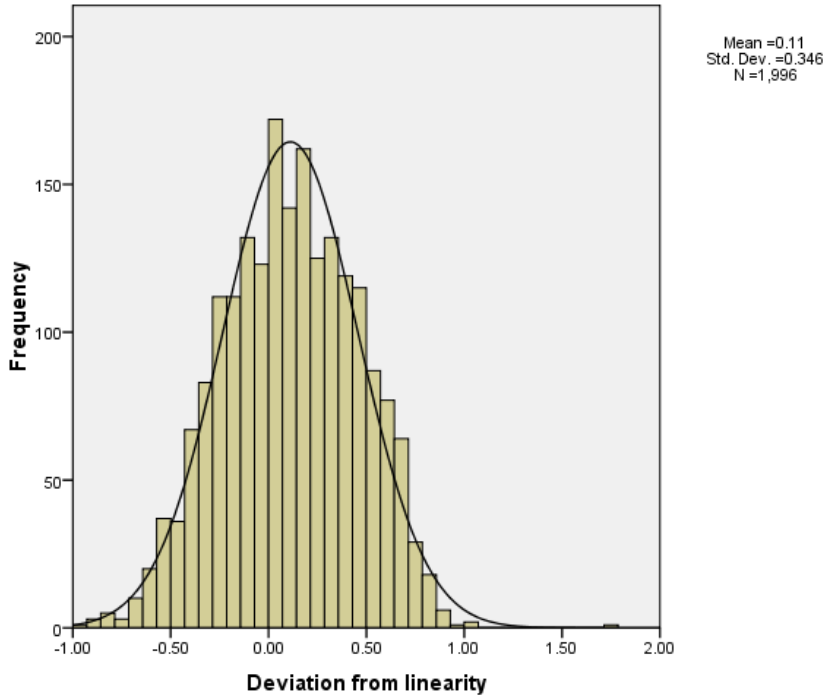

Figure 49. Histogram of deviations from linearity for 500 ˚C at 1 ˚C/s with 7 s hold-time

Figure 47 to 49 is for TL done up to 500 ˚C at 1 ˚C/s with 7 second hold-time. The linearity of stimulation for this is shown in figure 47. Figure 48 shows the error in this stimulation which is also shown using a histogram in figure 49. The mean error was 0.11 and the standard deviation was 0.346

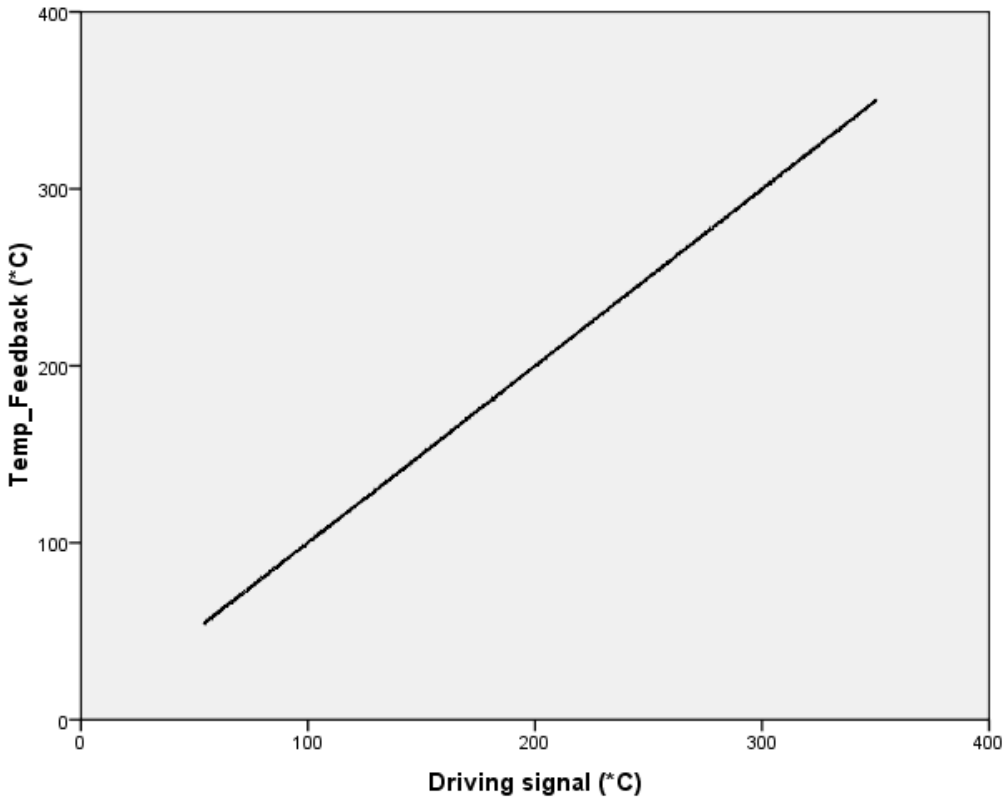

Figure 50. Linearity in thermal stimulation for TL done up to 350 ˚C at 0.5 ˚C/s

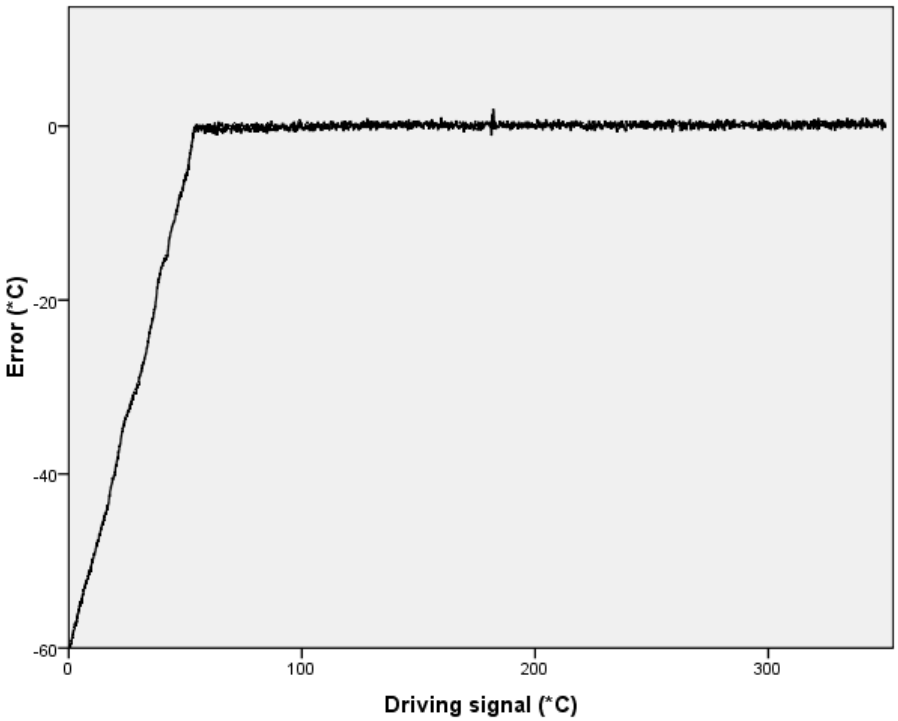

Figure 51. Error in thermal stimulation for TL done up to 350 ˚C at 0.5 ˚C/s

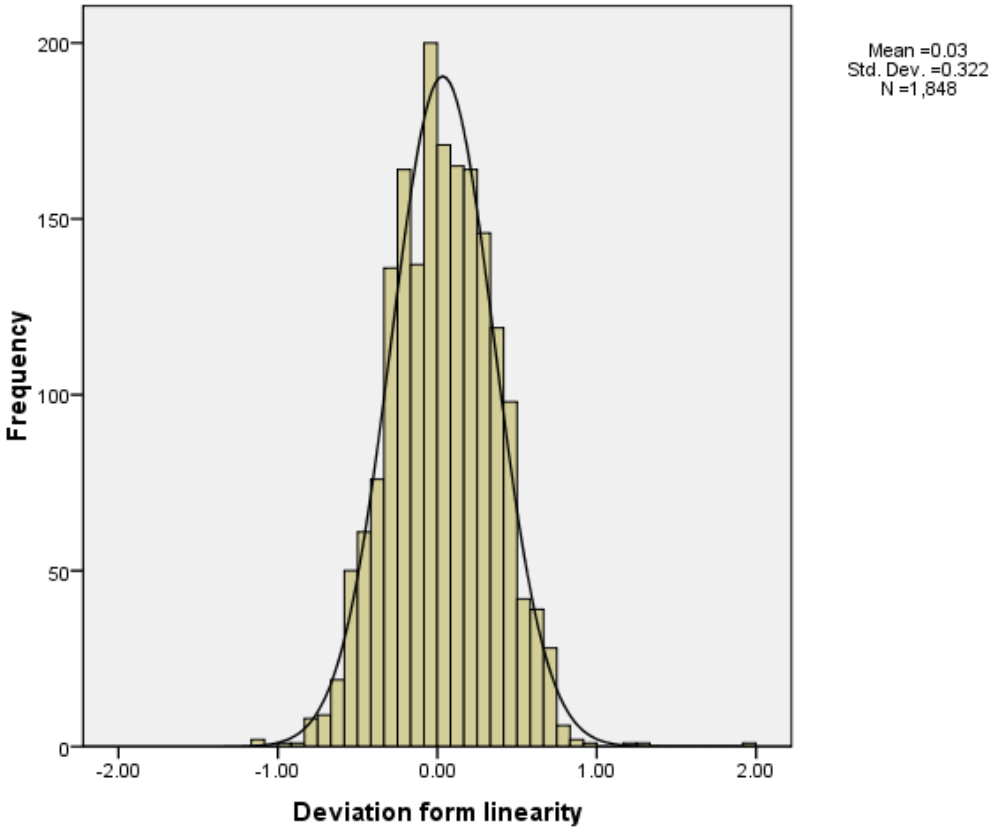

Figure 52. Histogram of deviations from linearity for 350˚C at 0.5 ˚C/s

Figure 50 to 52 is for TL done up to 350 ˚C at 0.5 ˚C/s. The linearity of stimulation for this is shown in figure 50. Figure 51 shows the error in this stimulation which is also shown using a histogram in figure 52. The mean error was 0.03 and the standard deviation was 0.322

Figure 53 to 67 shows the error in the optical stimulation, linearity, histogram of deviation from linearity when OSL was done up to 100% intensity with the rates 0.1, 0.5, 1.0, 1.5, and 2 %/s and with 15 seconds hold-time. Figure 68 shows the error when CW OSL was done at 70% for 30 s. Figure 69 shows the histogram of deviation for the same case.

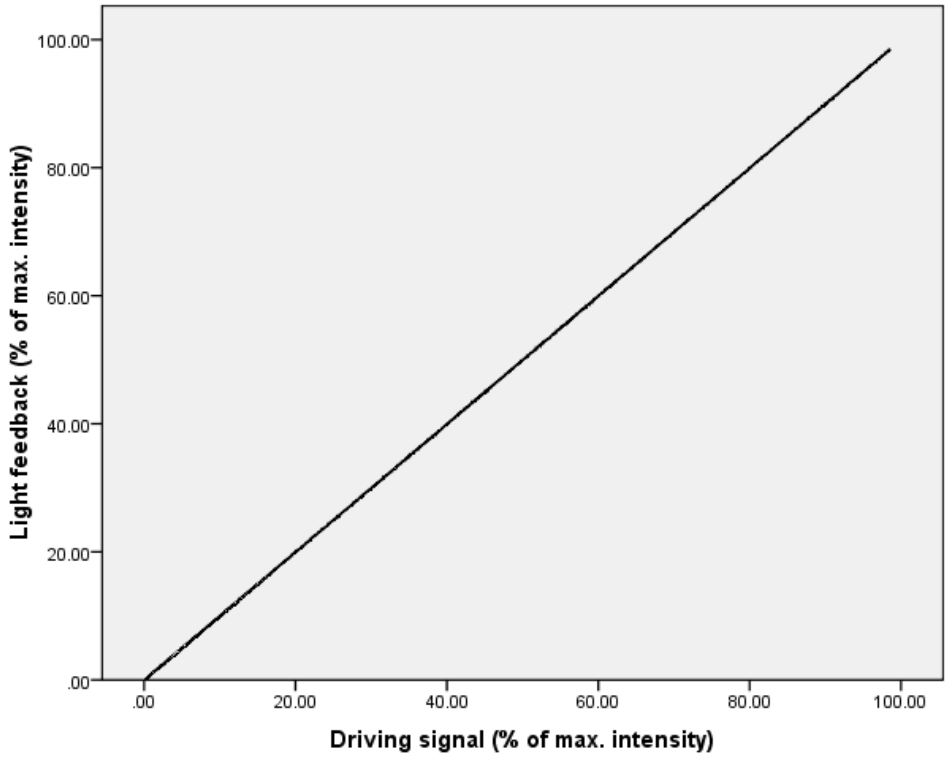

Figure 53. Linearity in optical stimulation for ramping upto 100% intensity at 0.1 %/s rate with 15 s hold-time

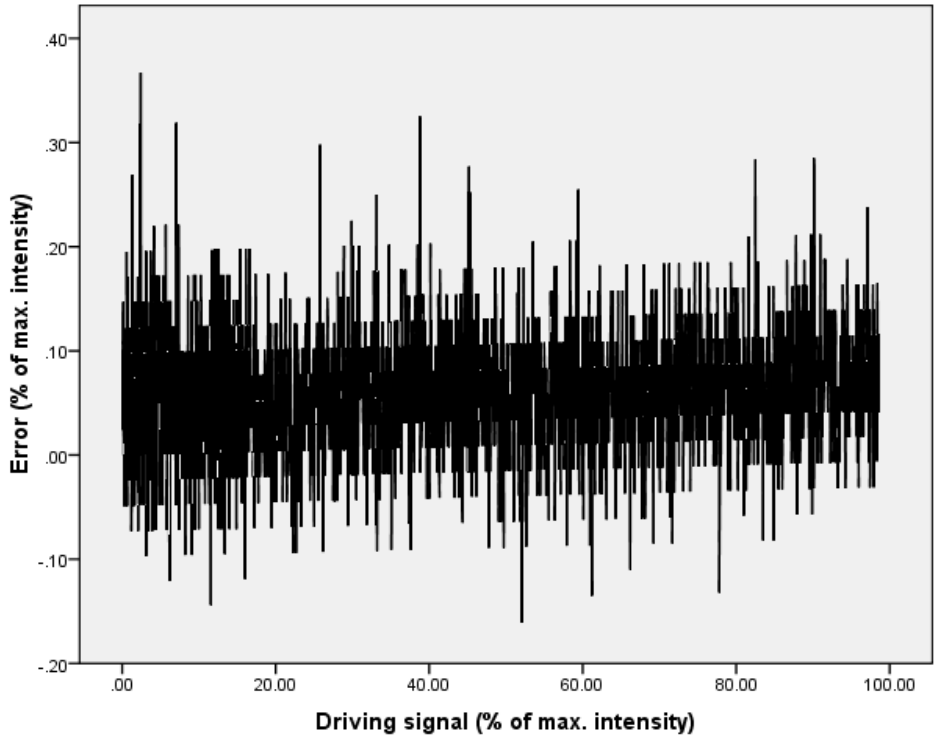

Figure 54. Error in optical stimulation for OSL done up to 100% at 0.1 %/s with 15 s hold-time

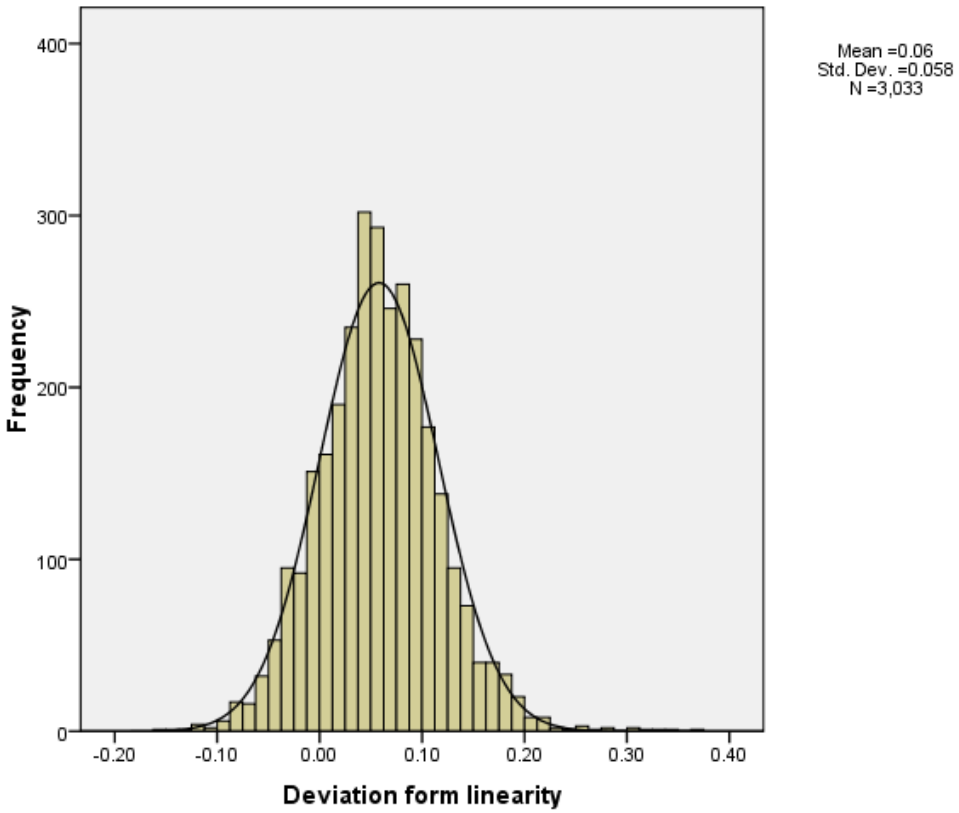

Figure 55. Histogram for 100% at 0.1 %/s with 15 s hold-time

Figure 53 to 55 is for OSL done up to 100% of its maximum intensity at 0.1 %/s with 15 second hold-time. The linearity of stimulation for this is shown in figure 53. Figure 54 shows the error in this stimulation which is also shown using a histogram in figure 55. The mean error was 0.06 and the standard deviation was 0.058.

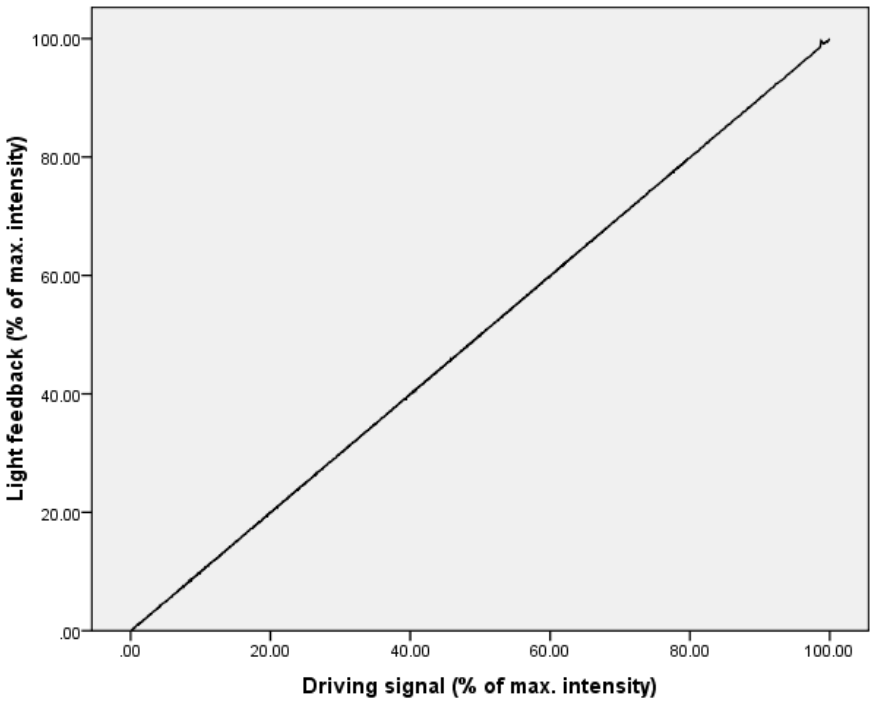

Figure 56. Linearity in optical stimulation for ramping upto 100% intensity at 0.5 %/s rate with 15 s hold-time

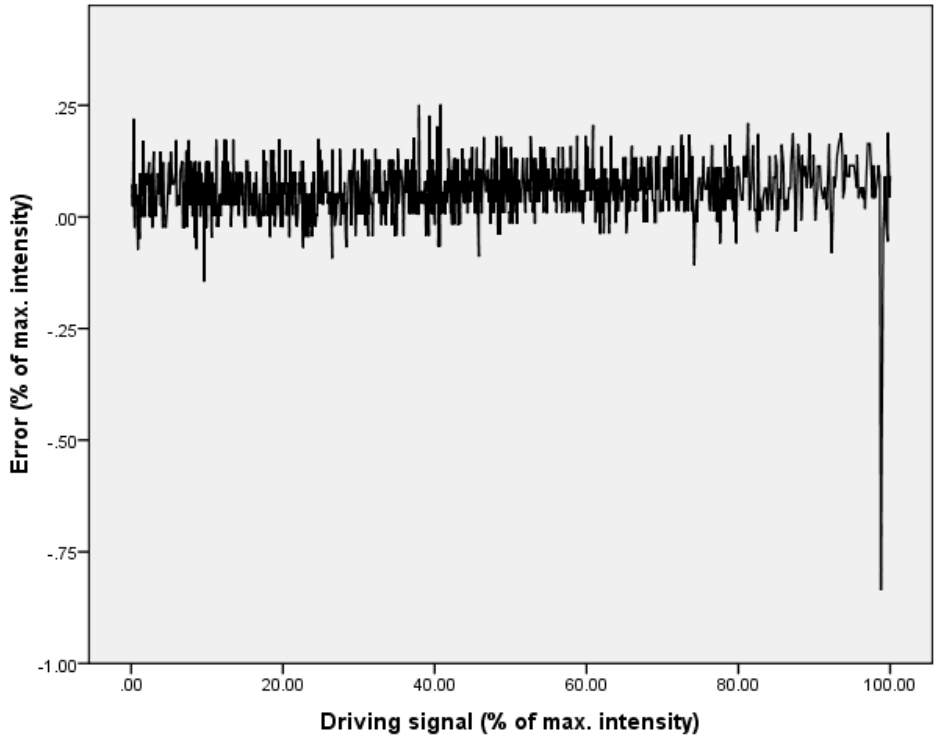

Figure 57. Error in optical stimulation for OSL done up to 100% at 0.5 %/s with 15 s hold-time

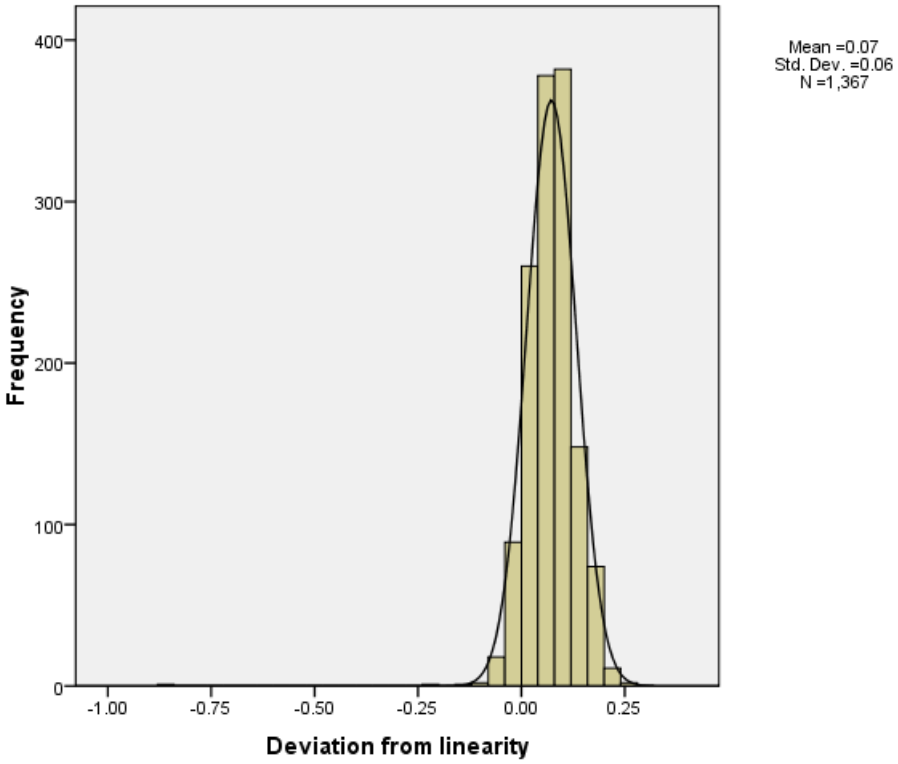

Figure 58. Histogram for 100% at 0.5 %/s with 15 s hold-time

Figure 56 to 58 is for OSL done up to 100% of its maximum intensity at 0.5 %/s with 15 second hold-time. The linearity of stimulation for this is shown in figure 56. Figure 57 shows the error in this stimulation which is also shown using a histogram in figure 58. The mean error was 0.07 and the standard deviation was 0.06.

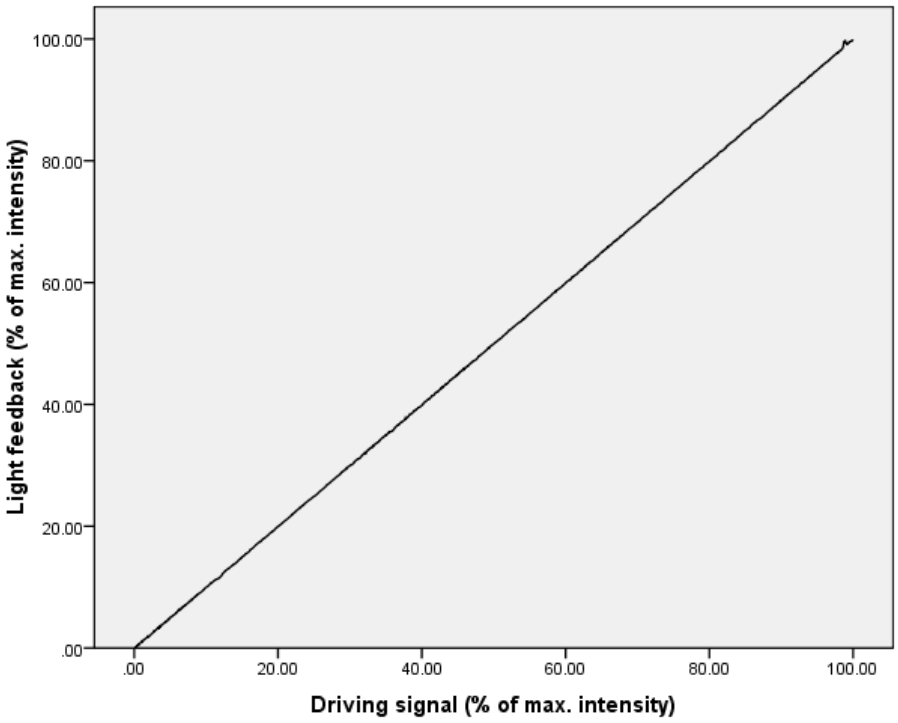

Figure 59. Linearity in optical stimulation for ramping upto 100% intensity at 1 %/s rate with 15 s hold-time

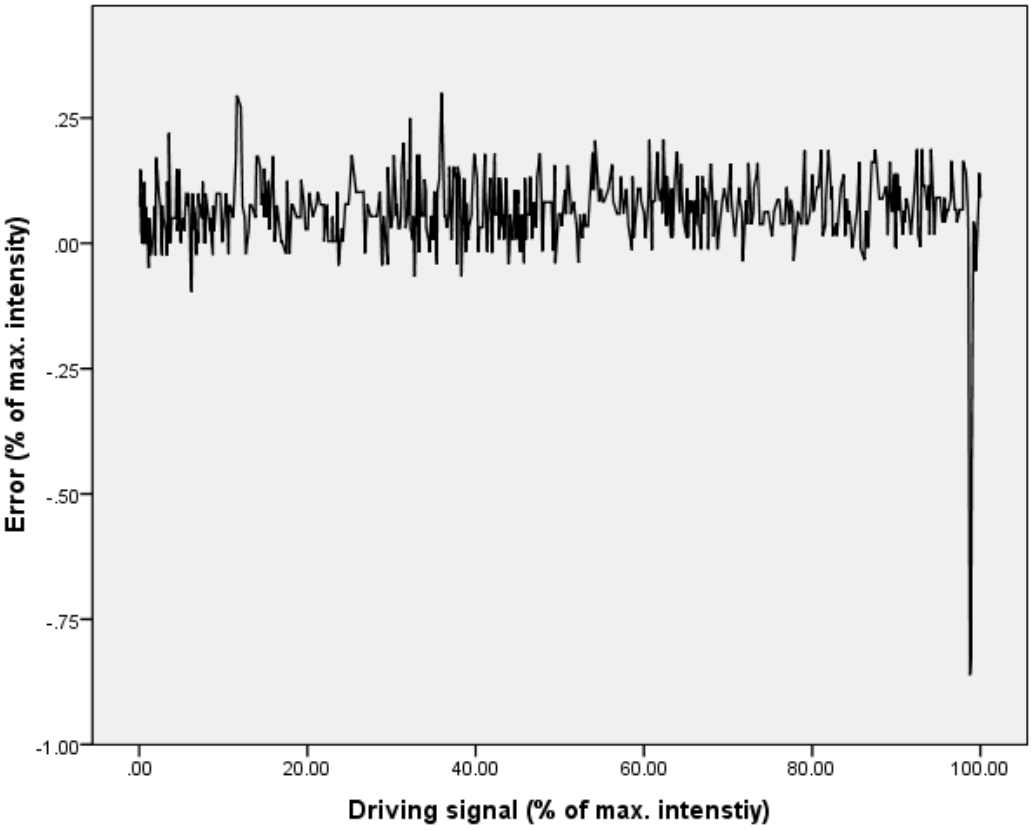

Figure 60. Error in optical stimulation for OSL done up to 100% at 1 %/s with 15 s hold-time

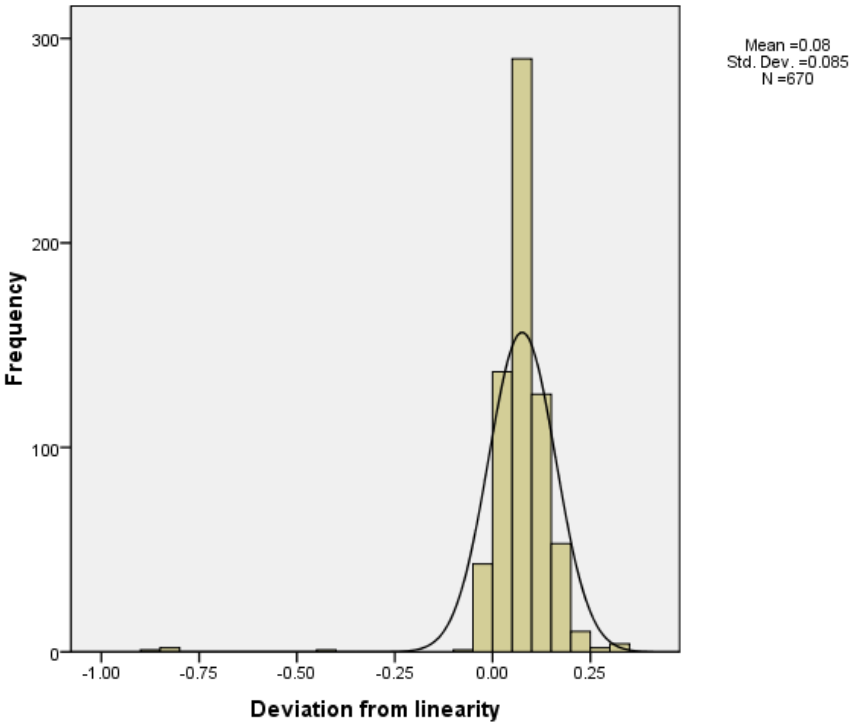

Figure 61. Histogram for 100% at 1 %/s with 15 s hold-time

Figure 59 to 61 is for OSL done up to 100% of its maximum intensity at 1 %/s with 15 second hold-time. The linearity of stimulation for this is shown in figure 59. Figure 60 shows the error in this stimulation which is also shown using a histogram in figure 61. The mean error was 0.08 and the standard deviation was 0.085.

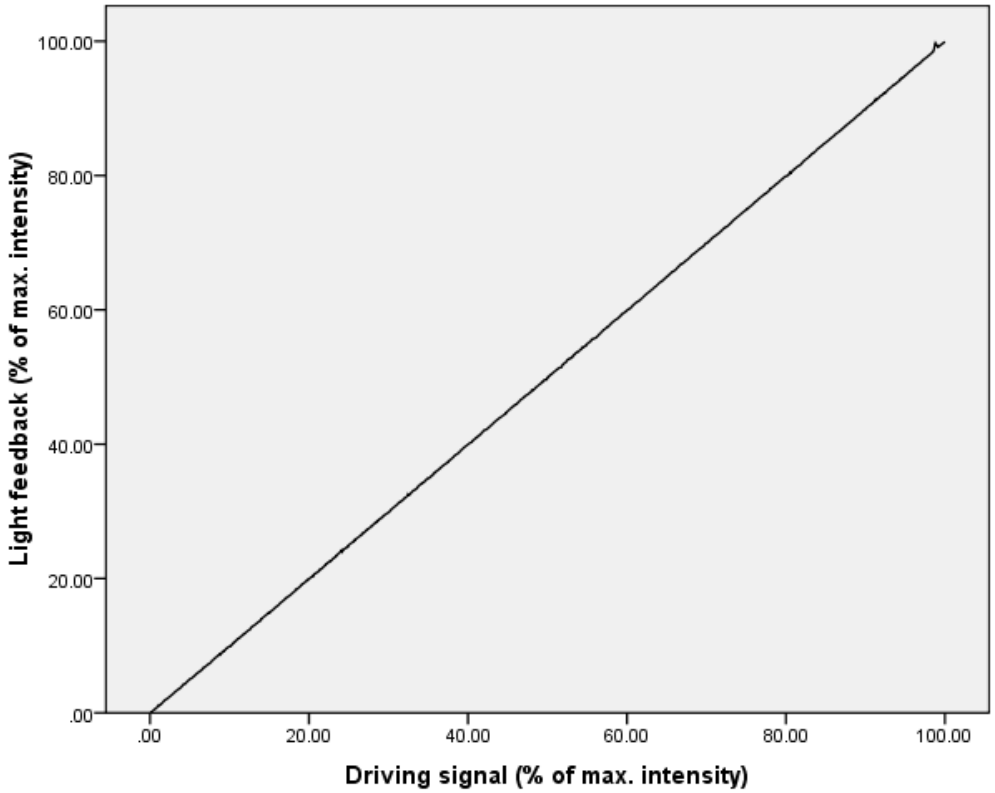

Figure 62. Linearity in optical stimulation for ramping upto 100% intensity at 1.5 %/s rate with 15 s hold-time

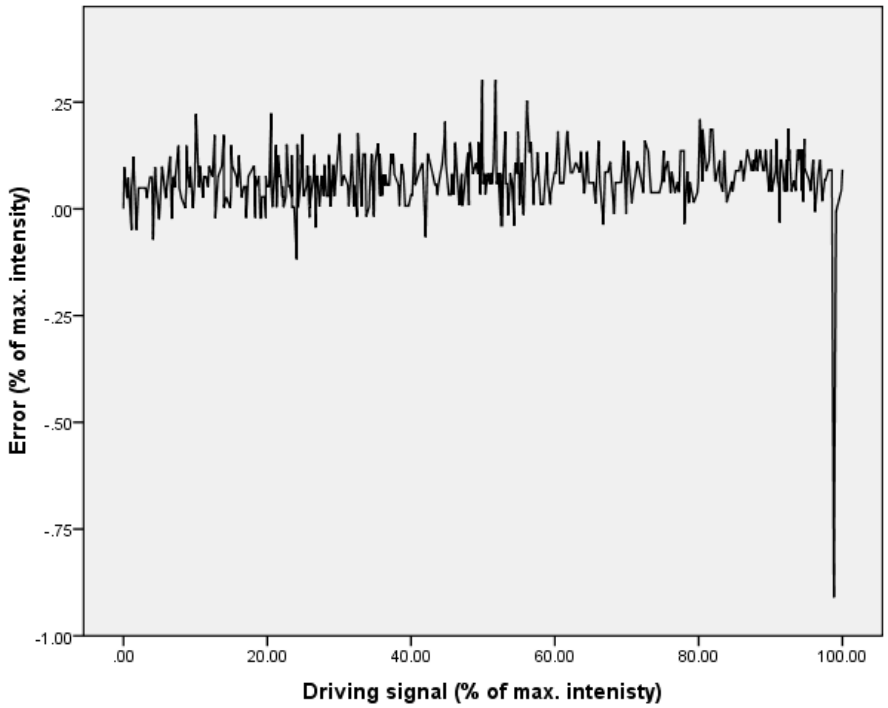

Figure 63. Error in optical stimulation for OSL done up to 100% at 1.5 %/s with 15 s hold-time

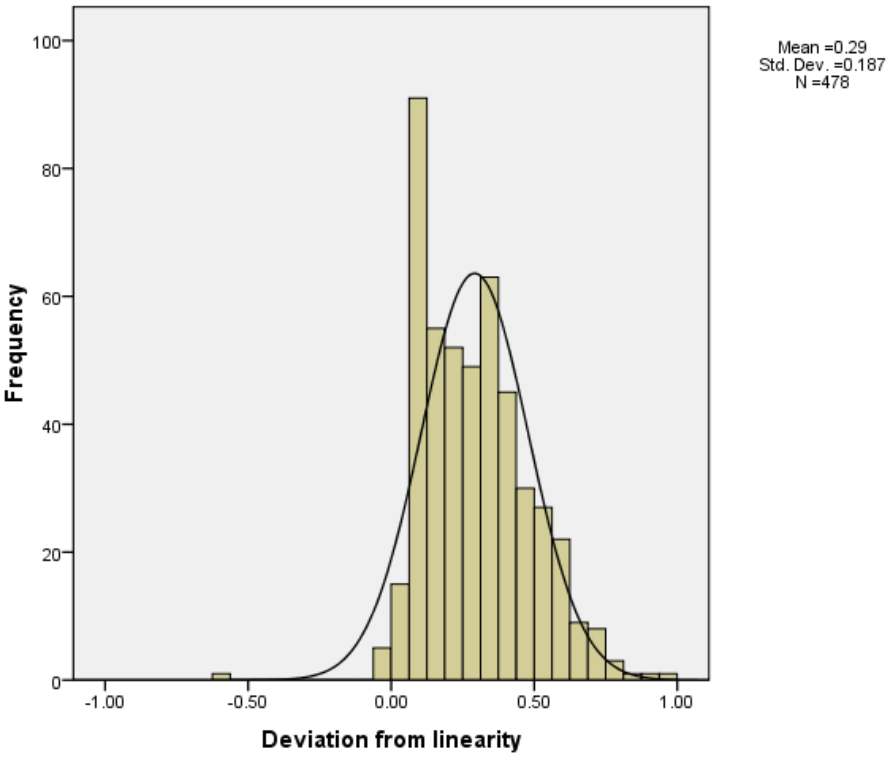

Figure 64. Histogram for 100% at 1.5 %/s with 15 s hold-time

Figure 62 to 64 is for OSL done up to 100% of its maximum intensity at 1.5 %/s with 15 second hold-time. The linearity of stimulation for this is shown in figure 62. Figure 63 shows the error in this stimulation which is also shown using a histogram in figure 64. The mean error was 0.29 and the standard deviation was 0.187.

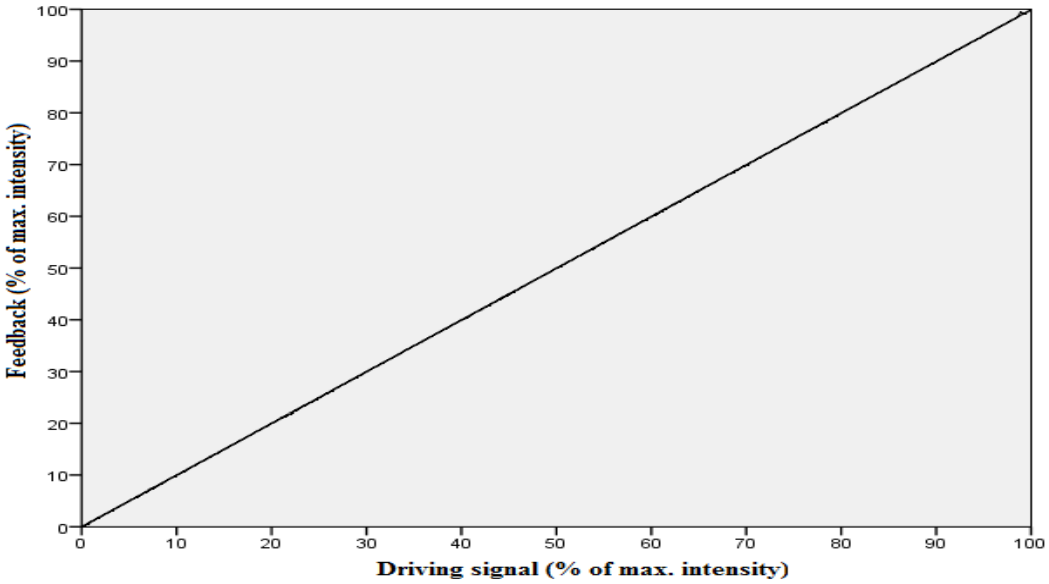

Figure 65. Linearity in optical stimulation for ramping upto 100% intensity at 2 %/s rate with 15 s hold-time

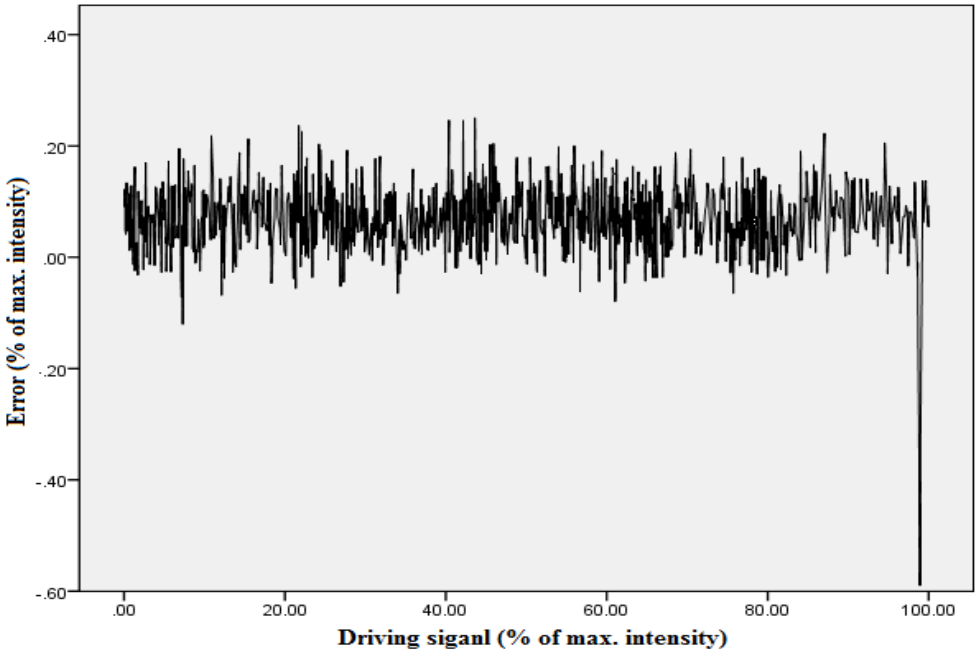

Figure 66. Error in optical stimulation for OSL done up to 100% at 2 %/s with 15 s hold-time

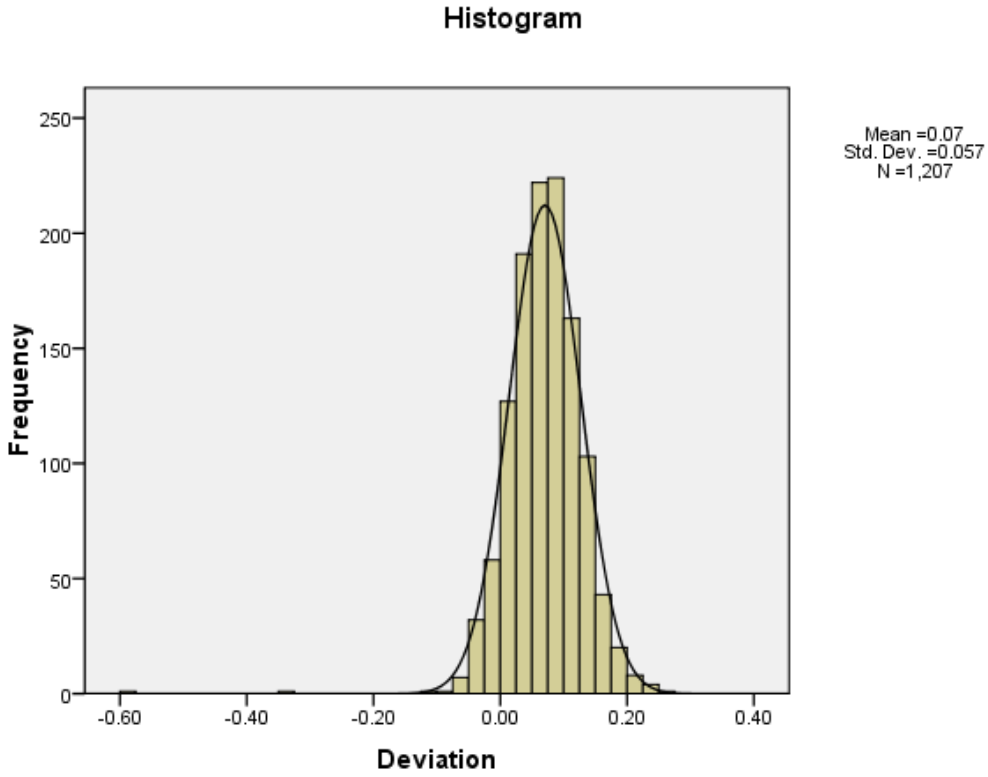

Figure 67. Histogram for 100% at 2 %/s with 15 s hold-time

Figure 65 to 67 is for OSL done up to 100% of its maximum intensity at 2 %/s with 15 second hold-time. The linearity of stimulation for this is shown in figure 65. Figure 66 shows the error in this stimulation which is also shown using a histogram in figure 67. The mean error was 0.07 and the standard deviation was 0.057.

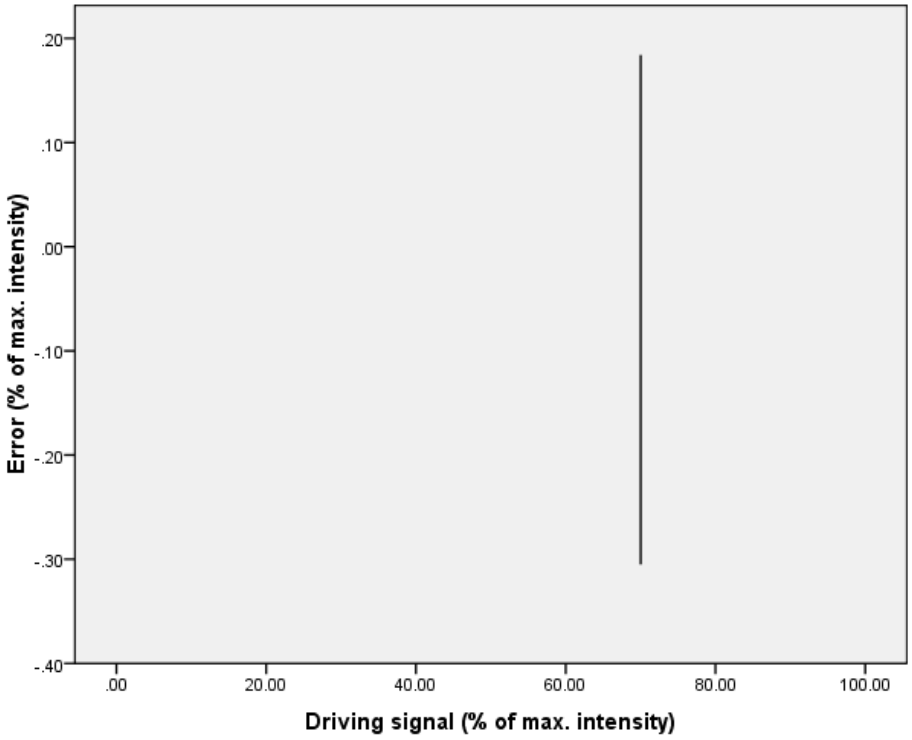

Figure 68. Error in optical stimulation for CW-OSL (step profile) at 70% intensity for 30 s

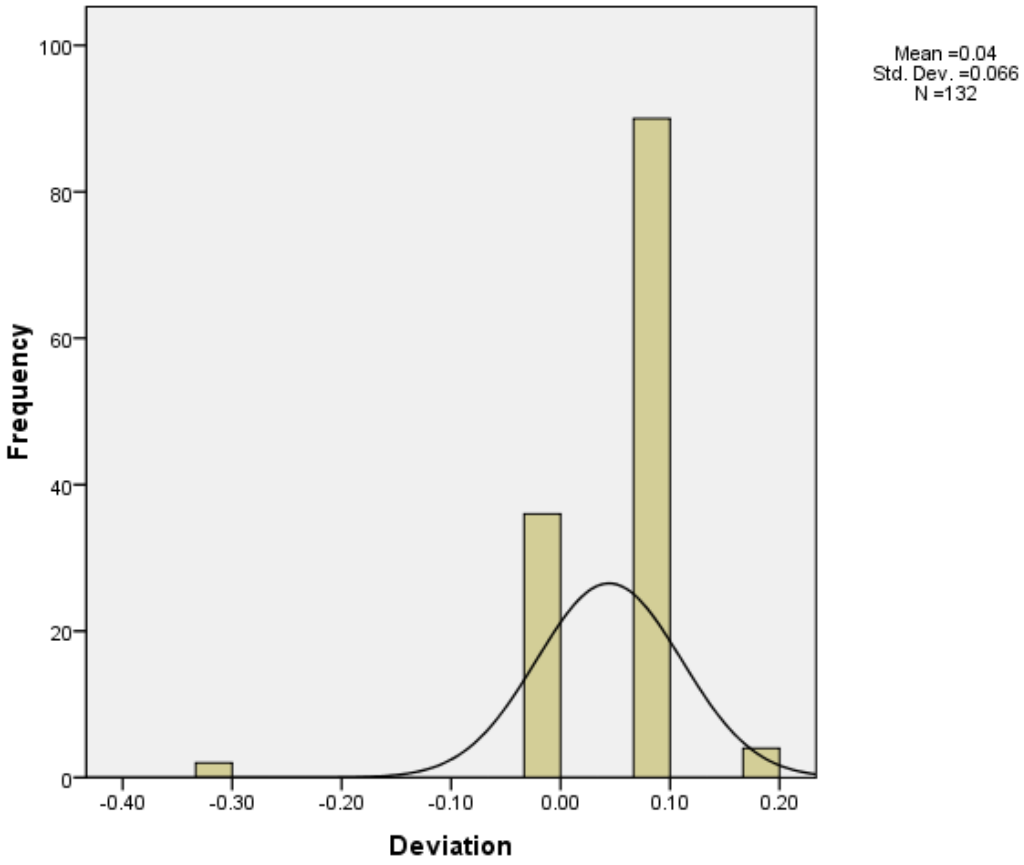

Figure 69. Histogram for optical stimulation for CW-OSL (step profile) at 70% intensity for 30s

Figure 68 and 69 is for OSL done up to 70% of its maximum intensity in the CW-OSL mode with 30 second hold-time. Figure 68 shows the error in this stimulation which is also shown using a histogram in figure 69. Here the mean error was 0.04 and the standard deviation was 0.066.

3.12 Dose recovery tests

For the dose recovery tests the regenerative method was used. An EMCCD based spatially resolved luminescence arrangement and the associated software developed in Matlab was used. The system besides recording the photon counts also maintains the spatial resolution. The data is acquired in the form of images which are then used after image processing to derive the required dose information. Dose recovery tests were done for quartz and feldspar and the results for most of the grains were found to be within ± 10% of the real value which is generally considered to be the acceptable range of error. The luminescence from quartz is shown in figure 70 while that from feldspar is shown in figure 71.

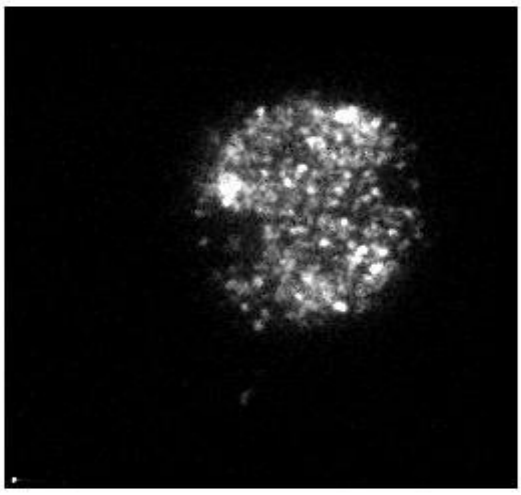

Figure 70. Luminescence from quartz

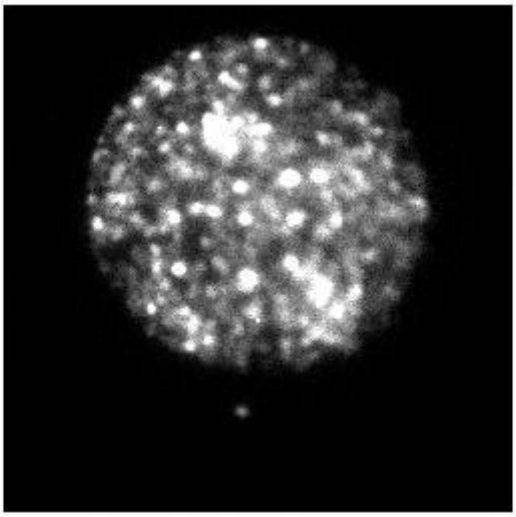

Figure 71. Luminescence from Feldspar

3.12.1 Dose recovery tests with Daybreak, Risoe, and FPGA-EMCCD system using CaF_2

Dose recovery test was done on Daybreak 2200 model TL/OSL reader. Table 1 shows the doses given and its corresponding counts. A graph of counts verses dose gives a linear line from which the unknown dose is calculated as shown in figure 72.

Dose (Gy)	Counts
80	43450222
100	53093352
120	65821668
100	54965844

Table 1. Doses given by the Daybreak system and its corresponding counts

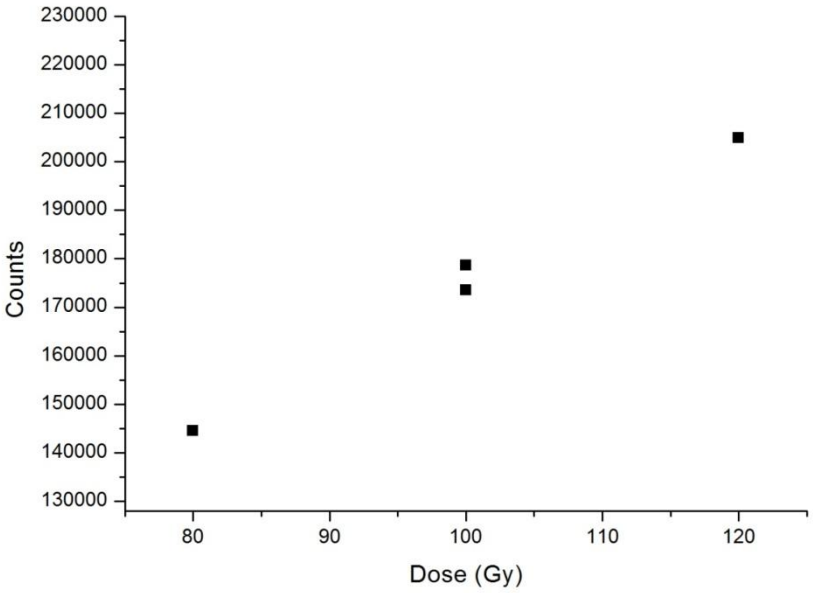

Figure 72. Counts versus dose graph for the Daybreak system

Table 2 shows the doses and its corresponding counts for Risoe TL/OSL DA-20 system. Figure 73 gives the counts verses doses graph from which the unknown dose is calculated.

Dose (Gy)	Counts
80	69791628
100	89224705
120	1.08E+08
100	86319397

Table 2. Doses given by the Risoe system and its corresponding counts

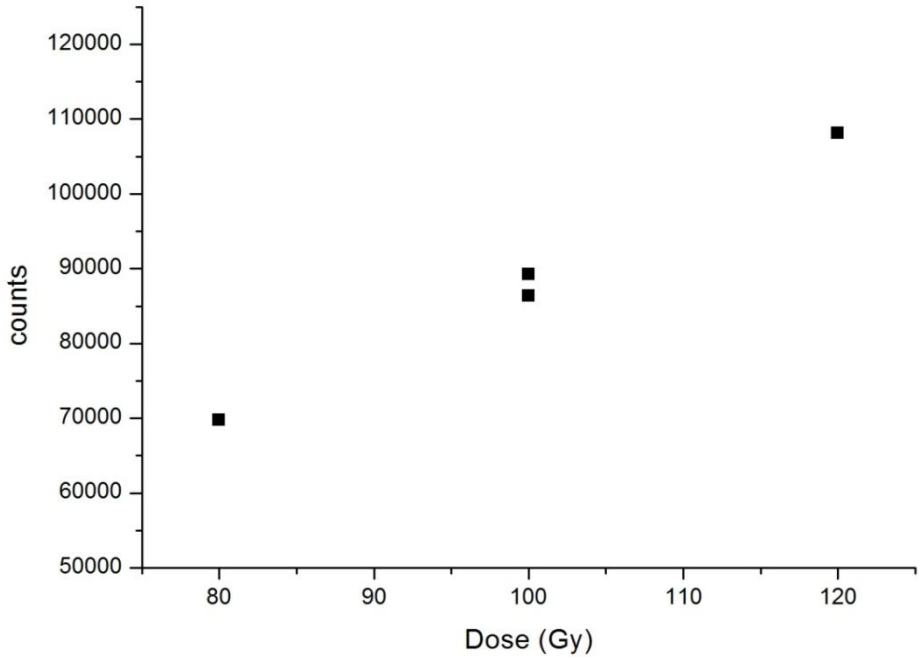

Figure 73. Counts versus dose graph for the Risoe system

In the FPGA-EMCCD system dose recovery test was done using the method described above. The doses given were 70, 80, 100 Gy and one more dose of 80 Gy which was treated as unknown dose to be found out. For each of the given dose a corresponding image is obtained. From the analysis of these images the unknown dose is found out. The brightness of the images is directly proportional to the doses received by them. Doses can be found at different parts of the image. Figure 74 shows the luminescence obtained for one of the doses given.

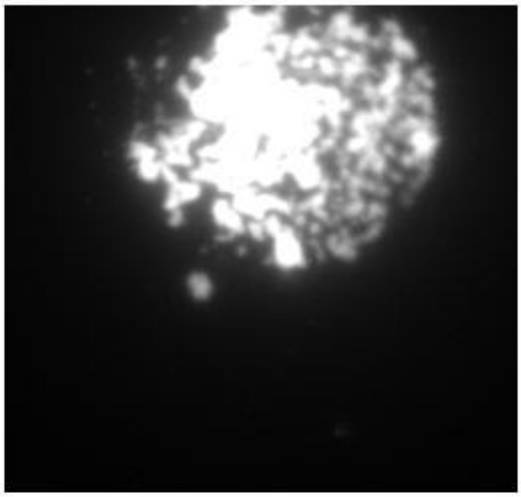

Figure 74. Luminescence from Calcium Fluoride

Doses calculated at different parts of the image are 81.12 Gy, 71.10 Gy, 85.47 Gy, 89.55 Gy, 71.16 Gy and 80.23 Gy. As is seen all the recovered doses are within 10 % of error, which is generally an acceptable range of error, for the case of Daybreak 2200, Riso TL/OSL-DA and the EMCCD-FPGA system.

3.13 Conclusion

An FPGA based system with an EMCCD camera for spatial imaging has been developed for the thermal and optical stimulation of samples. Luminescence signals emitted by feldspars, quartz, and CaF_2 were detected by it. The system has been tested and its performance has been presented in this chapter. In the case of TL, it was found that the average standard deviation from linearity is 0.36 ˚C, while the average error is less than 0.35 ˚C. At the hold-time the average variation in temperature is 0.18 ˚C. In the case of OSL, it was found that the average of the standard deviation from linearity of all the readings is 0.068%, while the average error was <0.1%. At the hold-time the average variation in light intensity is 0.065%. The system gives more flexibility for the luminescence researcher to explore the realm of spatial luminescence with a more versatile instrument.

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