Chapter 3

Reference Tracking in Electric Spring and Phase Locked Loop Structures

3.1 Introduction

A phase-locked loop (PLL) is a system being used to identify the phase and frequency of a signal. Appleton proposed the concept of basic PLL structure in 1923, for the application of radio signal synchronization, and the same can be seen from Fig:3.1. With the emergence of new devices and technologies that works with the power grid, the interest of power system engineers in PLL is constantly increasing.

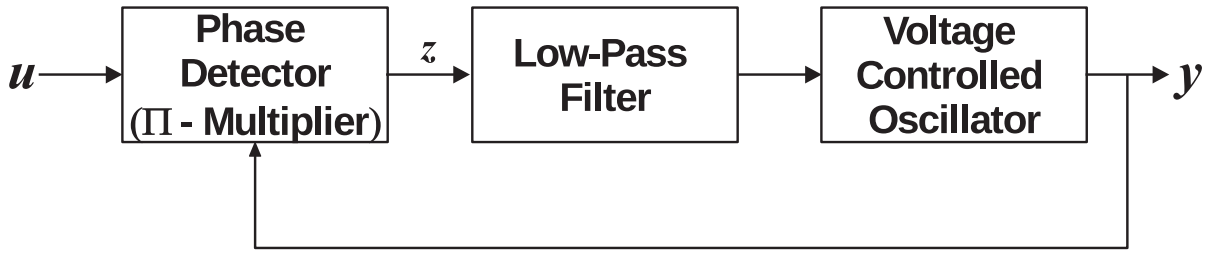

Figure 3.1: Standar Structure of a Phase-Locked-Loop (PLL).

Here, the phase detector produces a signal proportional to the phase difference between the reference signal and the feedback signal using a multiplier. This signal upon filtration, generally being executed using PI controller, drives the Voltage Controlled Oscillator

(VCO) to generate the output, following the referenced input signal.

3.2 Application of PLL in Power System

Information of Phase angle, Frequency, Magnitude, and Rate-of-change-of-frequency ($ROCF$) is of prime importance for the signals associated with power frequency applications. These parameter measuring systems must possess enough robustness to get immunity against the repercussions related to frequency variations, distortion, and noise. The application of PLL for the frequency and phase estimation of power electronic devices and converters, which are inherently non-linear, asks for non-linear system analysis.

Following is the list of few potential power frequency applications that encompass the PLL structure for the measurement of phase, amplitude, and frequency measurement:

- Proliferation and use of power electronic converters have considerably increased with the advent of restructured power systems, due to the interconnection and integration of distributed generators and storage units, into the grid. Further, it can be elaborated as:
  - Renewable energy sources such as solar and wind, integrated with the distribution grid, have emerged as nonpolluting sources of energy due to greater awareness and environmental concern. Grid-tied inverters are used in conjunction with these distributed generators.
  - FACTS and Custom power devices are used to regulate active and reactive power, bringing stability to the grid.
  - UPS is used to ensure the quality and well-regulated supply to critical loads.
  - Active Power Filters are used to ensure the system's power quality amidst the presence of non-linear loads.
- The micro-grid concept encompasses a mechanism that optimally and efficiently harnesses electrical energy from more than two sources, either in the stand-alone mode called islanded mode or grid integrated mode.
- The digitalization of the power system has brought about the smart grid concept by tapping the potential of advanced communication and computer technology for enhancing and improving the reliability and performance of the power system.

- Phasor Measurement Units (PMUs) are the sophisticated monitoring device dispersed throughout the grid for wide-area measurement (WAM), at critical locations in the power system, being used for power system's protection, stability, and planning.

This basic PLL structure mentioned in Section: 3.1 does not work well with the power frequency signals for the following reasons:

1. Non-sinusoidal wave-shape of the power signal, due to distortions in the form of harmonics, bias, transient, disturbances, notches, and noise. The prime cause of distortion is the presence of nonlinearities in the system components.

2. The power system is operating with a range-bound frequency variation ($\pm 1\%$), and not at an exact frequency, ω_n, due to the demand-supply mismatch.

Non-robust performance of basic PLL structure and a plethora of applications has encouraged the power system engineers to develop some new and improved PLL structures. The researchers have suggested numerous modifications for a typical power system application, and the same has been reviewed in the next section.

3.3 State-of-the-Art in Frequency and Phase Measurement for Power System Application

Numerous PLL structures have been suggested by the researchers for a typical power system application. Few of the frequency estimation methods have been presented here, along with their pros and cons as:

- Zero-cross detection-based techniques are the most widely used frequency estimating methods [79] [80], primarily being used for its simplicity and ease of implementation. Speed of operation and accuracy are a big concern with these methods when used for the frequency estimation of molested signals [81], and their output garbles under the influence of switching transients [80].

- Fourier Transforms (FT)/Fast Fourier Transforms (FFT)/Discrete Fourier Transforms (DFT) is being used for the spectrum analysis of a periodic signal. The

robustness of these methods, being employed in PLL [82], is extremely poor in handling the distorted signals [83] due to spectral leakage problem associated with the aperiodicity of the power signal outside the measurement window.

- Larger Window length [80][83] of measurement happens to be an issue with Phasor Rotation based algorithm [83], though it is possessing excellent robustness.
- Greater dependency on the model parameters debilitates the robustness of Kalman filter-based methods [84][85].
- Demodulation based methods [80] suffer the lack of sensitivity against noise.
- Adaptive neural network (ANN) based approaches [86][87] can perform well in dealing with the noisy and molested signals, requires significant training time, plenty of computational efforts, and not so easy to implement.
- Methods using Least Square Fit technique [88][89], can not deal with the system's singularity.
- Newton-type algorithm [90], Adaptive notch filters [91], and various signal processing methods have also been presented in the literature, as methods of Frequency and or Phase estimation.

3.4 Requirement of PLL Structures for the Application with Electric Spring

Electric Spring, being a custom power device employed at the consumer's premises for voltage regulation, is subjected to the following conditions:

- Changing voltage and current magnitude due to:
    1. Change in the connected load.
    2. Shortfall in the grid supply.
    3. Point of connection of the load, within a secondary distribution system, i.e., whether the load is connected close to the fag end of the feeder or away from it.

- Variation in the frequency, due to demand-supply mismatch.
- Presence of Harmonics in the voltage and current signals, due to non-linear loads connected at the point of common coupling (PCC)
- Transients, due to switching of larger loads within the feeder or in its vicinity.
- Phase angle variation, due to varieties of loads, operating at different power factor (pf).

These enumerated conditions lead to the changing phase and/or frequency in an electrical signal. The phase, so generated, acts as the angle of a sinusoidal reference, being used in conjunction with the $VSC's$ (ES) control.

The main task of PLL structure, being used with ES, is to extract the accurate phase of the grid voltage in the presence of harmonics and generate a perfect sinusoidal command reference of unity magnitude, being synchronized with the grid voltage. This signal is going to be acting as a reference signal, being tracked by the controller of the ES.

3.5 Experimental Test System for PLL

A PLL structure to be used with the ES system for phase and frequency detection must possess ample robustness to withstand the changes mentioned in Section: 3.4. Robustness of the adopted PLL structure, to be used in the control of ES, is desired to attain stability within the least possible time, in the presence of:

1. Step change in the voltage ($184V$ to $230V$ to $276V$)
2. Step change in the frequency ($47Hz$ to $50Hz$ to $53Hz$)
3. Phase Jumps ($0°$ to $45°$ to $90°$)
4. Inclusion of 3^{rd} and 5^{th} harmonics in the fundamental signal, with a corresponding $(1/3)^{rd}$ and $(1/5)^{th}$ of the magnitude of fundamental signal.

As shown in Fig: 3.2, an experimental setup has been established to test the performance of the PLL systems amidst changing voltage magnitude, frequency, and harmonics.

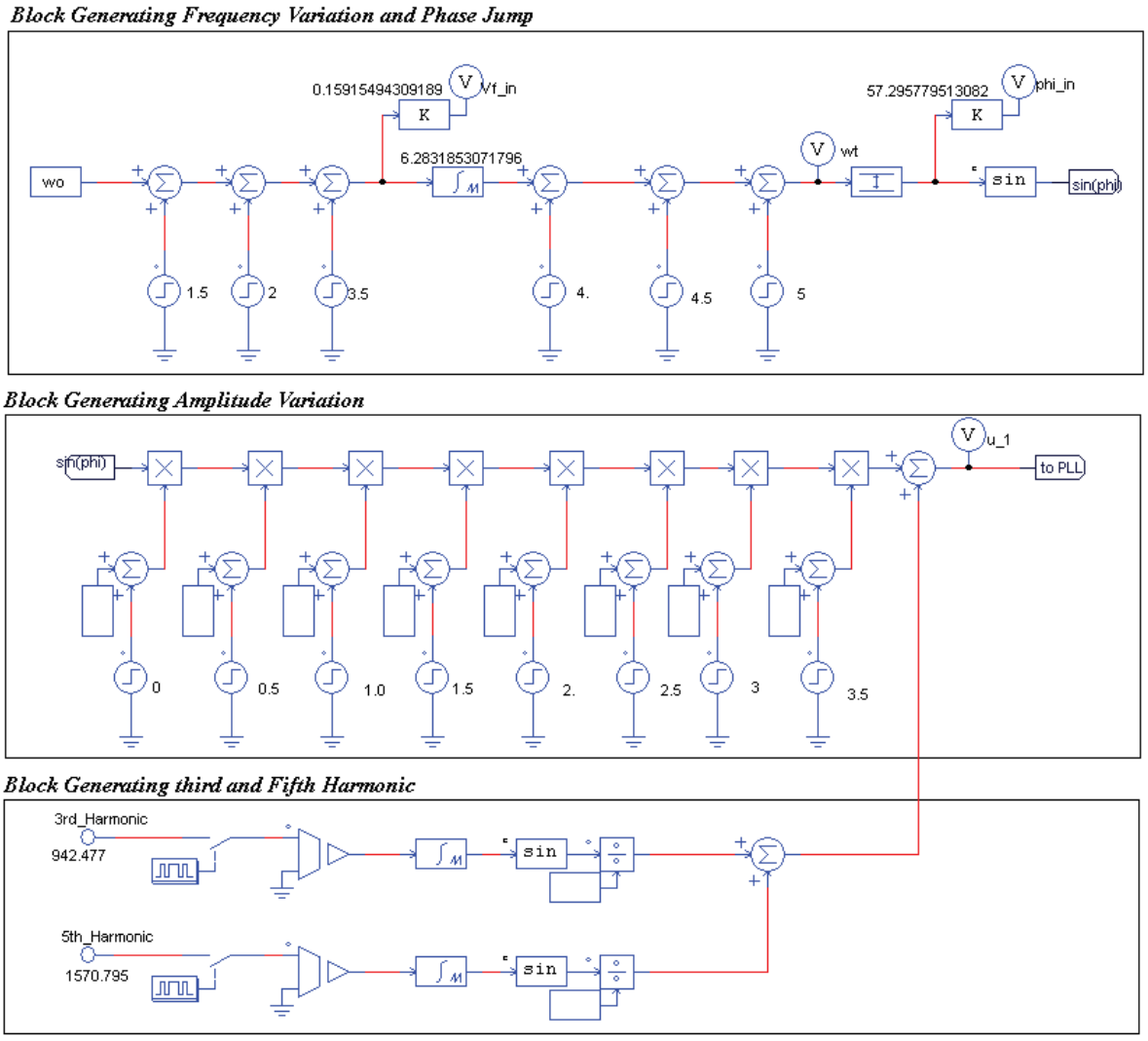

Figure 3.2: Experimental Test System, for Checking the Robustness of PLL.

3.6 PLL Structures for Electric Spring

Robustness of three different PLL systems, two of them using orthogonal signal generator through the use of (i) a-b-c to d-q transforms, and (ii) Second-Order-Generalized-Integrator ($SOGI$), and the third one implemented using (iii) Enhanced-PLL (E-PLL), have been tested using the test setup as presented in the upcoming sections.

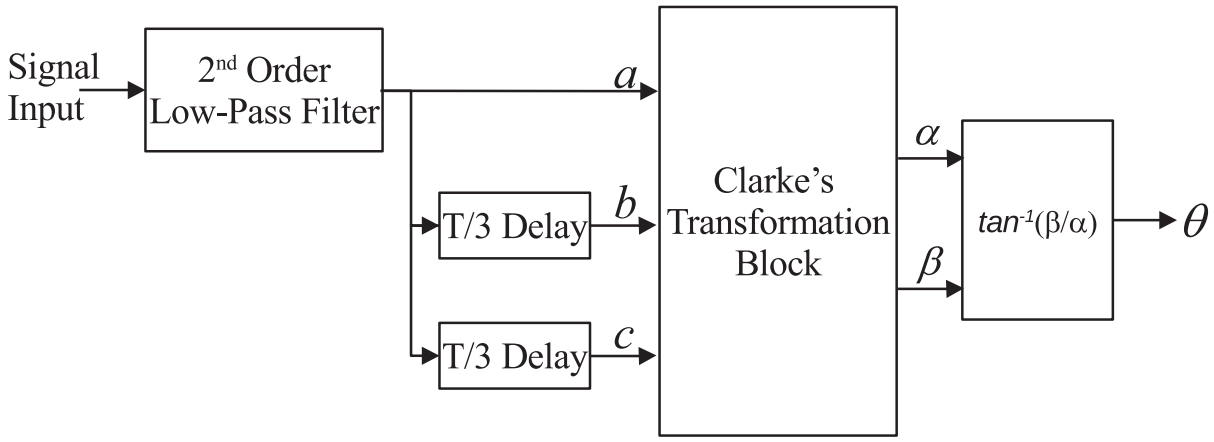

Figure 3.3: T/3 Delay PLL, using Clarke's Transformation.

3.6.1 T/3 Delay PLL

A $T/3$-$Delay$ PLL has been the simplest PLL structure that was tried to start working with the ES. Clarke transformation, being used for transforming the three-phase (a-b-c) into $2-\phi$ (α-β) quantities, has been used to create the phase angle of the reference signal. The creation of three-phase from the single phase has been carried out using a delay of one-third of the time period. For a time period of $20ms$, this delay has been calculated as $6.6667ms$. Phase angle θ can be calculated as,

$$\theta = tan^{-1}\frac{\beta}{\alpha} \tag{3.1}$$

The whole arrangement of this PLL can be seen from Fig: 3.3.

Looking at the results from Fig: 3.4, it is evident that this PLL has been working satisfactorily in the presence of harmonics, phase jumps, and signal amplitude variation, but it loses its efficacy as soon as it is subjected to a change in frequency. It responds to the amplitude variation, and phase jumps within two cycles ($40ms$) but can not follow the input in the case of variation in frequency and hence proved non-robust.

3.6.2 Single-Phase Synchronous Reference Frame PLL using Second Order Generalized Integrator as Orthogonal Signal Generator

This PLL structure is operating on the principle of orthogonal signal generation. Numerous methods of creating an orthogonal signal, using transport delay (presented in

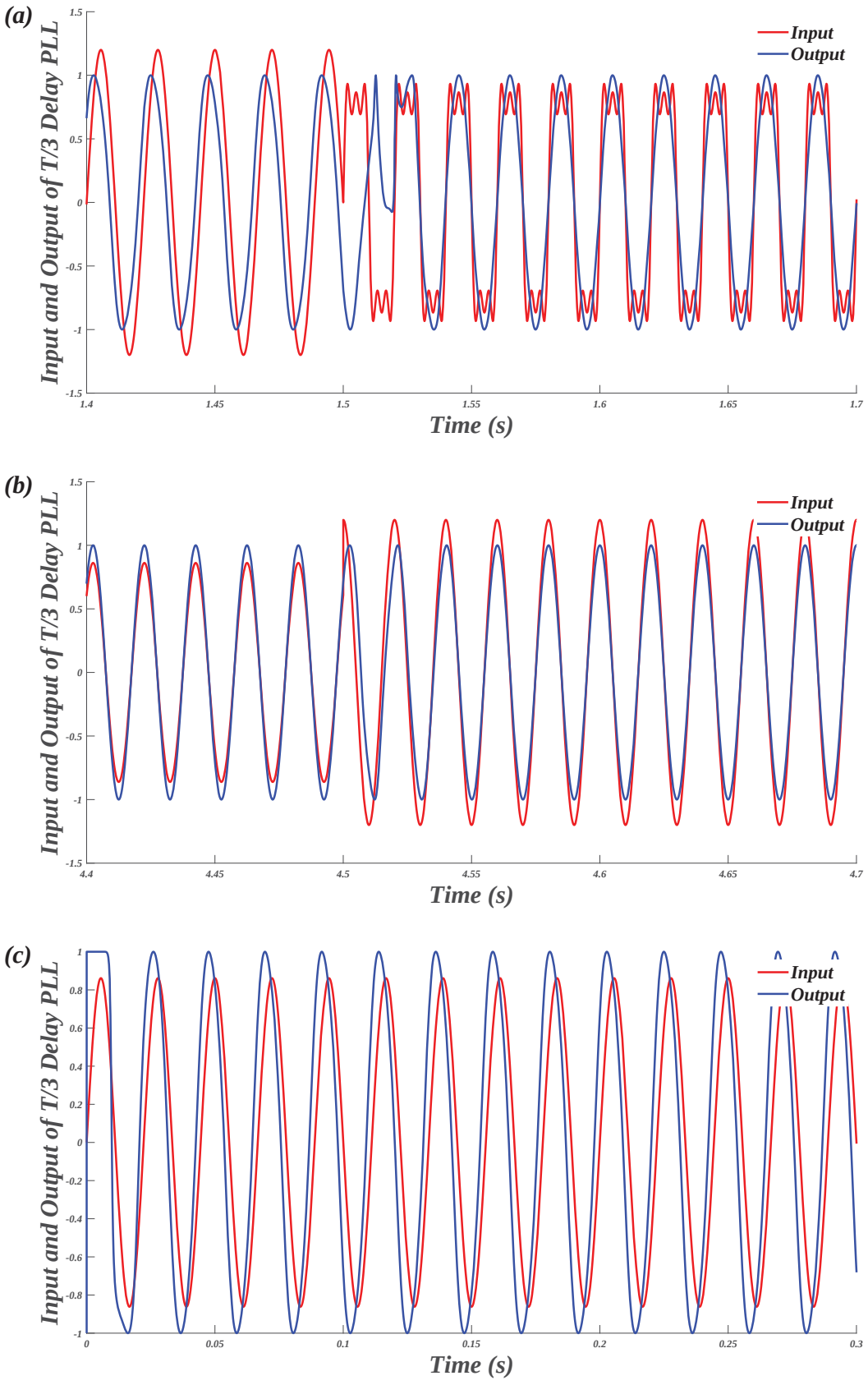

Figure 3.4: Results of the $T/3$-$Delay\ PLL$, amidst (a) Presence of 3^{rd} and 5^{th} Harmonics, (b) Change in signal Magnitude and Phase Jump, and (c) Change in Frequency.

Sec:3.6.1), Hilbert transforms [92], inverse Park's transforms [93] etc., have been presented in the literature, with their pros and cons. A robust single-phase PLL structure, using Park's transformation, has been presented in this section. This transformation of signals residing in the stationary reference frame ($u_{\alpha\beta}$) to the synchronous reference frame (u_{dq}) requires two signals, mutually orthogonal to each other. A simple and yet robust mechanism of Second-Order-Generalized-Integrator ($SOGI$) [94], has been adopted in this work for the creation of orthogonal signal u_β from the input signal u ($= u_\alpha$). The transformation can be explained using the space phasors. Let the space phasor $\vec{u}(t) = U_m e^{j(\omega t+\theta)} = u_\alpha + ju_\beta$. This can be transformed into dq-frame as,

$$u_d + ju_q = \vec{u}(t)e^{-j\delta t} = (u_\alpha + ju_\beta)e^{-j\delta t} \tag{3.2}$$

Let the input signal u, whose frequency and phase along with its magnitude is to be derived by the PLL, and the corresponding orthogonal signal u_q be represented as,

$$u_d = U_m cos(\omega t + \theta - \delta), \tag{3.3}$$

$$u_q = U_m sin(\omega t + \theta - \delta),\ further,\ let, \tag{3.4}$$

$$\frac{d\delta}{dt} = \omega(t) \tag{3.5}$$

Substituting $\delta(t) = (\omega t + \theta)$, for a condition where dq-frame is revolving in tandem with the angular velocity of the signal, leads u_q to zero. A system of regulating $u_q = 0$ can be developed on the following feedback law:

$$\omega(t) = H(p)\ u_q(t) \tag{3.6}$$

where,

$\omega(t)$, angular velocity of signal,

$H(p)$, transfer function of the controller,

p, a differential operator (d/dt),

Substituting (3.4) into (3.6) modifies it as,

$$\frac{d\delta}{dt} = H(p)\ U_m sin(\omega t + \theta - \delta) \tag{3.7}$$

Equation (3.7) represents a non-linear dynamic system, referred to as PLL. Tracking of $\omega t + \theta$, by the PLL structure leads $\omega t + \theta - \delta$ nearly to zero and hence (3.7) can again be modified to,

$$\frac{d\delta}{dt} = H(p)\ U_m(\omega t + \theta - \delta) \tag{3.8}$$

Equation (3.8) mimics a classical unity feedback control loop, possessing $\omega t + \theta$ as a command input, δ as an output and $H(s)\ U_m$ as a transfer function of the loop-gain, as can be depicted form Fig:3.5. The derivation and corresponding explanation of the

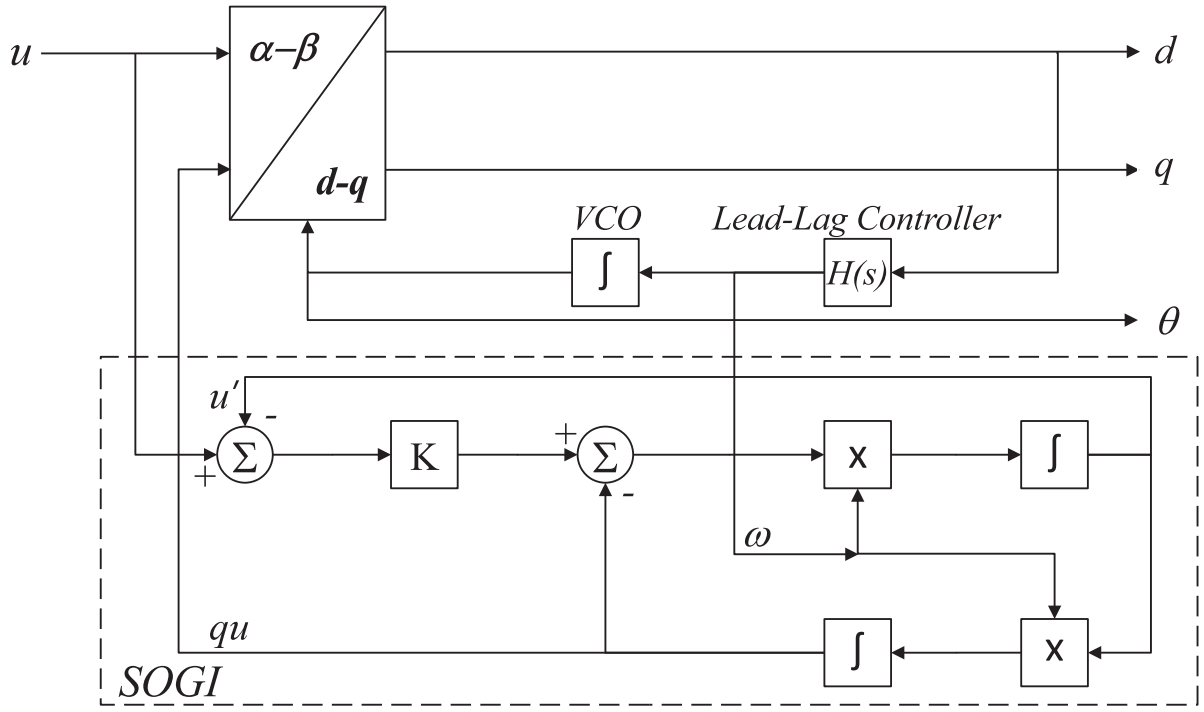

Figure 3.5: *SOGI-PLL* Structure Employing a *Lead* Compensator.

Controller ($H(s)$) and *SOGI*, mentioned in the Fig:3.5, have been presented in detail in the following sub-sections.

3.6.2.1 Second Order Generalized Integrator as Orthogonal Signal Generator

The standard structure of *SOGI* [94], in the form of the transfer function (G), can be represented as,

$$G(s) = \frac{\omega s}{s^2 + \omega^2} \tag{3.9}$$

The same in the closed loop be represented as,

$$G_d(s) = \frac{u'}{u} = \frac{k\omega s}{s^2 + k\omega s + \omega^2} \tag{3.10}$$

$$G_q(s) = \frac{qu}{u} = \frac{k\omega^2}{s^2 + k\omega s + \omega^2} \tag{3.11}$$

The bandwidth of the $SOGI$ is greatly dependent on the value of constant-k, and the same has been elaborated through the bode plot and step response plot. Bode plot of (3.10) resembles that of a band-pass filter, as can be depicted from Fig:3.6(a). Fig:3.6(b) shows bode plot of (3.11) resembling a low-pass filter. Step response of $SOGI$ for different values of k can be seen from Fig:3.7. Further, the value of k has an impact on the filtering abilities and response speed of the system. Larger value of k leads to a narrower pass-band but takes a longer time to respond to and vice-a-versa. Considering all these intricate factors of selecting the "k", the value of $k = 0.9$ has been considered for the realization of $SOGI$. Fig:3.8 authenticates the judicious selection of k, for the reason that the input signal u is nicely synchronized with the output signals u' and collectively, they are in quadrature with qu. The filtering action of $SOGI$ can be seen from the Fig:3.9(a) and Fig:3.9(b). Generation of orthogonal signal "qu" (having THD of 3.8%), from the input signal "u" possessing 3^{rd} and 5^{th} Harmonics (having THD of 38%) has nicely been executed by $SOGI$, without the loss of signal's amplitude.

$SOGI$ structure (3.9), being dependent on the operating frequency, has an adverse impact of change in the frequency. Adaptive tuning of the $SOGI$ has been executed through the ω extracted from the PLL structure.

3.6.2.2 Controller Design for PLL Structure

The controller $H(s)$ present in the "q" loop of the PLL has been acting as a filter, and a re-settable integrator (automatically reset to zero, as soon as it attains a value of 2π) has to serve the purpose of VCO, so as to generate the phase angle, δ. As mentioned in Sec:3.6.2, a PLL is required to track $\omega t + \theta$, which comprises a constant part associated with θ and a ramp signal associated with ωt. The constant part of the reference can be negotiated by the integral term present in the loop-gain to bring the steady-state error to zero, but the ramp component requires at least two integral terms, one of which having pole placed at zero and the pole location of another integrator can be fixed as per the demanded BW of PLL. The presence of the harmonics and double frequency component in the system debilitates the performance of PLL by introducing oscillations. The double frequency components demand more significant attenuation for the reason that their amplitudes are much greater than the other harmonic components. A strong Low-pass character can be achieved by the PI controller but with the compromised bandwidth. Robust

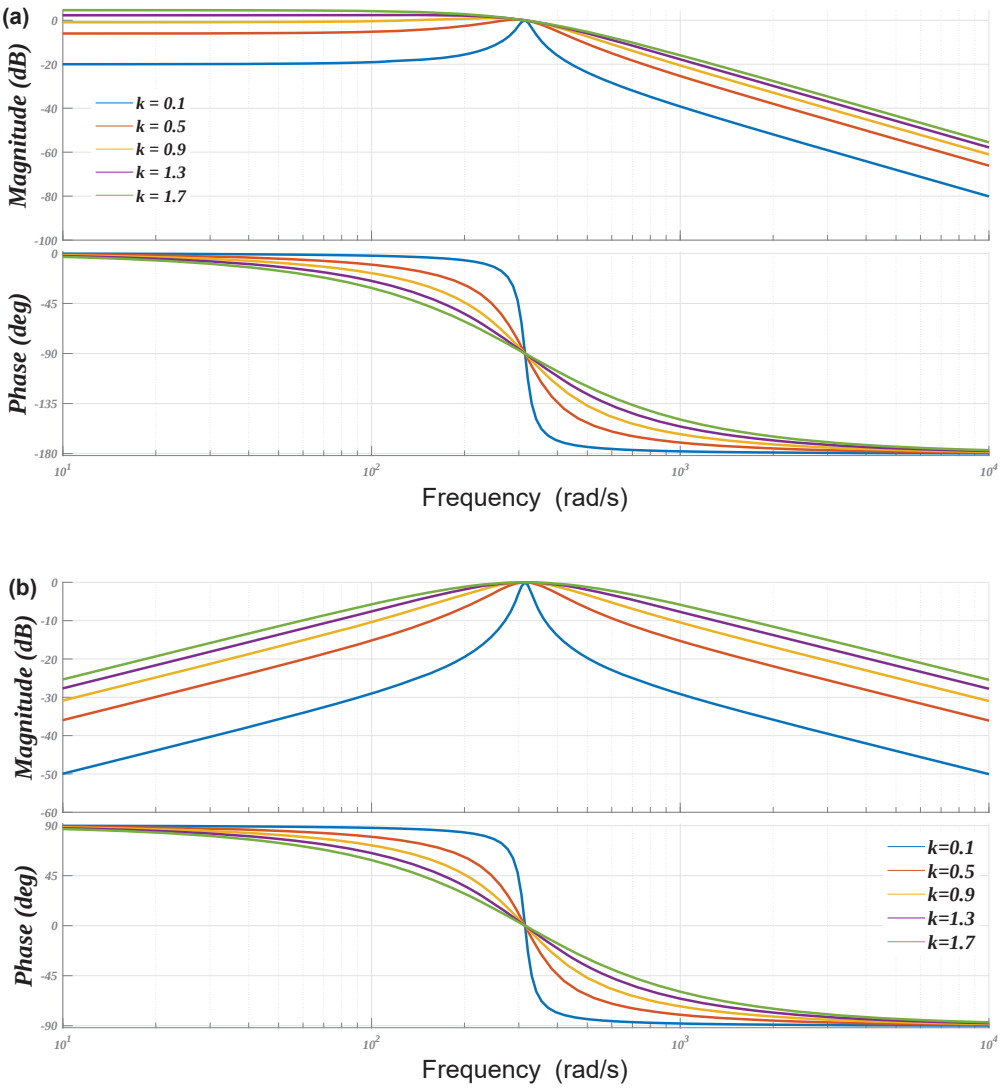

Figure 3.6: Performance Analysis of $SOGI$ through(a) Bode Plot of u'/u, and (b) Bode Plot of qu/u.

performance can only be achieved through the larger bandwidth. Further, smaller BW leads to fast response but introduces amplitude and phase angle error. On the other hand, larger BW leads to sluggish responses and may not serve the control system's very purpose. Conflicting requirement of controller design can be fulfilled by choosing adequately sufficient BW, way larger than the frequency of the command reference, and the same can be easily achieved using a *Lead* controller, having a larger BW and adequate robustness.

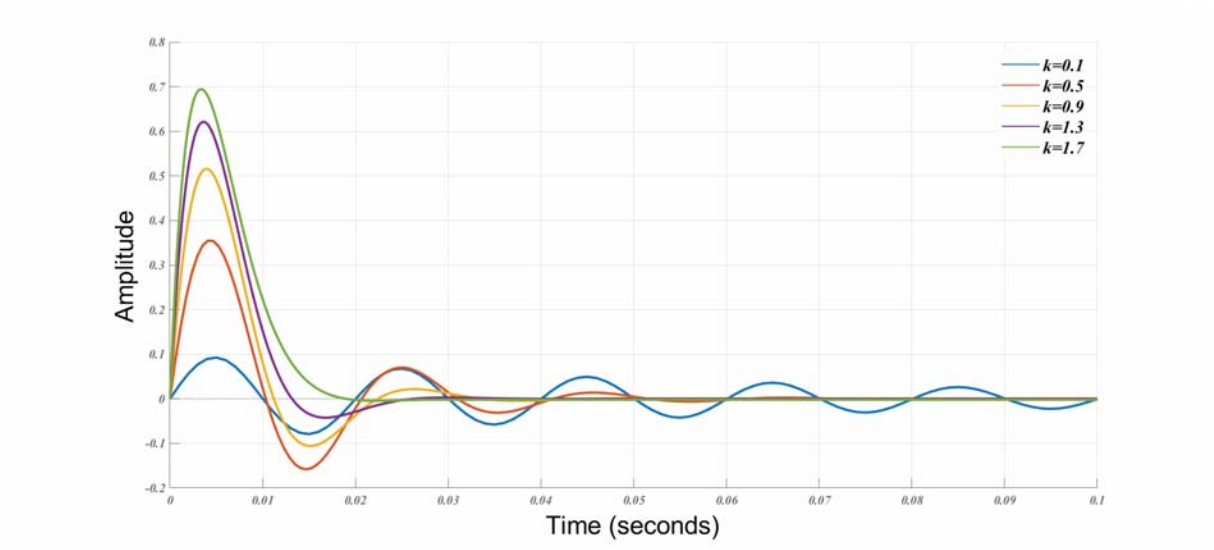

Figure 3.7: Performance Analysis of $SOGI$ through Step Response Employing u'/u.

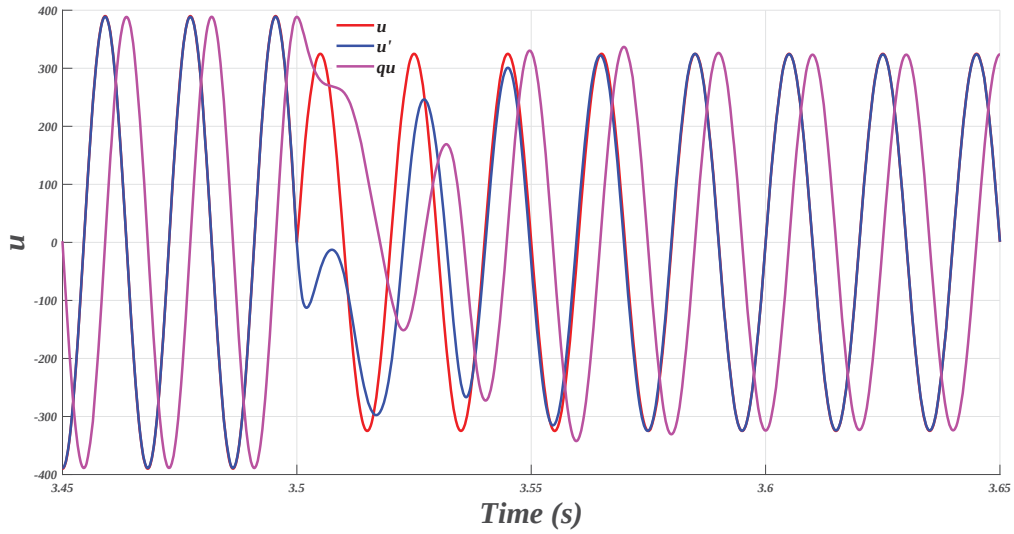

Figure 3.8: Performance Analysis of $SOGI$ through Instantaneous Variation of u, u' and qu.

The frequency response approach using loop shaping [95], through bode plot, has been used for deriving the *Lead* controller for the PLL structure mentioned in the Fig:3.5.

Consider the input signal u, having $U_m = 400$V, and $f = 50Hz$, applied to PLL. The *Lead* controller is required to counter the effect of the double frequency component, and hence, two complex conjugate zero's at $s = \pm j2\omega$, a pole at $s = 0$, and two real poles

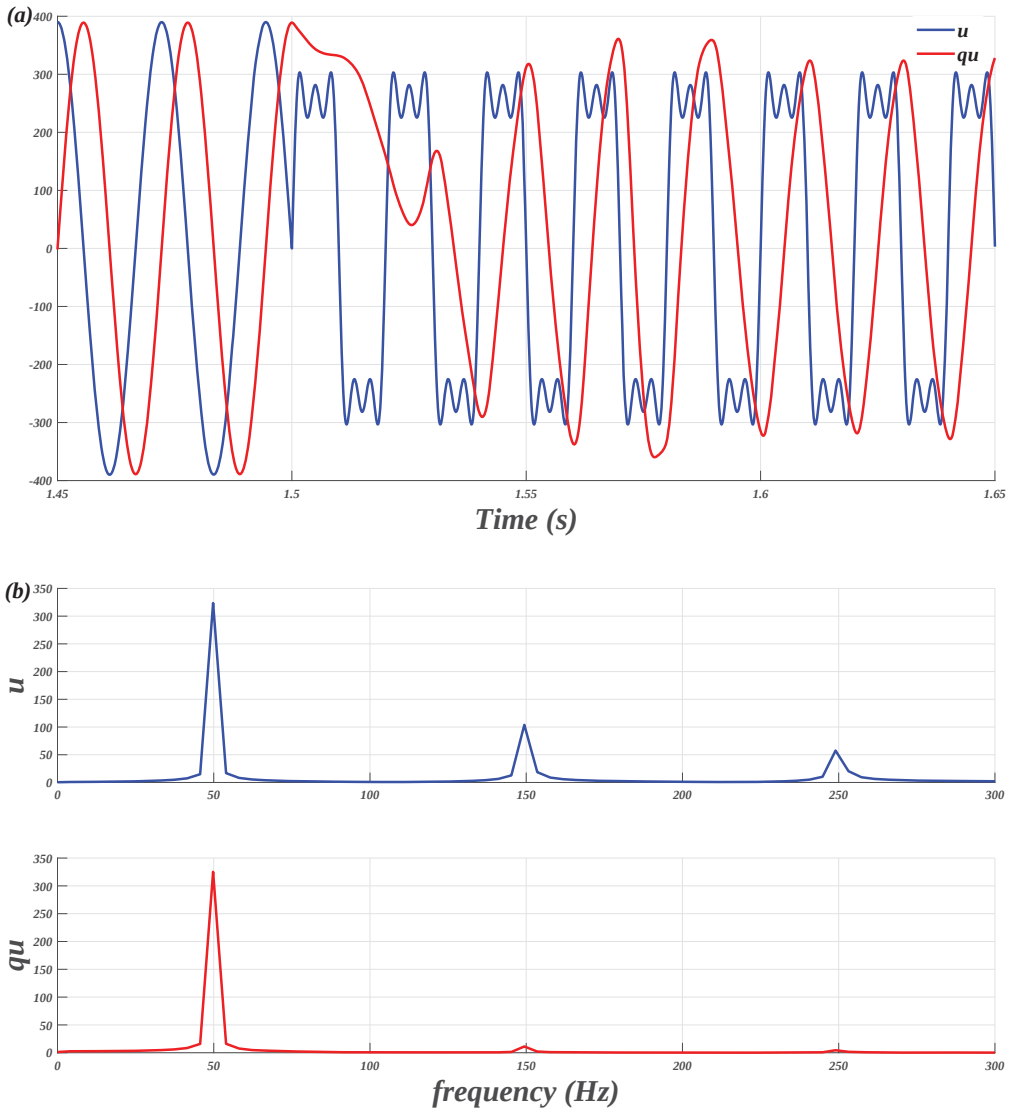

Figure 3.9: Performance Analysis of $SOGI$ through (a) u and qu in the presence of 3^{rd} and 5^{th} Harmonics, and (b) FFT of u and qu in the presence of 3^{rd} and 5^{th} Harmonics.

are placed at $s = -2\omega$, to mitigate the dynamics of $\omega t + \theta$, and it leads to the transfer function of the controller as,

$$\begin{aligned} H(s) &= \left(\frac{h}{U_m}\right)\frac{(s+j2\omega)(s-j2\omega)}{s(s+2\omega)^2}F(s) \\ &= \left(\frac{h}{U_m}\right)\frac{s^2+(2\omega)^2}{s(s+2\omega)^2}F(s) \end{aligned} \tag{3.12}$$

$F(s)$ is the proper transfer function of a *Lead* controller, with the absence of zero at $s = 0$.

The Loop gain, $\ell(s)$, as can be depicted from the Fig:3.5, be formulated as,

$$\ell(s) = \nu \frac{s^2 + (2\omega)^2}{s^2(s+2\omega)^2} F(s) \tag{3.13}$$

Considering $\nu F(s) = 1$, and anticipating a $P.M. = 60^\circ$ and gain-crossover frequency $\omega_c = 200 rad/sec$, the corresponding loop-gain has been found as $\angle \ell(j200) = -126^\circ$. The phase lead compensator $F(j200)$ is suppose to add a phase of 90° to $\angle \ell(j200)$, which happens to be an unachievable task for a *Lead* compensator, and hence it could be realized using two cascaded lead controllers offering a phase lead of 45° each.

The standard structure of the *Lead* compensator in [96], has been given as:

$$\begin{aligned} f_{Lead}(s) &= \frac{s+z}{s+p} = \frac{s+(\frac{p}{\alpha})}{s+p} \\ F(s) &= f_{Lead}(s)^2 = \left(\frac{s+(\frac{p}{\alpha})}{s+p}\right)^2 \end{aligned} \tag{3.14}$$

Value of h can be found for,

Maximum phase lead $\sigma_{max} = 45^\circ = sin^{-1}\left(\frac{\alpha-1}{\alpha+1}\right)$,

the value of α is found to be $\alpha = 5.83$, which is further being used in deducing the value of p from,

$\omega_c = \frac{p}{\sqrt{\alpha}}$, giving $p = 82.84$.

Substituting these values in (3.14), we get,

$$\begin{aligned} f_{Lead}(s) &= \frac{s+82.84}{s+482.8}, \\ F(s) &= \left(\frac{s+82.84}{s+482.8}\right)^2 \end{aligned} \tag{3.15}$$

Substitution of (3.15) in (3.13), yields $\ell(s)$ as,

$$\ell(s) = \nu \left(\frac{s^2 + 628.32^2}{s^2(s+628.32)^2}\right)\left(\frac{s+82.84}{s+482.8}\right)^2 \tag{3.16}$$

Further, calculating the value of h for $|\ell(j200)|$, gets us $h = 2.8571e+05$ and using $U_m = 400V$, ultimately leads to $\nu = 714.27$. Substituting this value of ν and (3.15) into (3.12) yields the overall transfer function of the controller $H(s)$ as,

$$H(s) = \frac{714.3s^4 + 1.183e05s^3 + 2.869e08s^2 + 4.672e10s + 1.935e12}{s^6 + 2222s^5 + 1.841e06s^4 + 6.742e08s^3 + 9.204e10s^2} \tag{3.17}$$

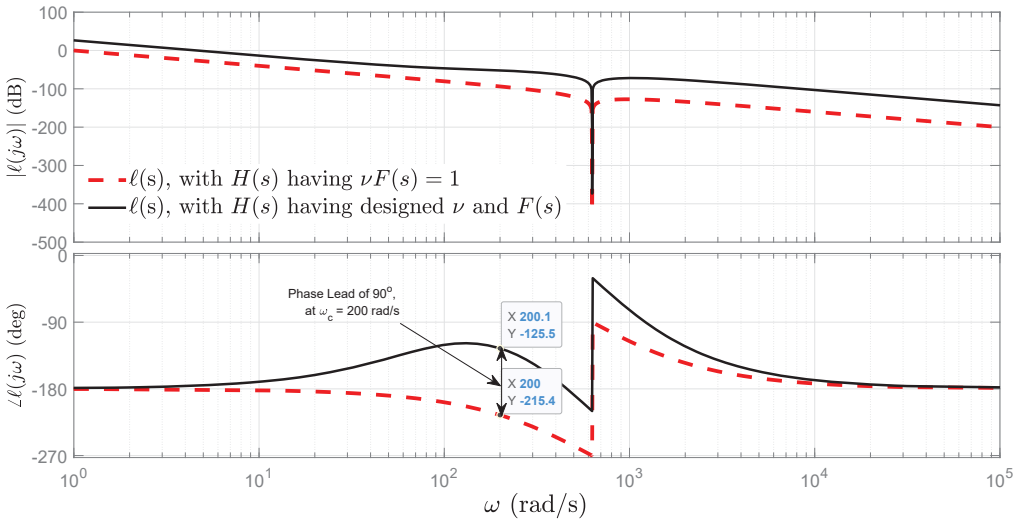

Figure 3.10: Frequency Response of Controller Employing *Lead* Compensator.

Frequency response plot (shown in Fig:3.10) of the resulting loop gain ($\ell(s)$) shows a phase lead of 90° added by the *Lead* controller ($F(s)$) to the initial phase. The compensator's performance has been tested with the test-bench (Fig:3.2), and the corresponding results have been presented in the next section.

3.6.2.3 Results of Second Order Generalized Integrator-PLL

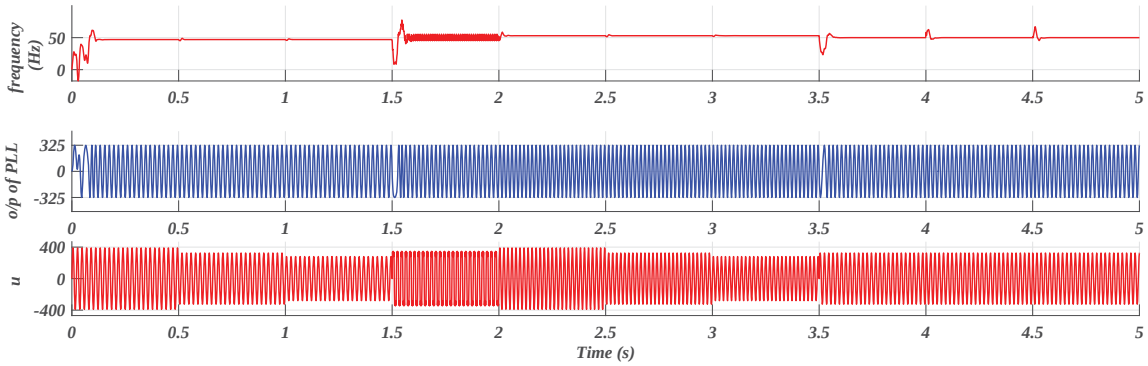

Figure 3.11: Absolute Spectrum of the Results Fached through *SOGI-PLL*.

Performance of the *SOGI-PLL* can be justified from Fig: 3.11 through Fig:3.15, showing measured frequency and output of PLL for an input u. The frequency and

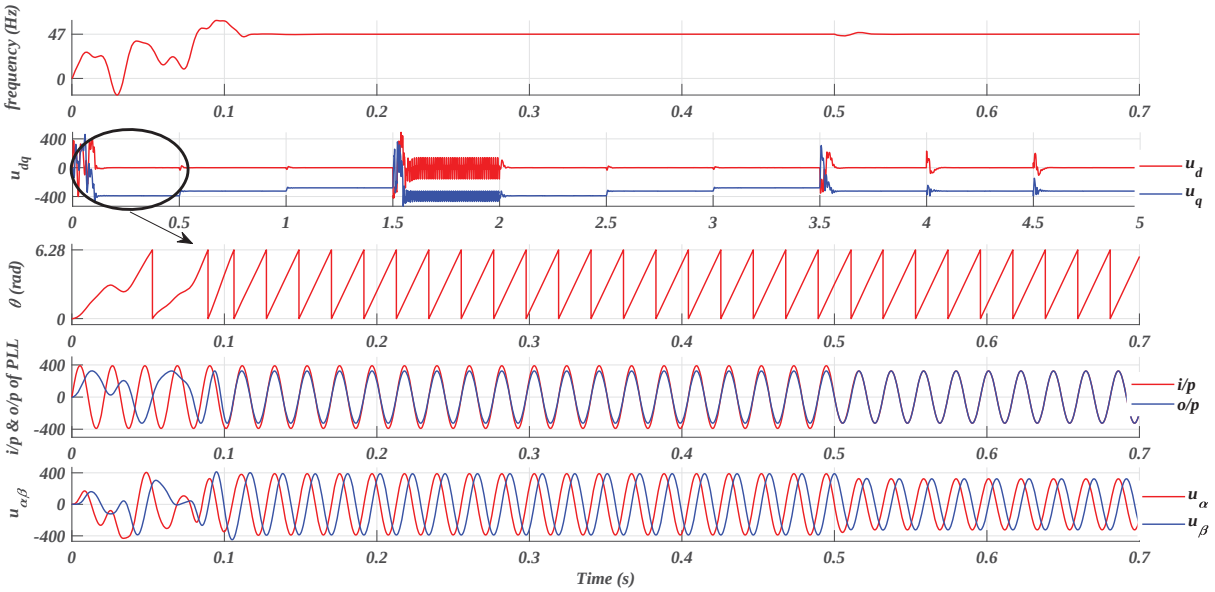

Figure 3.12: Results of *SOGI-PLL* Showing Start-up Delay.

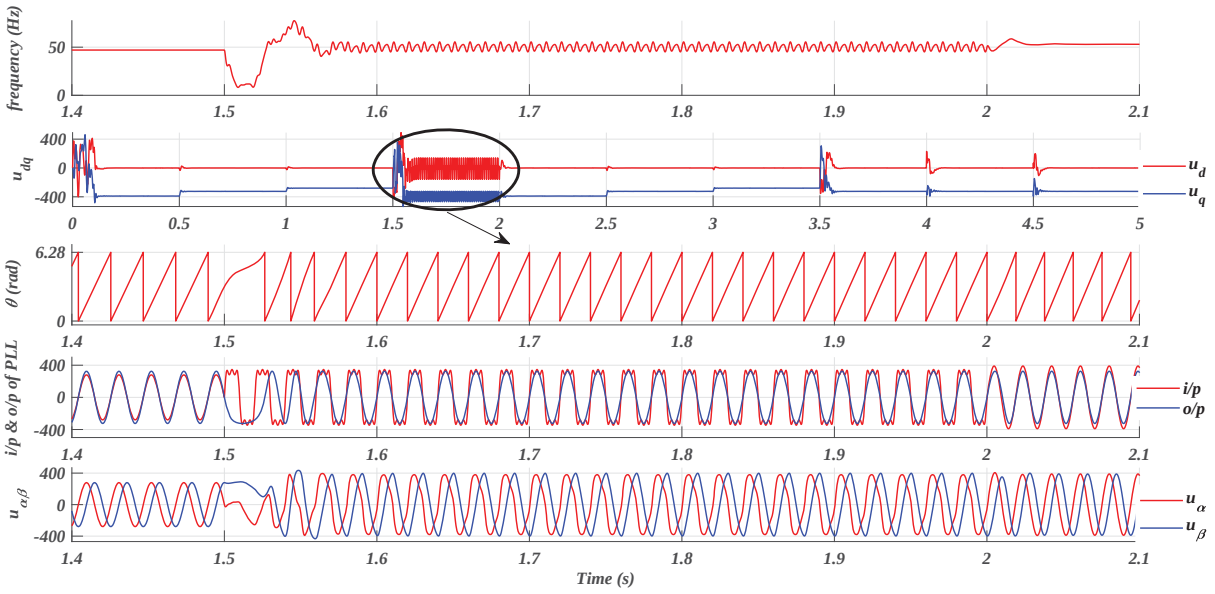

Figure 3.13: Performance of *SOGI-PLL* in the Presence of Harmonics.

amplitude of the signal u have been varied as per the Table:3.1.

Period of the results pertaining to the encircled portion of u_{dq} of Fig:3.12 through Fig:3.15 has been magnified to present the changes that is taking place in (i) output of PLL, (ii) $u_{\alpha\beta}$, (iii) u_{dq}, (iv) δ and (v) measured frequency, at the wake of perturbations in

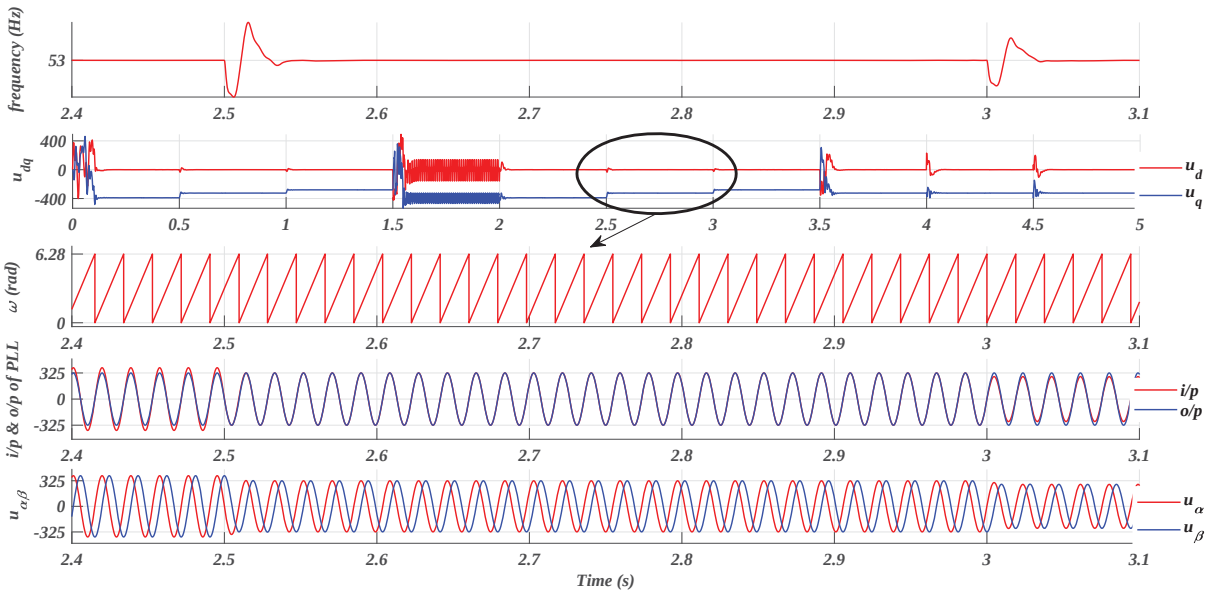

Figure 3.14: Performance of *SOGI-PLL* Amidst Step Change Applied in the Magnitude of the Input Signal.

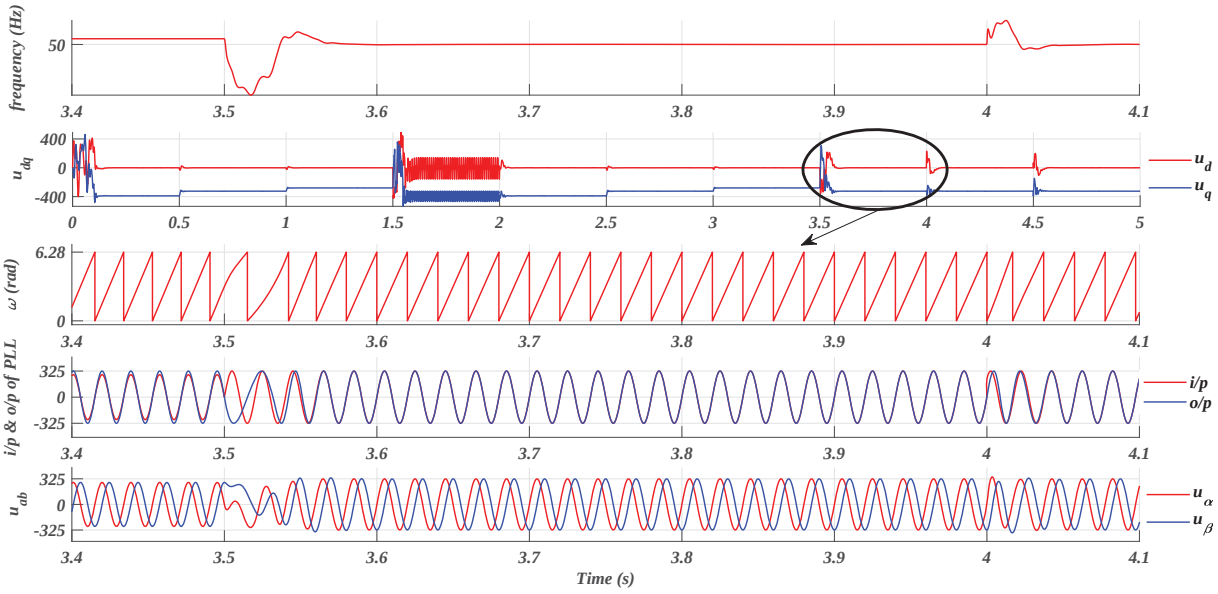

Figure 3.15: Performance of *SOGI-PLL* Amidst Step Change Applied in the Phase of the Input Signal.

amplitude and frequency of the input of the *PLL*. The results pertaining to the change in frequency, amplitude, phase jump, and start-up delay have been assimilated in the

Table 3.1: Results of *SOGI-PLL*, Employing a Phase *Lead* Controller

Time Interval (in s)	***Peak Amplitude*** U_m	***Frequency of u (in Hz)***	***Order of Harm. in u***	***Phase Angle (in deg.)***	***Type of Change***	***Synchro. Time (in s)***	***Error (in deg.)***
0.0-0.5	400	47	f_o	0	Amplitude	0.1	0.226728
0.5-1.0	325	47	f_o	0	Amplitude	0.01	0.223852
1.0-1.5	280	47	f_o	0	Amplitude	0.01	0.225036
1.5-2.0	$U_o = 325$; $U_3 = U_o/3$; $U_5 = U_o/5$	f_o=50; f_3=150; f_5=250	f_o + f_3 + f_5	0	Harmonics	0.08	0.223513
2.0-2.5	400	55	f_o	0	Frequency & Amplitude	0.02	0.222667
2.5-3.0	325	55	f_o	0	Amplitude	0.07	0.221821
3.0-3.5	280	55	f_o	0	Amplitude	0.02	0.220975
3.5-4.0	400	50	f_o	0	Frequency & Amplitude	0.07	0.220129
4.0-4.5	325	50	f_o	45	Amplitude & Phase	0.07	0.219283
4.5-5.0	280	50	f_o	90	Amplitude & Phase	0.06	0.218437

Table:3.1, with corresponding error in the measurement.

SOGI-PLL is taking the start-up time of around $0.1s$ to get the output synchronized with the input, which happens to be the worst-case delay. This *PLL* responds to amplitude jump in less than 1.5 cycles, and Phase jump is managed by it in 3.5 cycles. Error encountered in the measurement is around 0.2°. These results reveal the excellent performance of the *SOGI-PLL* and its controller's robust worthy performance under the considered variation in the signal conditions considered for the application with *ES*.

3.6.3 Enhanced-Phase Locked Loop Structure

The enhanced phase-locked loop (*EE-PLL*) alleviates the primary limitation of the standard *PLL* structure, i.e., oscillations created due to double frequency components and further responsible for introducing error. *E-PLL* structure was proposed in [97]. A modified version of the same has been presented in Fig:3.16 comprising of *PLL* structure

shown within the dotted rectangular box, and the rest is acting as VCO to bring out the *E-PLL* structure.

A lot of information associated with an input signal u can be recovered or estimated, and the same has been listed as follows:

1. Phase angle θ.
2. Orthogonal information of θ that is $\theta^{\perp}$
3. Angular frequency ω.
4. Signal's amplitude U_o, and corresponding normalized amplitude U_{on}
5. Signal y_f and a filtered version y, perfectly synchronized with the input signal u.
6. Total distortion present in the input signal (in the form of white noise, harmonics, DC offset, phase and frequency induced oscillations and transients).

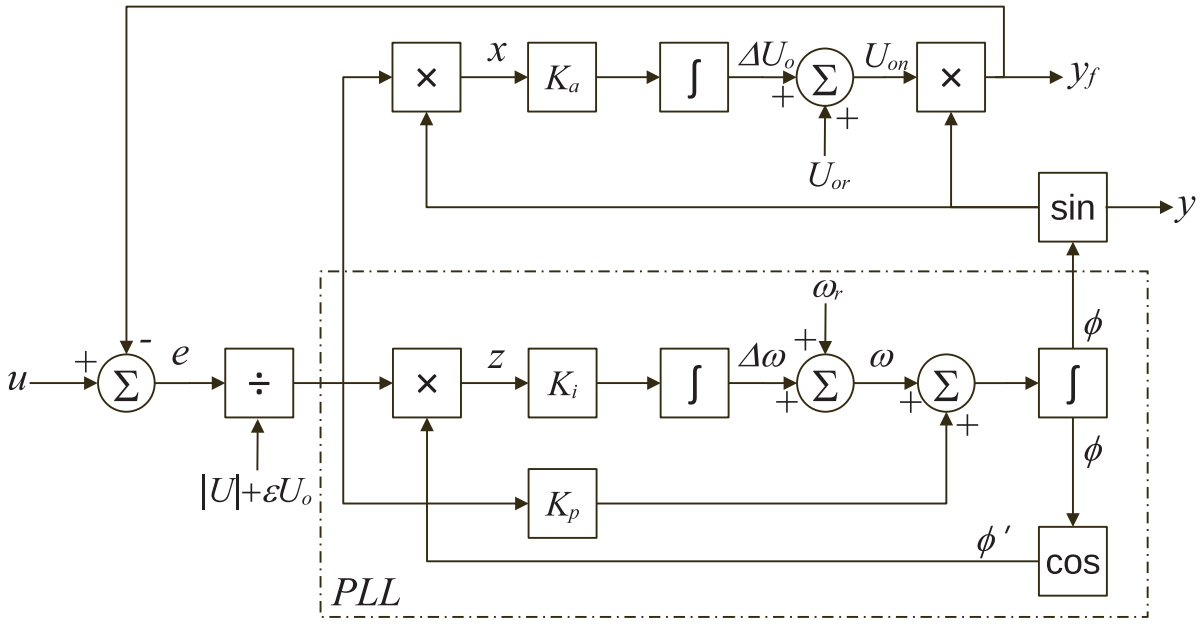

Figure 3.16: *E-PLL* Structure.

Much information can be assimilated from *EE-PLL*, with a bit of modification in the standard *PLL* structure to get it transformed into *EE-PLL*.

Let, Double Frequency error

$$\begin{aligned} u &= U_m sin\phi_i = U_m sin(\omega t + \theta), \\ y &= U_o sin\phi_o \end{aligned} \tag{3.18}$$

if, $u = y$, than we can say that $U_m = U_o$, $\phi_o = \phi_i$, and all these conditions lead to $e = 0$ and the output of the P.D.(multiplier) in PLL block, leads to,

$$\begin{aligned} z &= e\ cos\phi_o = (U_i sin\phi_i - U_o sin\phi_o)cos\phi_o, \\ &= \frac{U_i}{2} sin(\phi_i - \phi_o) + \frac{U_i}{2} sin(\phi_i + \phi_o) - \frac{U_o}{2} sin(2\phi_o) \end{aligned} \tag{3.19}$$

Similarly, top multiplier gives,

$$\begin{aligned} x &= e\ sin\phi_o = (U_i sin\phi_i - U_o sin\phi_o)sin\phi_o, \\ &= \frac{U_i}{2} cos(\phi_i - \phi_o) - \frac{U_o}{2} - \frac{U_i}{2} cos(\phi_i + \phi_o) + \frac{U_o}{2} cos(2\phi_o) \end{aligned} \tag{3.20}$$

The equations (3.19) and (3.20) incorporate double frequency components. Under steady state condition, i.e., where $U_i = U_o$, $\phi_o = \phi_i$, the double frequency components cease to zero, leading to asymptotic stability and error free response. The analysis of $E\text{-}PLL$ has nicely been elaborated using "Gradient Method" and "Newton Method" in [97].

The $E\text{-}PLL$ structure is employing three gains named as, K_p (Proportional constant), K_i (integral constant) and K_a (amplitude constant). Recommended range of these parameters has been presented in [97]. As per the recommendations these values could be chosen as, $K_p = K_a = 2 \times \zeta_1 \omega = 444.29$, and $K_i = \frac{\omega^2}{2} = 49348$. In this work, the integral gain K_i has been adaptively chosen to minimize the start-up time and improvise the transient performance of the frequency measurement at the instance of phase jump, and the same is represented as,

$$K_i = \omega^2 \times \frac{1}{1 + \frac{\lambda|e|}{|U_m| + \epsilon U_o}} \tag{3.21}$$

where, $\lambda = 10$ and $\epsilon = 0.01$ have been chosen for calculating the value of K_i (3.21), which has been adaptively changing its value depending on the magnitude of the error.

3.6.3.1 Results of Enhanced-Phase Lock Loop Structure

Designed $E\text{-}PLL$, as per the specifications mentioned in Sec:3.2, has been implemented in experimental test-bench (Fig: 2.7) and the corresponding results, have been assimilated

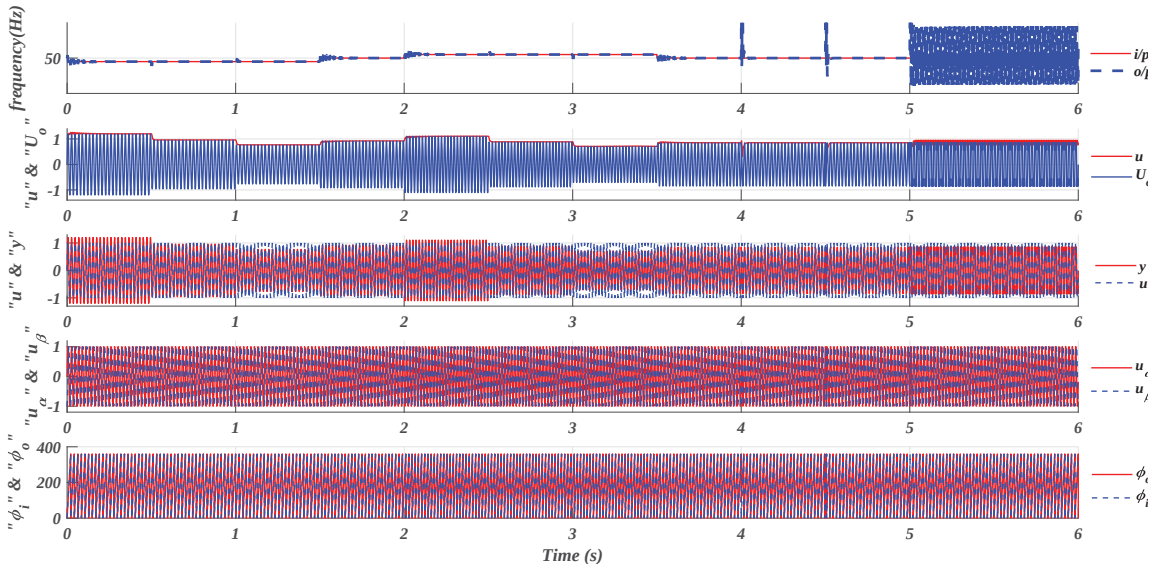

Figure 3.17: Absolute Spectrum of *E-PLL* Results.

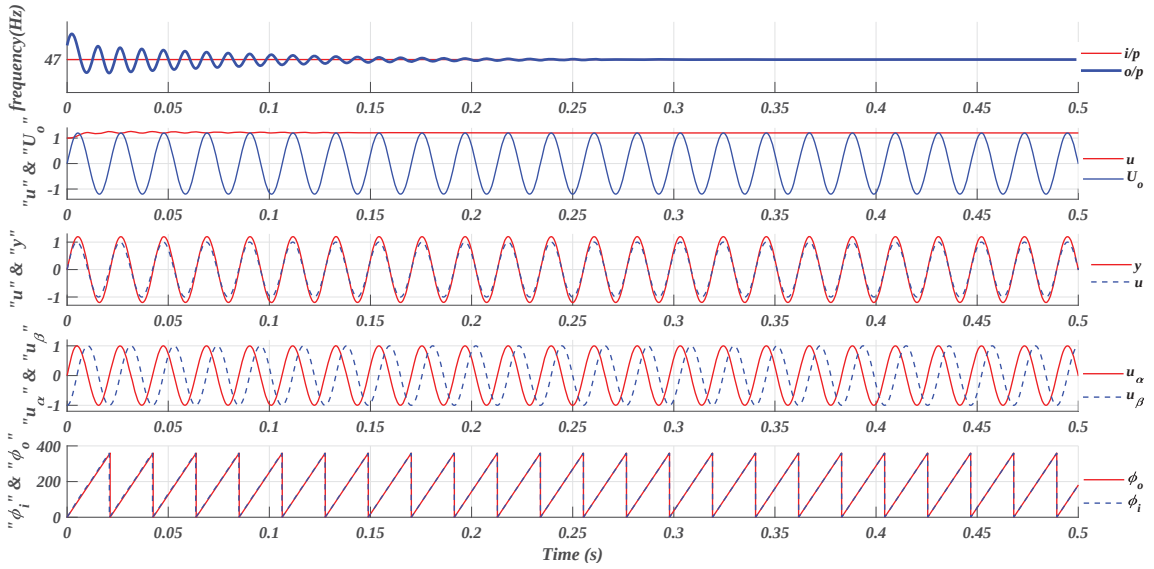

Figure 3.18: Spectrum of *E-PLL* Results Showing Start-up Delay.

in the Table: 3.2 and have graphically been presented in Fig:3.17 through Fig: 3.23. Complete spectrum of the results has been presented in Fig: 3.17. This spectrum has been magnified, at the point of a step change of interest, i.e., at the wake of changes applied in the Amplitude, Frequency, and Phase, and presence of harmonics at the time stamp mentioned in Table: 3.2, to get the performance evaluation of *E-PLL*.

Fig: 3.18 depicts an initial start-up time of 0.01s and is quite satisfactory. The transition of 47Hz to 50Hz can be seen to be smoothly accomplished by this structure in just

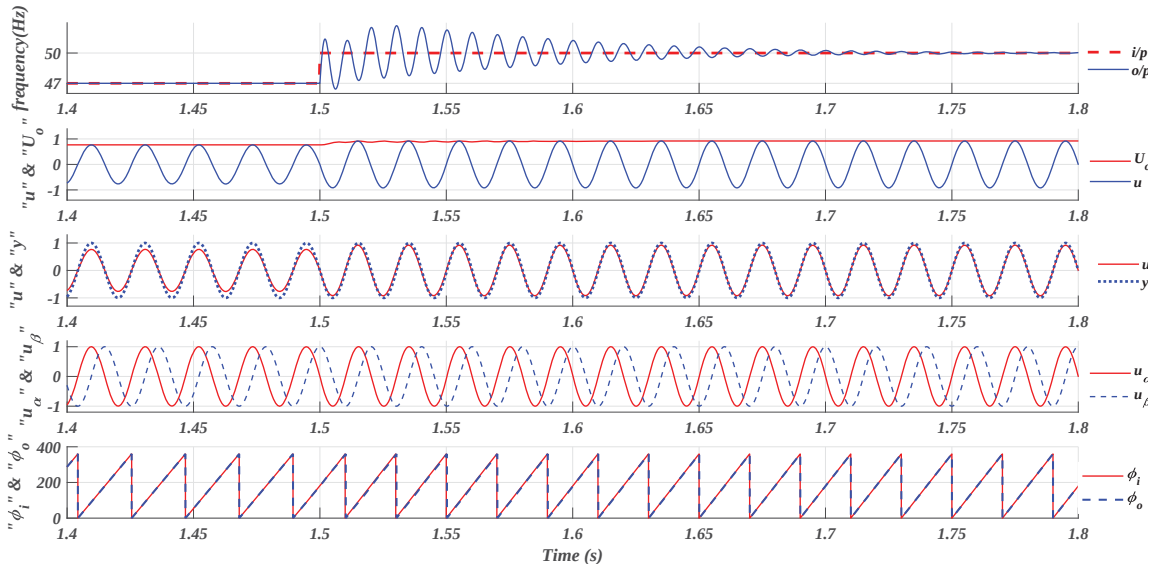

Figure 3.19: Spectrum of *E-PLL* Results Showing Frequency Jump.

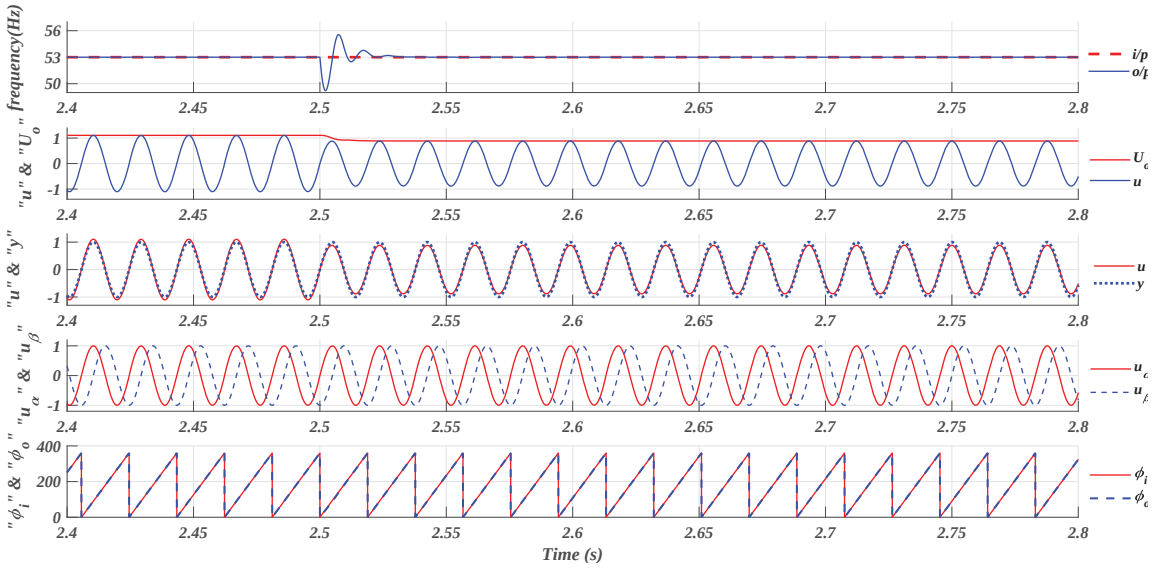

Figure 3.20: Spectrum of *E-PLL* Results Showing Step Change in the Amplitude.

three cycles of the supply frequency, as shown in Fig: 3.19. Detection of zero-crossing and hence phase angle is accomplished within less than three cycles for all the types of dynamic conditions. Phase jump (0° to 45°) and amplitude variation are settled in just one cycle i.e., less then $20ms$, by this PLL and the same can be verified from Fig: 3.21 and Fig: 3.20. The harmonically molested signal can be deciphered from the Fig: 3.22 and corresponding filtering performance is evident from Fig: 3.23 through its FFT analysis. This PLL structure has not performed filtering action, with excellent efficacy (THD of

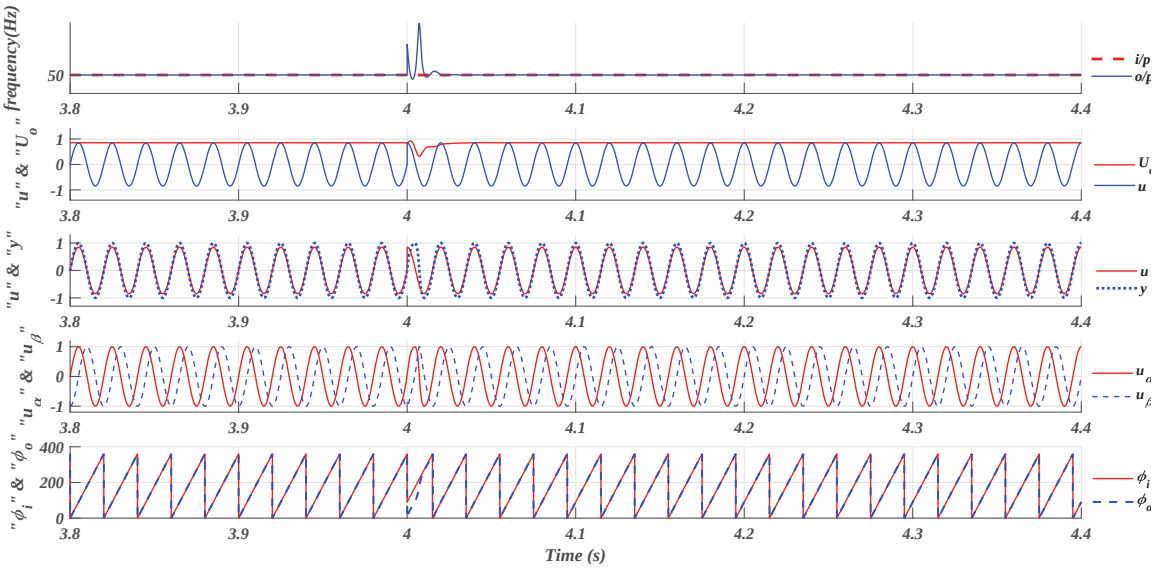

Figure 3.21: Spectrum of *E-PLL* Results Showing Phase Jump.

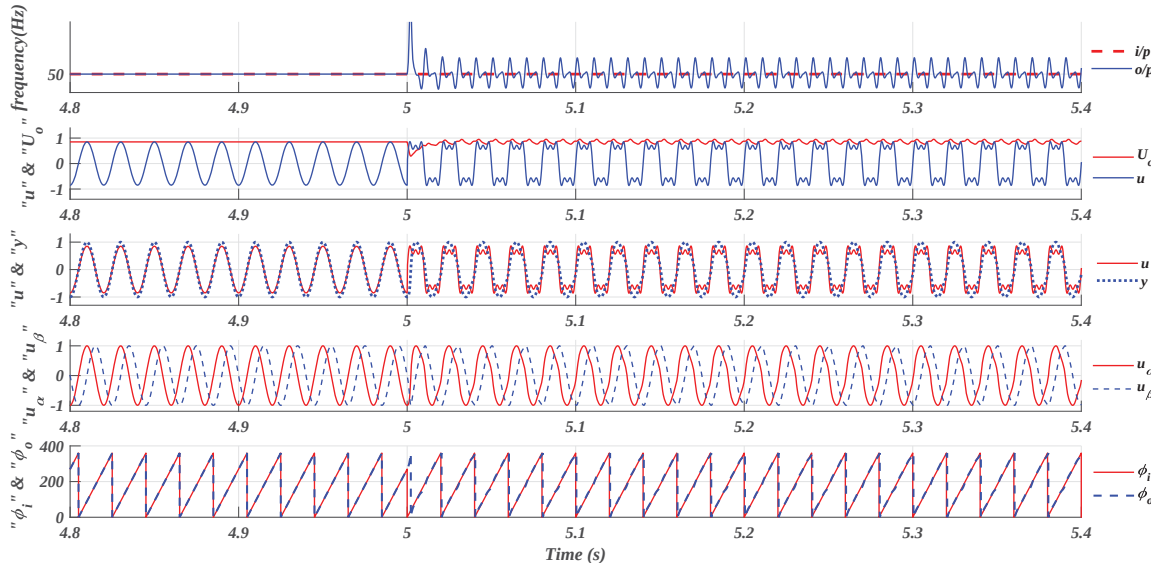

Figure 3.22: Performance of *E-PLL* in the Presence of Harmonics in the Input.

9%), as evident from its *FFT* spectrum. Frequency measurement shows dynamics (as can be seen from Fig: 3.17 through Fig: 3.22), but then it is not the needed quantity for the application of *ES*, and hence it could always be neglected.

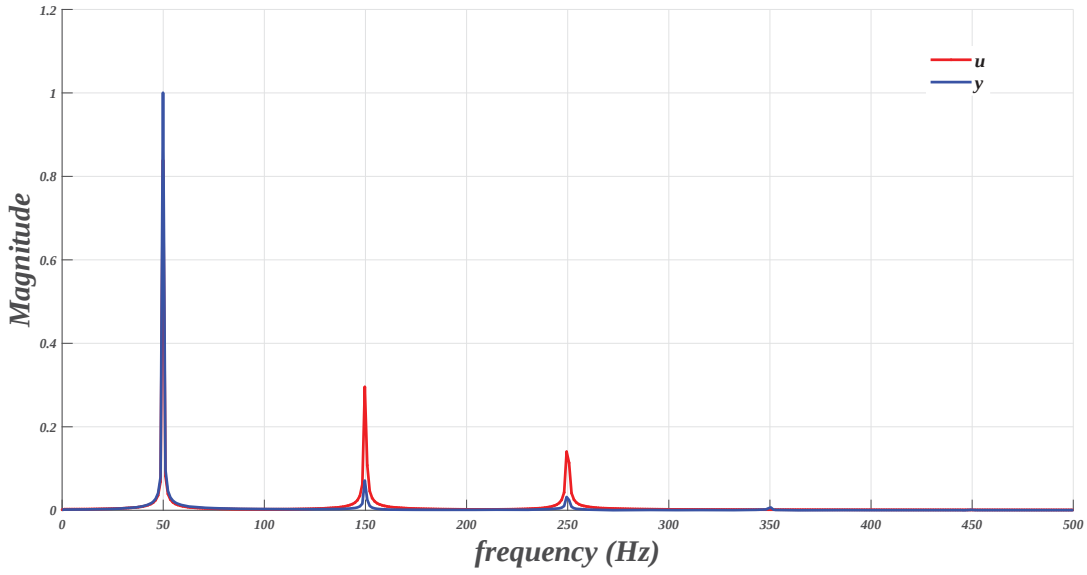

Figure 3.23: E-PLL Results Showing the FFT Spectrum of the Input and Output Signals.

3.7 Comparison of the Results

A comparative analysis of the results achieved from the performance of three PLL structures presented in Section: 3.6 has been carried out to check the compliance of different PLL structures, to set aside performance indices. It can be seen from the performance of the $T/3-$delay PLL (Fig: 3.4) that it can not catch up with the frequency jump, and hence it has not been considered here for the comparison. Further, the frequency estimation is irrelevant to the application of ES, and hence dynamics present in its estimation can always be ignored for this application, though synchronization of "y" with "u" is the most desired one with changing frequency. Absolute spectrum of the results can be seen from the Fig: 3.28, comprising of plots pertaining to input signal (u), Output of the $PLL's$ (y_{epll} and y_{spll} of E-PLL and $SOGI$-PLL, respectively), instantaneous phase angle variation pertaining to input (ϕ_i) and estimated ones (ϕ_{epll}, and ϕ_{spll}), Amplitude of the input signal (U_i) and estimated amplitudes (U_{epll}, and U_{spll}), and input frequency (f_i) and estimated frequencies (f_{epll}, and f_{spll}).

3.7.1 Start-up Delay

At the instance of the system's initial starting, a PLL structure undergoes some dynamics before getting into synchronization with the input signal perfectly, called start-up delay.

Table 3.2: Results of *E-PLL*

Time Interval (in s)	***Peak Amplitude*** U_m	***Frequency of u (in Hz)***	***Order of Harm. in u***	***Phase Angle (in deg.)***	***Type of Change***	***Synchro. Time (in s)***	***Error (in deg.)***
0.0-0.5	400	47	f_o	0	Amplitude	0.1	0.226728
0.5-1.0	325	47	f_o	0	Amplitude	0.01	0.223852
1.0-1.5	280	47	f_o	0	Amplitude	0.01	0.225036
1.5-2.0	325	50	f_o	0	Amplitude	0.01	0.225036
2.0-2.5	400	55	f_o	0	Frequency & Amplitude	0.02	0.222667
2.5-3.0	325	55	f_o	0	Amplitude	0.07	0.221821
3.0-3.5	280	55	f_o	0	Amplitude	0.02	0.220975
3.5-4.0	400	50	f_o	0	Frequency & Amplitude	0.07	0.220129
4.0-4.5	325	50	f_o	45	Amplitude & Phase	0.07	0.219283
4.5-5.0	280	50	f_o	90	Amplitude & Phase	0.06	0.218437
5.0-6.0	$U_o = 325$; $U_3 = U_o/3$; $U_5 = U_o/5$	f_o=50; f_3=150; f_5=250	f_o + f_3 + f_5	0	Harmonics	0.08	0.223513

Looking at the frequency and Amplitude plots of Fig: 3.25, start-up dynamics happens to be present in both *SOGI-PLL* and *E-PLL*, but in *E-PLL*, Amplitude, Phase, and Frequency attain steady-state and synchronism in less than Two Cycles which is way faster than *SOGI-PLL* (takes more than five cycles).

3.7.2 Step Change in the Magnitude of the Input

The amplitude step-change is applied to the signal under the measurement at the time instances specified in the Table:3.3. One such change can be envisaged from the Fig: 3.26. Both the $PLL's$ under consideration retaliates with this type of change instantaneously with a delay of less than 20ms. *E-PLL* attains steady-state faster than *SOGI-PLL* in terms of Frequency, Amplitude, and Phase estimation.

Table 3.3: Comparative Analysis of Results of *E-PLL* and *SOGI-PLL*

Time Interval (in s)	***Peak Amplitude Um***	***Frequency of u (in Hz)***	***Frequencies Included***	***Phase Angle (in deg.)***	***Type of Change***	***Time to Synchronize***						*PLL* ***Error (in deg.)***	***S-PLL Error (in deg.)***
						U_{epll}	U_{spll}	ϕ_{epll}	ϕ_{spll}	f_{epll}	f_{spll}		
0.0-0.5	390	47	f_0	0	Amplitude	0.02	0.11	0.04	0.1	0.01	0.11	0.226728	0.0
0.5-1.0	325	47	f_0	0	Amplitude	0.02	0.02	0.02	0.02	0.01	0.02	0.223852	0.0
1.0-1.5	271	47	f_0	0	Amplitude	0.01	0.01	0.02	0.02	0.01	0.02	0.225036	0.0
1.5-2.0	390	50	f_0	0	Frequency & Amplitude	0.08	0.06	0.02	0.07	0.08	0.04	0.219283	0.0
2.0-2.5	390	55	f_0	0	Frequency & Amplitude	0.06	0.06	0.02	0.05	0.08	0.04	0.222667	0.0
2.5-3.0	325	55	f_0	0	Amplitude	0.02	0.02	0.02	0.02	0.02	0.03	0.221821	0.0
3.0-3.5	271	55	f_0	0	Amplitude	0.02	0.02	0.02	0.02	0.02	0.03	0.220975	0.0
3.5-4.0	325	50	f_0	0	Frequency & Amplitude	0.08	0.08	0.02	0.05	0.08	0.06	0.220129	0.0
4.0-4.5	325	50	f_0	45	Amplitude & Phase	0.03	0.10	0.02	0.1	0.04	0.08	0.219283	0.0
4.5-5.0	325	50	f_0	90	Amplitude & Phase	0.03	0.10	0.02	0.14	0.04	0.11	0.218437	0.0
5.0-6.0	U_o = 325; $U_3 = U_o/3$; U_5=$U_o/5$	f_0=50; f_3=150; f_5=250	f_0 $+f_3$ $+f_5$	0	Harmonics	0.08	0.10	0.02	0.1	0.0	0.0	0.5562	8.9532

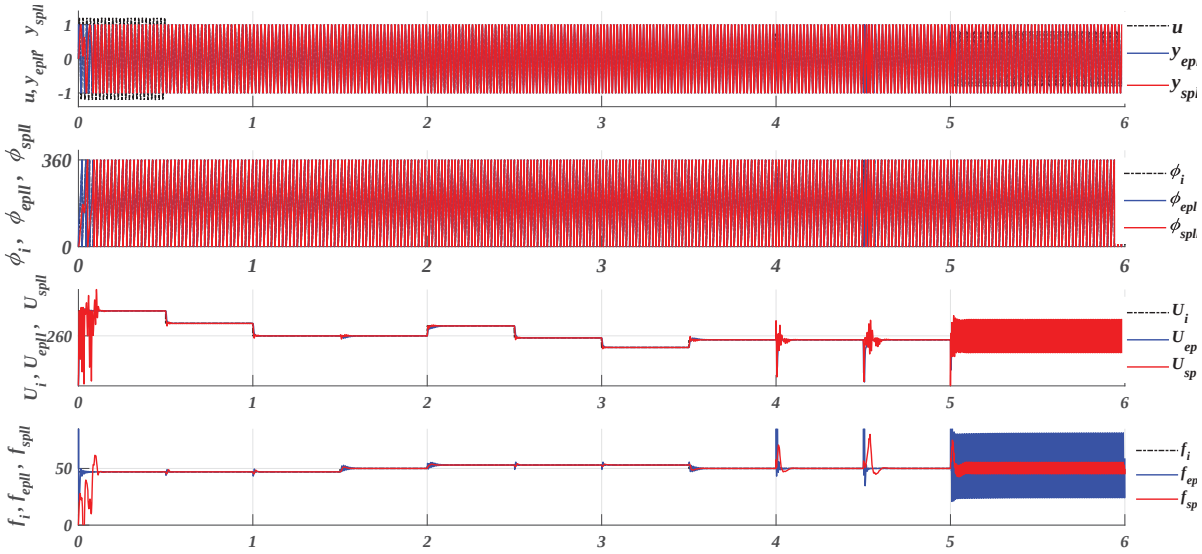

Figure 3.24: Absolute Spectrum of Comparative Results associated with u and y for (a) Instantaneous Per Unit Values, (b) Instantaneous Phase Variation, (c) Amplitude Variation and (d) Frequency Variation, of input and corresponding output of *E-PLL* and *SOGI-PLL*.

3.7.3 Step Change in the Frequency of the Input

The step-change in the frequency has been applied at three different instances (at 1.5s, 2s, and 3.5s) along with the amplitude variation. These changes have been negotiated

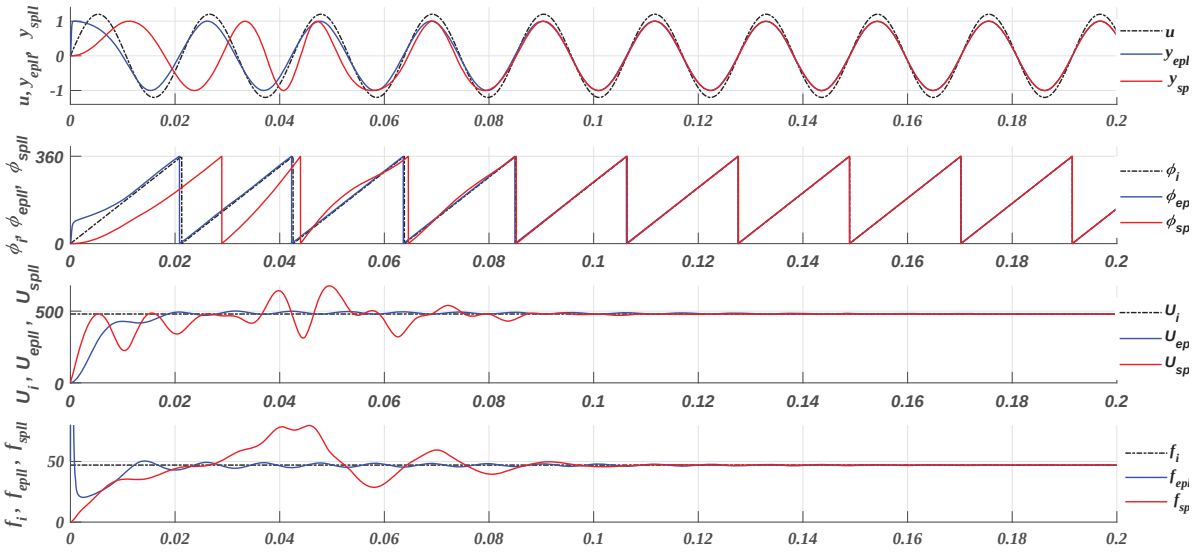

Figure 3.25: Magnified View of the Comparative Results Showing Start-up Delay.

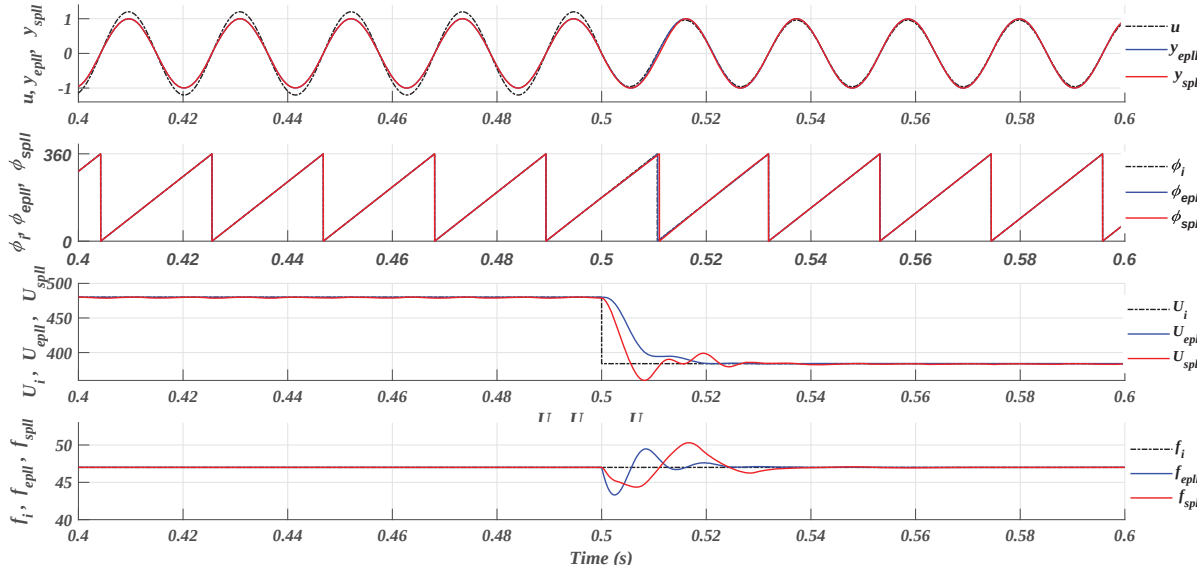

Figure 3.26: Magnified View of the Comparative Results Showing Step Change in the Magnitude.

by *E-PLL* pretty efficiently, in terms of Amplitude and Frequency estimation, as can be seen from Fig: 3.27. Phase angle has been estimated at almost the same instance by both the $PLL's$

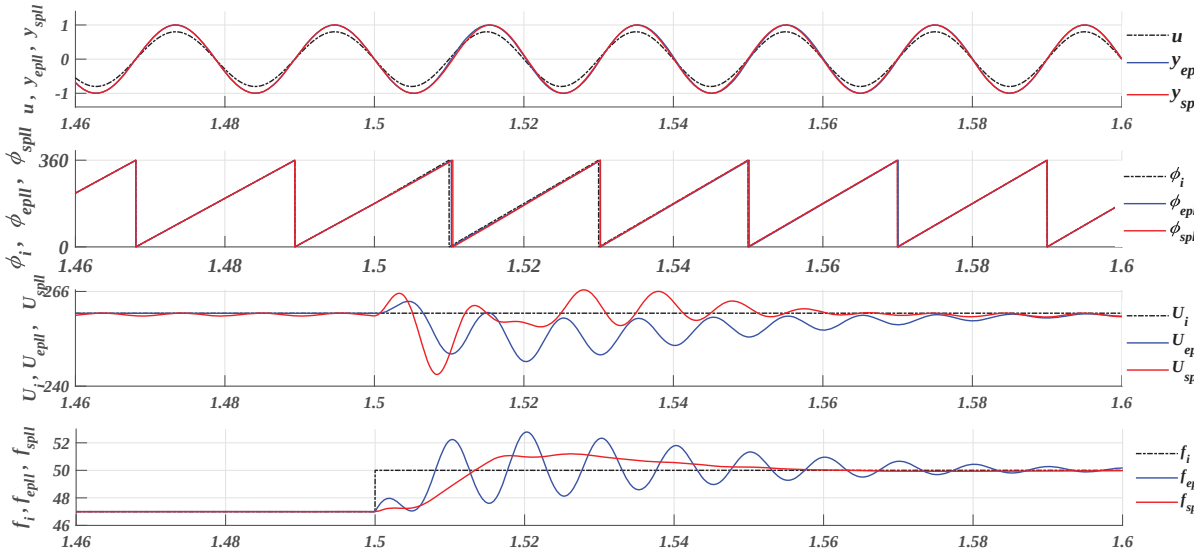

Figure 3.27: Magnified View of the Comparative Results Showing Step Change in Frequency.

3.7.4 Step Change in the Phase of the Input

Phase jump has been applied to the signal at two different instances (at 4s and 4.5s with a change in phase angle from 0° - 45°, 45° - 90° respectively). Looking at the instance of 4.5s, it can be seen that *E-PLL* attains synchronization in terms of estimation of Phase, frequency, and Amplitude in less than a cycle, whereas *SOGI-PLL* takes more than three cycles for the same task. *E-PLL* is a clear winner in terms of satisfactory accomplishment of this task.

3.7.5 Applying Step Change to the Amplitude and frequency of the Input

This type of change has been applied at two instances (at $1.5s$ and $2s$, with a change in amplitude of $1V$-$1.2V$, and $1.2V$-$1V$ (P.U.) with a corresponding change in frequency, from $47Hz$ to $50Hz$, and $50Hz$ to $53Hz$, respectively). One such instance, as depicted in Fig: 3.29, has been chosen for this analysis. Frequency change causes *E-PLL* to attain synchronization in a longer time compared to *SOGI-PLL*. Synchronization in the Phase estimation is achieved simultaneously by the two $PLL's$, in less than two cycles.

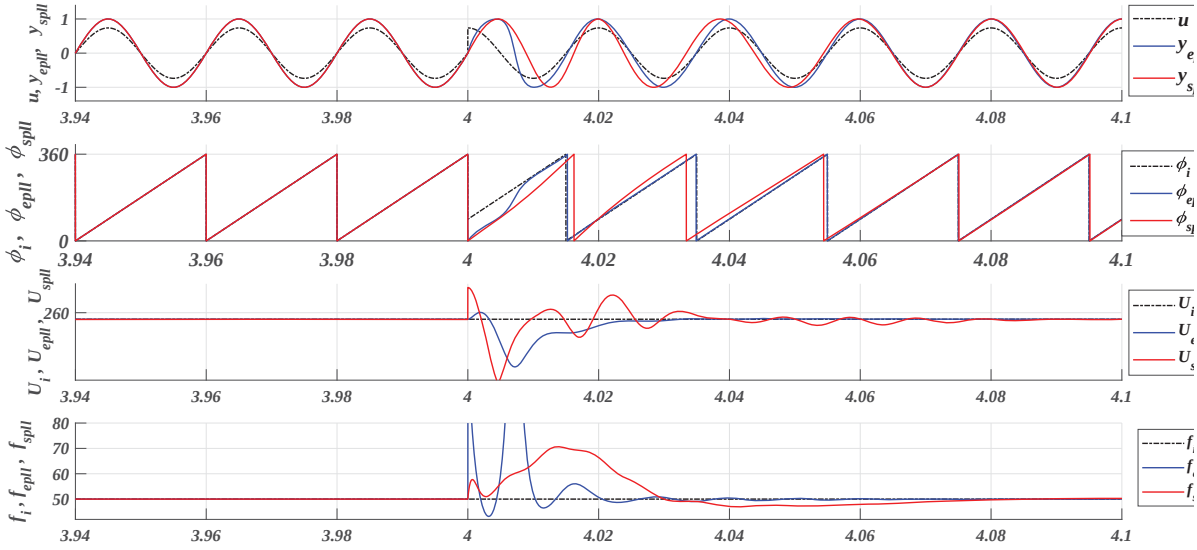

Figure 3.28: Magnified View of the Comparative Results Showing Phase Jump.

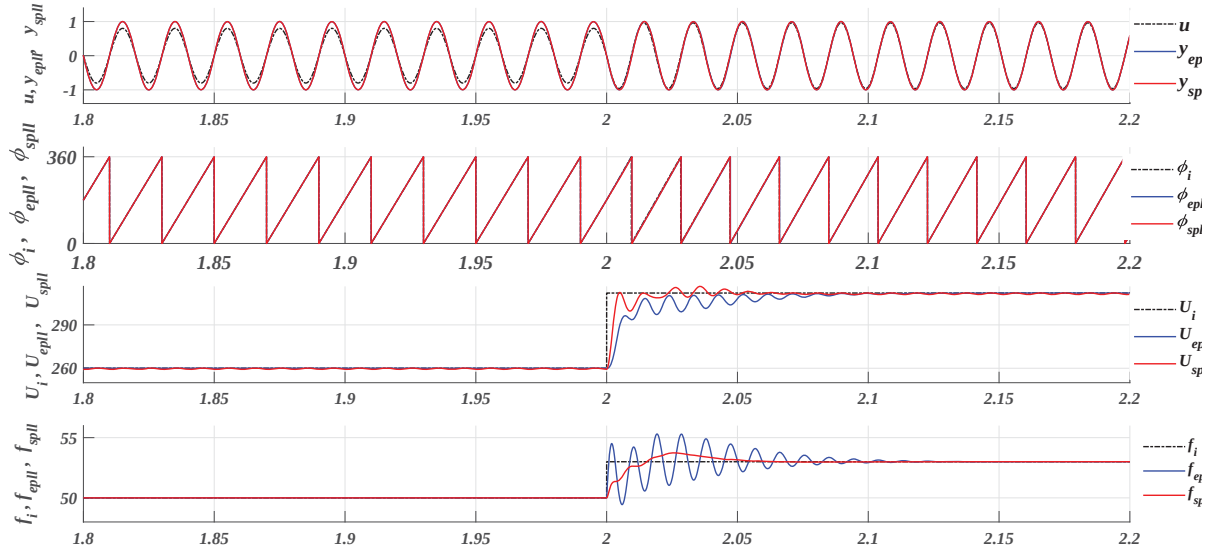

Figure 3.29: Magnified View of the Comparative Results Showing Simultaneous Step Change in Amplitude and Frequency.

3.7.6 PLL Subjected to Harmonics

3^{rd} and 5^{th} harmonic components having an amplitude of $U_m/3$ and $U_m/5$, respectively, have been applied with the fundamental one, at 5s. *E-PLL* attains the input phase (less than one cycle) much faster than *SOGI-PLL* (three cycles). Further, amplitude estimation is achieved by *E-PLL* with better accuracy and fewer oscillations, as compared

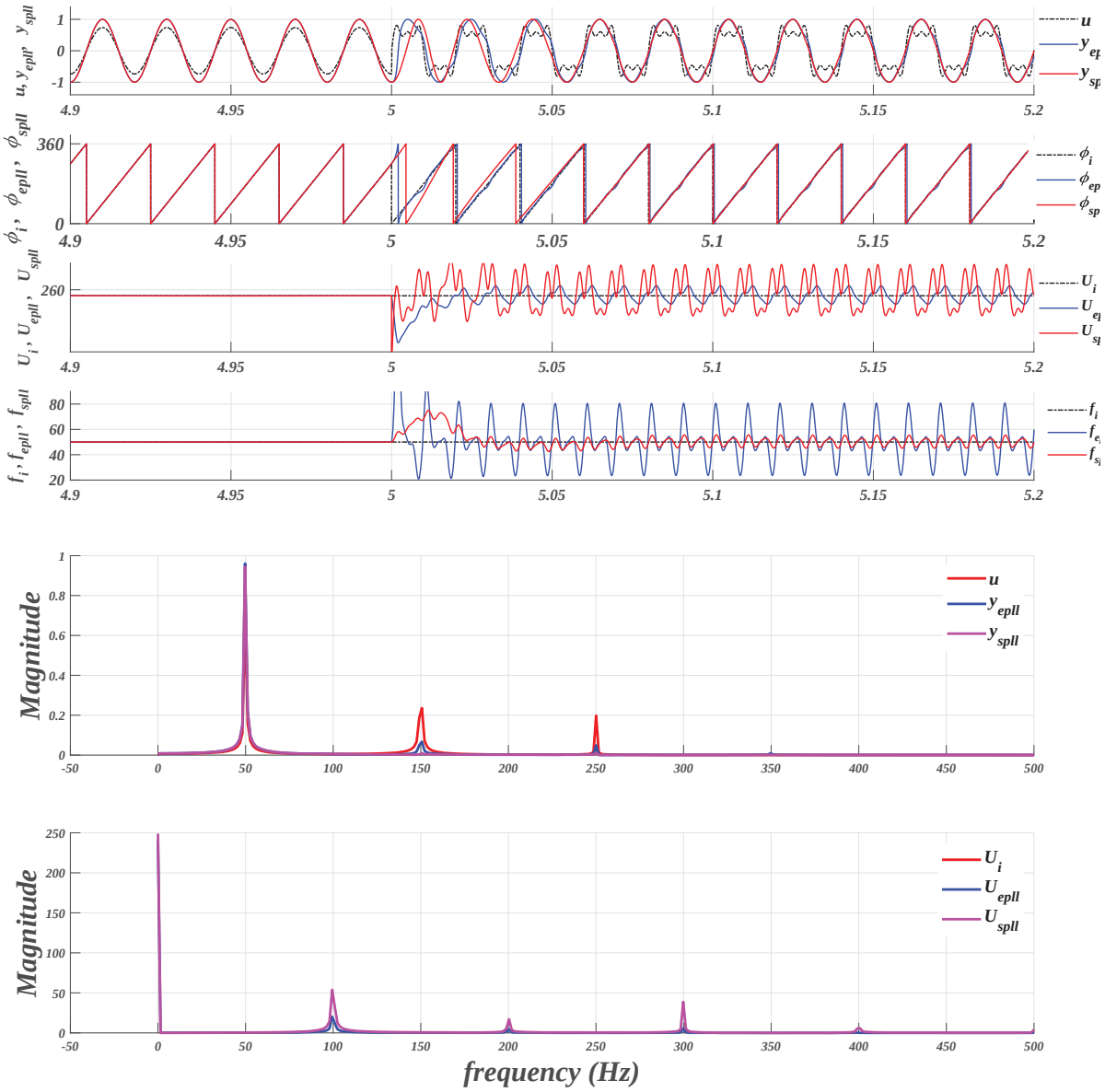

Figure 3.30: Magnified View of the Comparative Results for Harmonically Molested Signal.

to *SOGI-PLL* . Performance of the two *PLL* structures has also been compared in terms of their harmonic content (shown in Fig: 3.30) being measured through *THD*, using the *FFT* analysis. Harmonically molested input signal (u) having *THD* of 52% has been filtered, and corresponding *THD* is reduced to 1.5% in *SOGI-PLL* compared to 9% by *E-PLL*. The filtering performance of *E-PLL* has been enhanced by increasing "$\zeta_1 = 0.25$", at the cost of debilitating performance in response speed.

3.8 Conclusion

The design and implementation of $SOGI\text{-}PLL$, is far more complicated, as it represents a 5^{th} order controller compared to a 2^{nd} order controller in the case of $E\text{-}PLL$. Further, the estimation of phase angle and amplitude by $EE\text{-}PLL$ in the presence of step-change in amplitude, frequency, and phase jump has been performed excellently compared to $SOGI\text{-}PLL$. The Start-up delay of $E\text{-}PLL$ is almost negligible compared to $SOGI\text{-}PLL$. Frequency estimation is executed well by $SOGI\text{-}PLL$, compared to $E\text{-}PLL$, but is a quantity of non-interest, as far as the application of PLL for ES is concerned. Results of the comparative analysis lead to the conclusion that $E\text{-}PLL$ is a better choice for the application with ES.