Chapter 4

Control of Electric Spring: A Proportional Integral Controller Compensated Approach

4.1 Introduction

The controller is the brain behind the operation of ES, considering ES as the body of the system, being employed for the purpose of voltage regulation of Critical loads. The control of ES, being a crucial element of the system, has been analyzed critically, using a PI controller and its design aspect in this chapter. Published technical literature on ES invariably has a mention about its control aspect, which in most of the cases being implemented with a PI controller in a way or other.

Control of the system can broadly be categorized into three groups:

1. **Conventional Control Techniques** [**95**] - being executed with an assumption that the system is a $SISO$ system and controller is derived using pole placement methods through the transfer function derived from the mathematical model of the system, and the same has been the subject matter of this chapter.

2. **Modern Control Techniques** [**98**]- it can be employed using the state-space model of the system, which could be a $MIMO$ system. It is called a multi-variable system for the reason that it is being employed on the $MIMO$ system. Numerical methods of optimization of the controller can be employed here. This happens to

be the subject matter of the next two chapters.

3. **Heuristic [99] and Meta-Heuristic Methods [100]** - Optimization of the controller can be gained through the use of genetic algorithms, particle swarm optimization, and the gravitational search algorithm etc. Meta-heuristic methods of optimization could be employed using Fuzzy logic.

A short state-of-the-art survey of the control aspect of ES, employing conventional control techniques, has been summarized in the following Section.

4.1.0.1 State-of-the-art in Control of ES

In its maiden article [6], the control of ES has been employed using a PI controller. The δ-control [47], has been executed using a Proportional Resonant (PR) controller (a modified version of a PI controller) and asks for the precise parametric values of the system, which practically are not known in advance, due to parametric and load excursions. Radial-chordal decomposition (RCD) [101] using a PI controller has been used as a controller to calculate the v_{es} on a real-time basis and is quite cumbersome to be executed by a low-cost controller. The simple Power Decoupling (SPD) method [102] has also been executed using a PI controller, and it also requires having the precise knowledge of system parameters in advance. The internal model principle (IMP) using a quasi-PR controller has been proposed in a repetitive control [103], wherein precise information about the system's model and system frequency is a must and is causing the delay in the control. Looking at the state-of-art, it is evident that control of ES has been carried out using a PI controller, in one way or another. It has been decided to start working on the control aspect of ES using a conventional PI control and hence its design.

4.2 Control of Electric Spring using a PI Controller

PI controller has been the most fundamental and widely used controller for the control of any system. It is being used for the reason that it offers reasonable control with ease, efficiency, and simplicity in the design. A grid-tied inverter, requires tracking the grid voltage phase, and hence an E-PLL structure presented in the Sec: 3.6.3 of Chapter:3, has been employed to extract the phase of the grid voltage for generating the sinusoidal command reference for the control of ES. The PI controller design is crucial for accurate

and efficient control of the ES. Pole placement technique using Loop-Shaping technique [95] employing root-locus, and Bode-plot has been deployed to carry out a PI controller design.

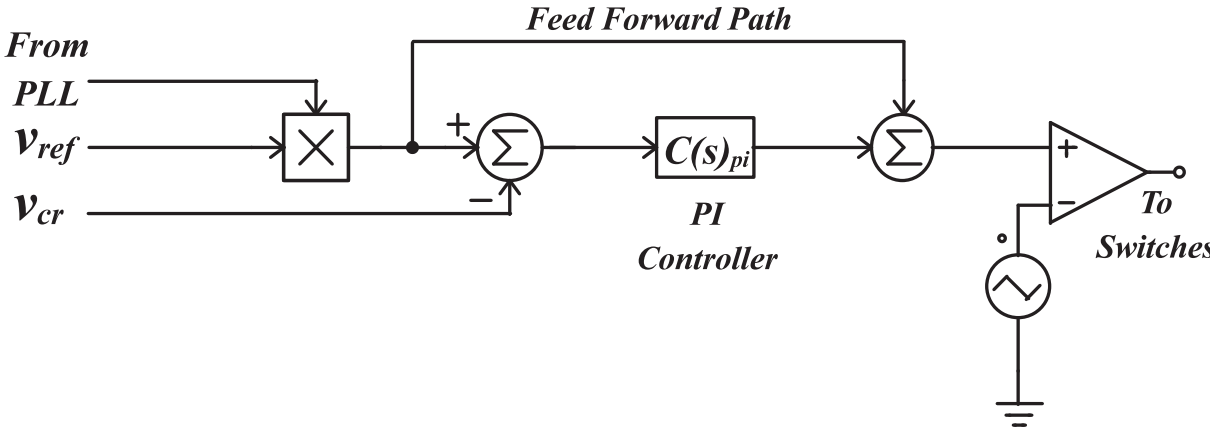

Figure 4.1: Control Block of ES Employing PI Controller.

4.2.1 Design of PI Controller

Mathematical model of the system of ES, derived in the Sec:2.4.2 of Chapter:2, has been used for the derivation of the PI controller using Loop-shaping technique by pole placement method [95]. The derived model in (2.7) is a $MIMO$ system, and hence it has been transformed into a $SISO$ system by applying following considerate assumptions:

- The disturbance input v_g is assumed to be stable, and hence its presence could be neglected. This assumption leads to a system with a single input that is a control input u (which ultimately has been driving the four switches of VSC through $U_1...U_4$) only.
- A single output, in the form of v_{cr}, has been considered for the reason that it is the quantity to be controlled, and hence it is of paramount interest.

These assumption lead to the development of a $SISO$ system, to be controlled through u. Thus simplified model can be represented as:

$$\begin{aligned} \dot{x(t)} &= A.x(t) + B.v_a(t), \\ y(t) &= C.x(t) + D.U(t), \\ \begin{bmatrix} \dot{x(t)} \\ y(t) \end{bmatrix} &= \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} x(t) \\ U(t) \end{bmatrix} \end{aligned} \tag{4.1}$$

The A, B, C and D parameter of the modeled system are:

$$\begin{aligned} A &= \begin{bmatrix} -\frac{1}{C_f(R_c+R_{NC})} & -\frac{1}{C_f} & \frac{R_c}{C_f(R_c+R_{NC})} \\ \frac{1}{L_f} & 0 & 0 \\ -\frac{R_c}{L_g(R_c+R_{NC})} & 0 & -\frac{R_cR_{NC}}{L_g(R_c+R_{NC})} \end{bmatrix} = \begin{bmatrix} -1.89e4 & -1.67e5 & 1.25e5 \\ 500 & 0 & 0 \\ -2459 & 0 & -7049 \end{bmatrix}, \\ B &= \begin{bmatrix} 0 \\ \frac{1}{L_f} \\ 0 \end{bmatrix} = \begin{bmatrix} 0 \\ 500 \\ 0 \end{bmatrix}, \\ C &= \begin{bmatrix} \frac{R_c}{(R_c+R_{NC})} & 0 & \frac{R_cR_{NC}}{(R_c+R_{NC})} \end{bmatrix} = \begin{bmatrix} 0.75 & 0 & 1.65 \end{bmatrix}, \\ D &= \begin{bmatrix} 0 \end{bmatrix} \end{aligned} \tag{4.2}$$

Where,

$x(t) = [v_{es}(t) \quad i_f(t) \quad i_g(t)]^T$,
$U(t) = [v_a(t)]$,
$u(t) = m.sin(\omega t + \theta)$, is the control input,
$v_a(t) \cong E_o.u(t)$ (assuming that higher order harmonics are absent),
m, modulation index of the converter,
$e(t) = v_g(t) = V_m.sin(\omega t)$, the disturbance input,
$y(t) = v_{cr}(t)$, voltage across the critical load
ω, angular velocity of v_g.

This derived model of ES (4.2) has been validated through the Matlab (function power_analyze() and corresponding Simulink model). This model has been transformed into the transfer function as:

$$G(s) = \frac{v_{cr}}{u} = C(sI - A)^{-1}B + D \tag{4.3}$$

$$= \frac{6.25 \times 10^7 s + 1.025 \times 10^{11}}{s^3 + 2.599 \times 10^4 s^2 + 5.242 \times 10^8 s + 5.874 \times 10^{11}} \tag{4.4}$$

This transfer function (4.4) has been used further to derive the PI controller being deployed for the control of ES.

Poles of the system can be placed to a desired location so as to get the desired control over a system, by setting the goals of the controller design. The design goals, of Settling time $t_s \leq 10ms$, Gain margin $G.M \geq 100db$ and Phase Margin $P.M \geq 60°$, has been set aside for the efficient control of ES. Control block of PI implementation can be seen form Figure. 4.1, where in $C(s)_{pi}$ represents a PI controller. A feed forward compensation has been added [71], to avert the impact of transients and to achieve smooth transition at the advent of load change and ever changing grid conditions. Implementing set aside design goals, using Matlab function "systune()", constants of the PI controller $C(s)_{pi}$ have been found as:

$$C(s)_{pi} = K_p + \frac{K_i}{s} \tag{4.5}$$

having,

$K_p = 3.35$, and $K_i = 6.18K$

Inculcating the (4.5) to control the system of ES, the loop gain can be derived as:

$$\ell(s)_{pi} = \frac{2.091 \times 10^8 s^2 + 7.287 \times 10^{11} s + 6.327 \times 10^{14}}{s^4 + 2.599 \times 10^4 s^3 + 5.242 \times 10^8 s^2 + 5.874 \times 10^{11} s} \tag{4.6}$$

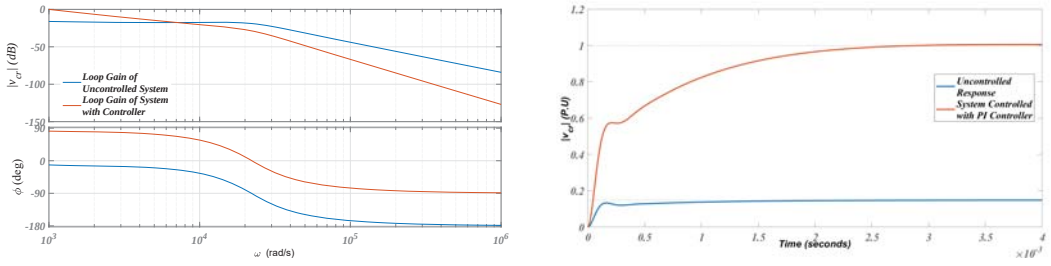

Figure 4.2: Frequency Response Plot and Step Response of System of ES Employing PI Controller.

Bode plot of (4.6) gives, $infinite\ dB$ of GM and PM of 109° at $1.11e+3\ rad/s$. Settling time, $t_s < 5ms$ can be depicted from the step response plot. Bode Plot and step response (Figure. 4.2), signifies the satisfactory achievement of the set aside design goals.

4.2.2 Result Analysis of PI Controlled ES

Satisfactory compliance of the PI controlled ES to the standard test input, i.e., step input, has provided the needed motivation to implement the designed controller (4.5), so as to execute the control of the system of ES, as has been presented in Fig: 2.14 of Chapter: 2. The control block can be depicted in Fig:4.1. The E-PLL structure derived in Sec: 3.6.3 of Chapter:3, has been tested with this construct to get the controller's output, getting synchronized with the grid voltage (v_g). The performance of the PI-controlled system can be evaluated through Table:4.1, and from the Fig:4.3 through Fig:4.9. Well regulated v_{cr} (from Fig:4.3) in the presence of perturbing v_g,v_{nc},v_{es},i_g,i_{nc}, and i_{cr} confirms the efficacy of the PI controlled ES.

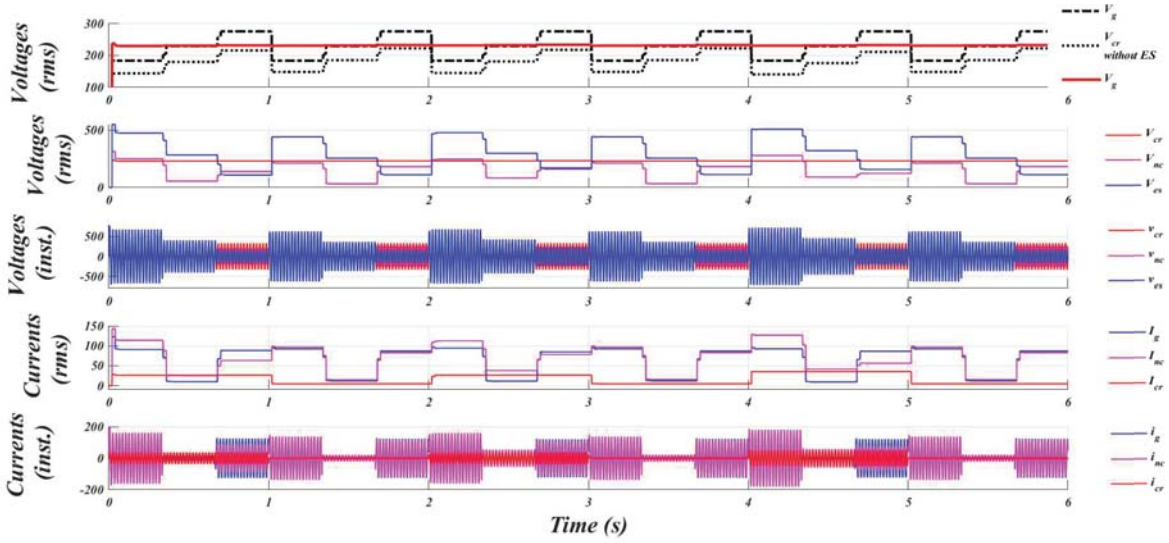

Figure 4.3: Instantaneous and RMS Variations in the System Parameters at the Wake of Step Changes in Load and Grid Voltage.

A grid voltage ($v_g = 230 \pm 20\%$) has been supplied to the load by the feeder, possessing an impedance ($Z_g = 0.5 + j0.1\Omega$) and this is causing a voltage drop (of around 20%) across it. The variation in the load and grid voltage has been mentioned in the Table:4.1 with corresponding time interval. ES has been operating either in the capacitive mode or in the

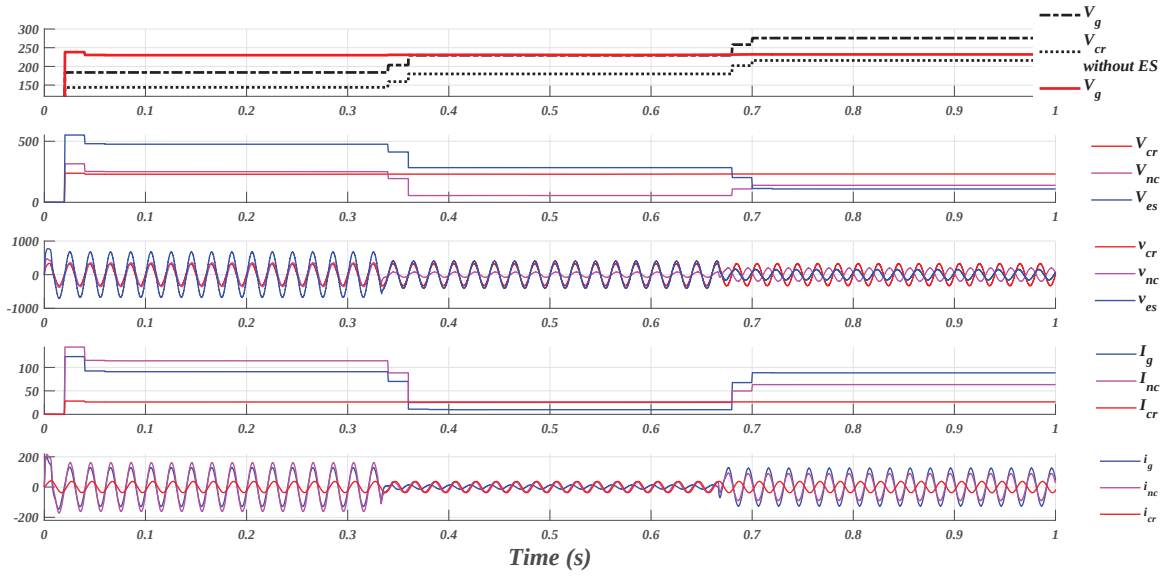

Figure 4.4: Instantaneous and RMS Variations in the System Parameters with R_1-L Load, at the Wake of Step Change in v_g.

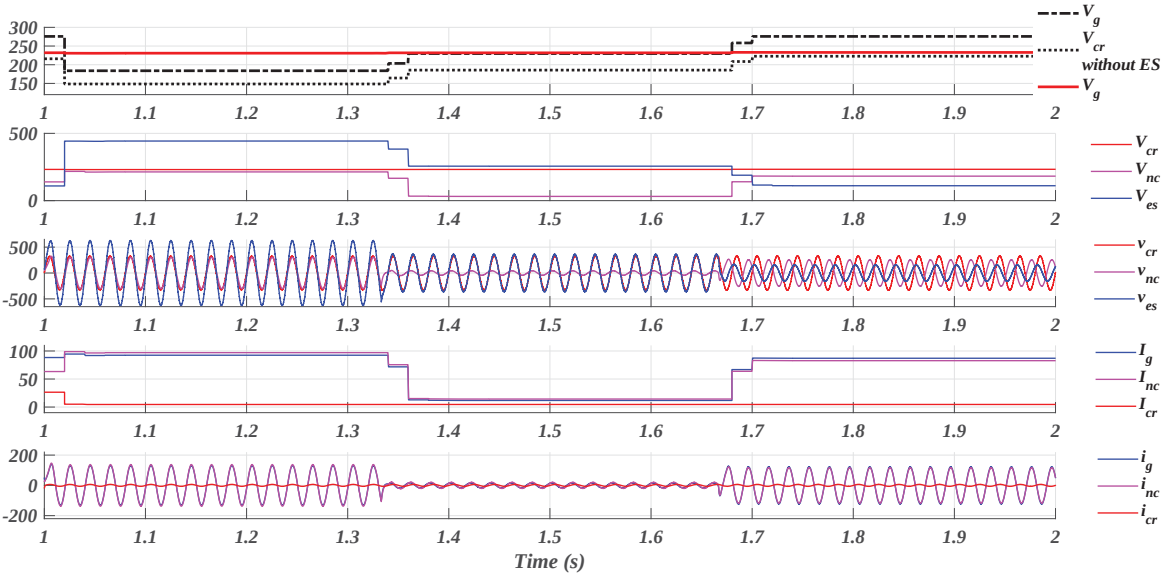

Figure 4.5: Instantaneous and RMS Variations in the System Parameters with R_2-L Load, at the Wake of Step Change in v_g.

inductive mode, by absorbing the excess voltage or by recuperating the deficit. A nicely regulated constant voltage (v_{cr}) across the critical load has been the end result of the judicious voltage regulating function of the PI-controlled ES. The lowest regulation that

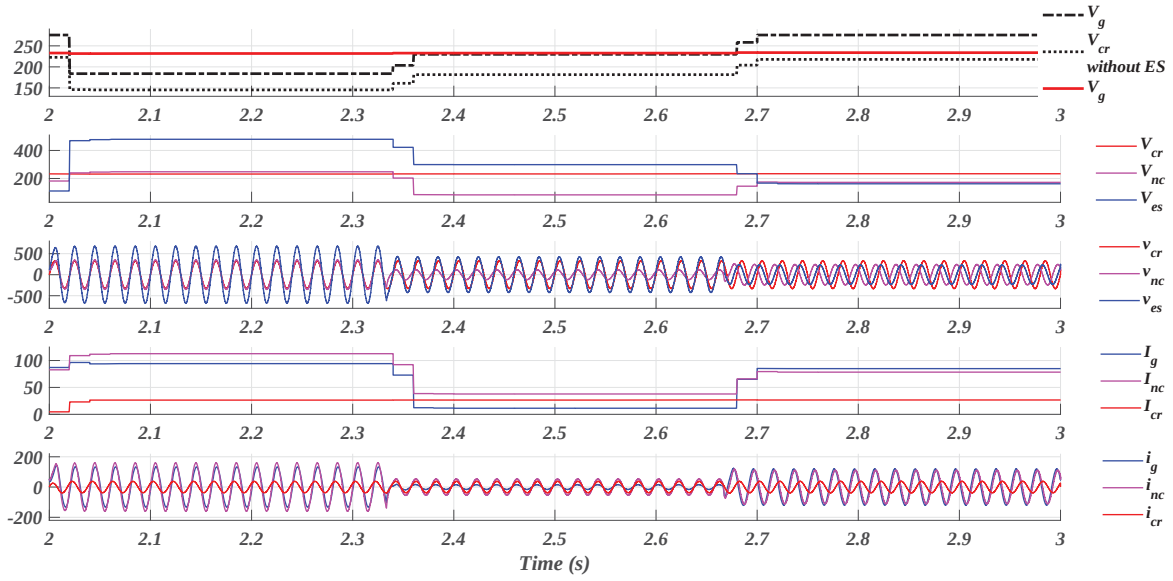

Figure 4.6: Instantaneous and RMS Variations in the System Parameters with R_1-C Load, at the Wake of Step Change in v_g.

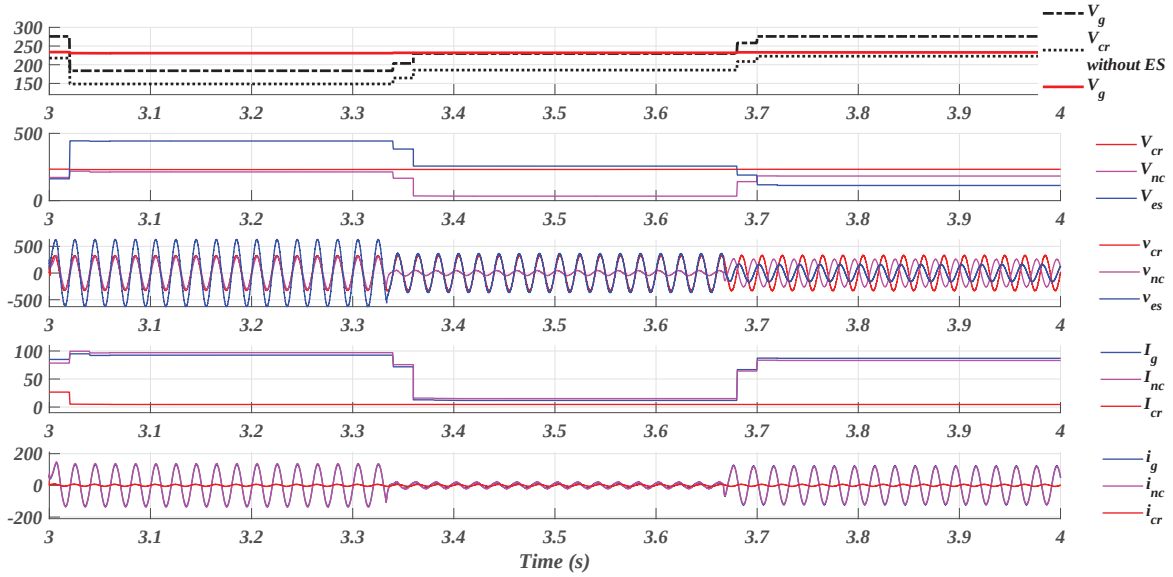

Figure 4.7: Instantaneous and RMS Variations in the System Parameters with R_2-C Load, at the Wake of Step Change in v_g.

could be noticed is of the order of 1.75% and the corresponding value of $v_{cr} = 233.82V$. This is simply validating and confirming the designed PI controller's test results, which have been achieved through the step response plot (Fig:4.2).

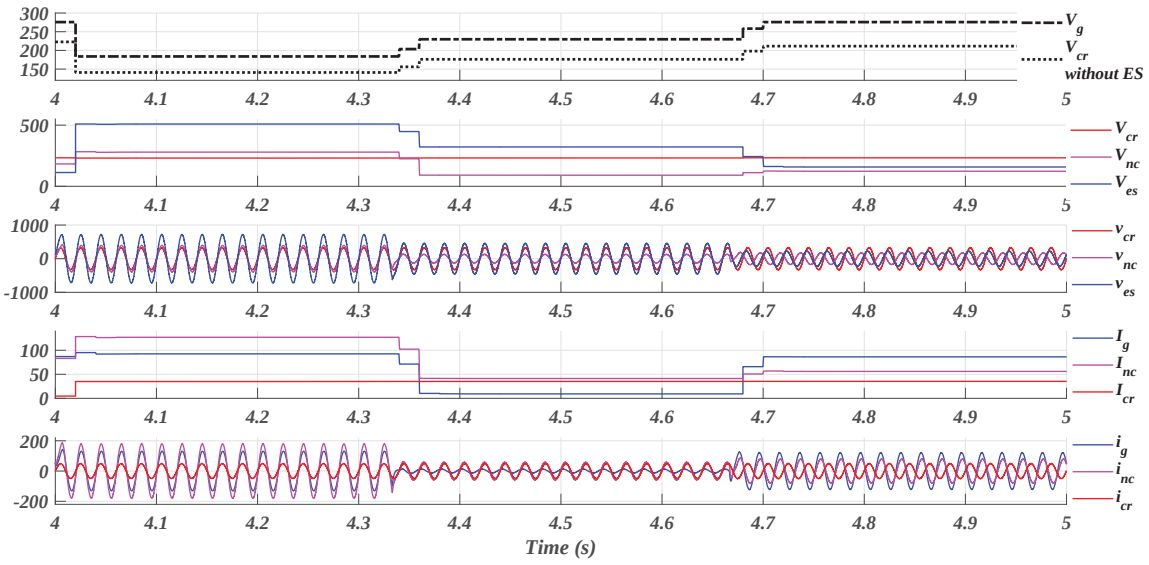

Figure 4.8: Instantaneous and RMS Variations in the System Parameters with R_1 Load, at the Wake of Step Change in v_g.

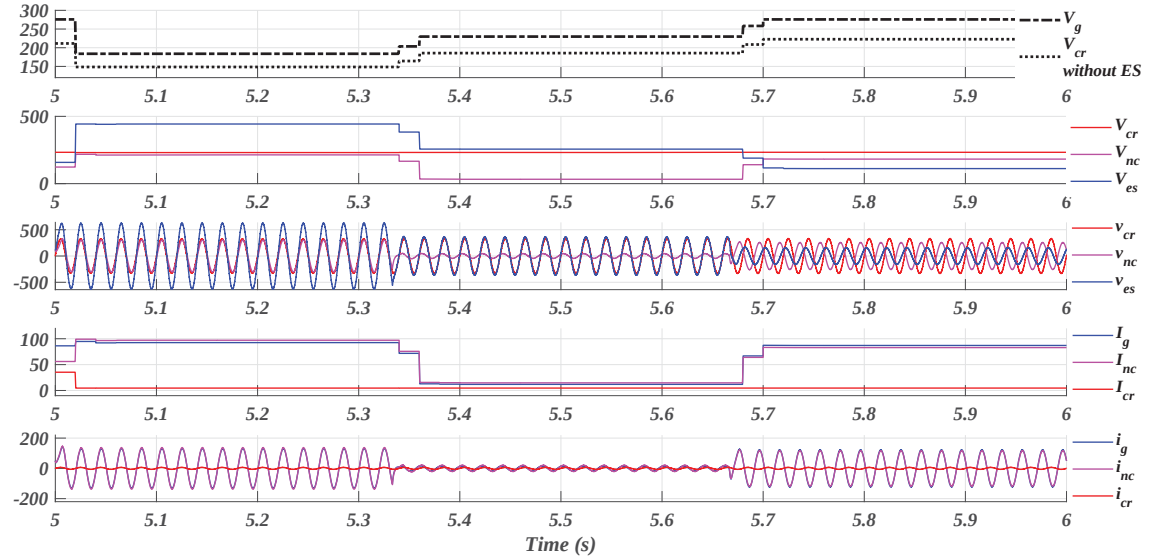

Figure 4.9: Instantaneous and RMS Variations in the System Parameters with R_2 Load, at the Wake of Step Change in v_g.

Fig:4.3 through Fig:4.9 shows the variation in the system parameters pertaining to the specific critical load. The current I_{cr} is maintained constant for a typical load even in the presence of varying v_g, which otherwise would vary in the absence of ES (as can be

Table 4.1: Results Assimilated from the Test Bench of PI Controlled ES

$Time(s)$	$Load(\Omega)$	V_g **(V)**	$V_{nc}(V)$	$V_{es}(V)$	$I_g(A)$	$I_{nc}(A)$	$I_{cr}(A)$	$I_{inv}(A)$	$Power(W)$	$V_{cr}(V)$	% Reg. of V_{cr}
0.00-0.33	6.6 + j5.78	183.85	250.85	475.94	90.82	114.02	26.24	113.98	20273.30	230.11	0.05
0.33-0.66	6.6 + j5.78	229.81	55.63	284.53	10.53	25.28	26.34	25.30	973.42	231.05	0.46
0.66-1.00	6.6 + j5.78	275.77	139.80	109.96	88.62	63.55	26.45	63.77	-18525.10	232.09	0.91
1.00-1.33	50 + j5.78	183.85	213.58	443.18	92.50	97.08	4.59	97.12	20769.20	230.95	0.41
1.33-1.66	50 + j5.78	229.81	33.28	257.25	12.65	15.13	4.61	15.66	1485.48	232.00	0.87
1.66-2.00	50 + j5.78	275.77	182.45	111.95	87.25	82.93	4.63	83.19	-18089.30	232.96	1.29
2.00-2.33	6.6 - j5.78	183.85	248.17	479.99	94.25	112.80	26.43	112.89	21207.10	231.84	0.80
2.33-2.66	6.6 - j5.78	229.81	84.46	299.56	11.94	38.39	26.54	38.80	1792.19	232.82	1.23
2.66-3.00	6.6 - j5.78	275.77	173.21	163.50	85.08	78.73	26.66	79.08	-17831.80	233.84	1.67
3.00-3.33	50 - j5.78	183.85	213.45	443.28	92.60	97.02	4.59	97.06	20796.50	231.00	0.43
3.33-3.66	50 - j5.78	229.81	35.07	257.75	12.70	15.94	4.61	16.48	1510.71	232.05	0.89
3.66-4.00	50 - j5.78	275.77	183.31	113.91	87.14	83.32	4.63	83.58	-18066.80	233.01	1.31
4.00-4.33	6.6 + j0.00	183.85	279.69	509.57	92.55	127.13	35.00	127.12	20697.80	230.97	0.42
4.33-4.66	6.6 + j0.00	229.81	91.34	322.00	9.76	41.52	35.13	41.71	1292.36	231.88	0.82
4.66-5.00	6.6 + j0.00	275.77	123.79	159.12	86.38	56.27	35.29	56.60	-18250.60	232.94	1.28
5.00-5.33	50 + j0.00	183.85	213.65	443.37	92.55	97.12	4.62	97.15	20784.10	230.97	0.42
5.33-5.66	50 + j0.00	229.81	34.25	257.62	12.67	15.57	4.64	16.10	1497.19	232.02	0.88
5.66-6.00	50 + j0.00	275.77	182.76	113.02	87.20	83.07	4.66	83.33	-18077.70	232.98	1.30

seen verified from the Fig:4.4 through Fig:4.9, and from Table:4.1) due to the enhanced support of smart load (depicting more number of alterations in v_{nc} and v_{es}).

4.3 Cascade Control of Electric Spring

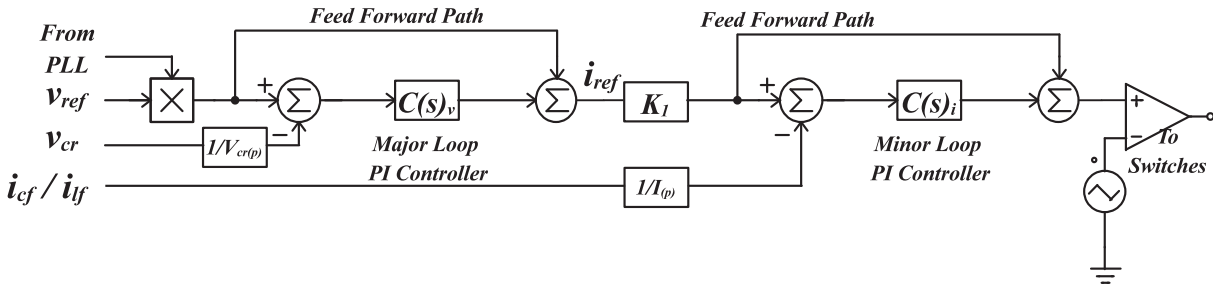

Figure 4.10: Control Block of ES Employing Loop-in-Loop Controller.

Performance improvisation, in terms of stability and dynamics, in the presence of frequent step changes taking place in load and grid voltage, can be achieved effectively employing multi-loop control strategies [104]. Numerous multi-loop control strategies

have been presented in the technical literature. Electric spring is essentially a current-controlled voltage source converter [6], and the performance of VSC acting as ES can be improvised by having a check on the current flowing through it. Loop-in-loop control employing two loops connected in cascade, the minor/inner one dedicated to current control and the outer/major one devoted to the conventional voltage control, can be depicted from Fig:4.10. The voltage feedback of v_{cr} being compared with the sinusoidal reference v_{ref} generates an error (value of the same is to be reduced to zero) which is acting as the input to the $C(s)_v$ controller. The output of the $C(s)_v$ is acting as a reference signal (I_{ref}) for the inner loop, being compared with the feedback conventionally taken from the current signal. The feedback for the inner current loop could be derived either from, (i) filtering inductor (i_{lf}) of VSC, or (ii) filtering capacitor (i_{cf}) of VSC. The output of the outer voltage-controlled loop generates the error and drives the inner loop's PI controller ($C(s)_i$). The generated output is the ultimate control signal which is responsible for driving the switches of ES to regulate the voltage of the critical load (v_{cr}) with a check on the i_{inv}/i_{lf}. The minor loop ensures faster dynamic response, further ascertaining the system's faster dynamic performance and acting in cascade with the outer voltage loop, and provides robustness against the step changes. The inculcation of a minor current control loop in the conventional feedback control provides an additional degree of freedom in the control structure. SOGI-PLL structure, presented in Sec: 3.6.2 of Chapter:3, has been tried with both the configurations of cascaded PI control of ES for the extraction of the phase of the v_g and to synchronize the output of ES. The intention of employing SOGI-PLL with cascade control is to verify the performance of its design.

4.3.1 Design of PI Controllers used for the Cascaded Control of ES

The control mechanism is employed to execute cascaded control through the control block shown in Fig: 4.10. Two PI controller, as can be seen from the control block, have been designed here using loop shaping technique mentioned in the Section:4.2.1.

The controller $C(s)_i$ of inner current control loop has been designed with of 20° having cross over frequency of 4.5KHz. The controller so designed is represented by,

$$C(s)_i = 1.516 + \frac{4.94e4}{s} \tag{4.7}$$

The controller $C(s)_v$ of outer voltage control loop has been designed with a slightly higher phase margin phase margin of 30° having cross over frequency of 2.25KHz (half the frequency of $C(s)_i$). The controller so designed is,

$$C(s)_v = 0.9679 + \frac{2.965e04}{s} \tag{4.8}$$

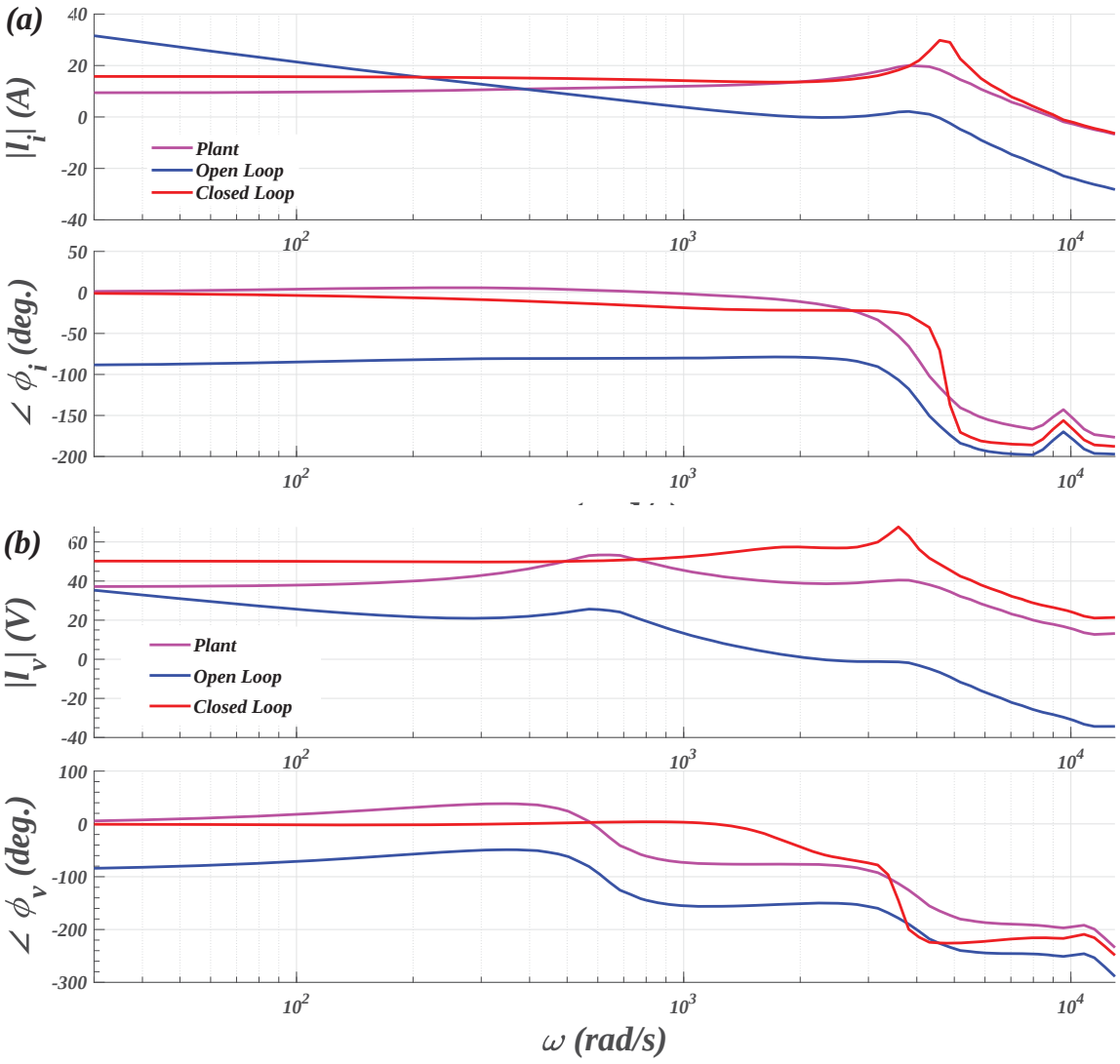

Figure 4.11: Frequency Response Plots of the loop gains employing (a) PI_i, (b) PI_v Controllers

The conventional mechanism of feedback signal extracted in the form of i_{lf}, for the minor loop, needs larger currents to be sensed by the current sensing element. Another approach is to get the current feedback for the inner loop from the current flowing through

the filtering capacitor C_f, i.e., i_{cf} which happens to be less. This method of extracting the feedback has been advocated in many research publications [105]. Results available from both the types of feedback (received from i_{lf} and i_{cf}) have been presented in the sections to follow.

The frequency response plot of the designed controllers in the open-loop and the closed-loop can be depicted from the Fig:4.11(a) and Fig:4.11(b), showing nice and flat responses with sufficient gains and bandwidth.

4.3.2 Results of Cascaded PI Controlled ES

Loop-in-Loop control of ES has been tried on the test bench presented in Fig: 2.14, using both the mentioned feedback mechanisms (feedback through i_{lf} and i_{cf}) of inner loop's current feedback. Results associated with cascade controlled ES, deploying i_{lf} and i_{cf} as feedback, have been presented in Table:4.2. Performance of the cascaded PI-control strategy executed using i_{lf} has been presented through the plots showing the variation in parameters can be depicted from Fig:4.12. Entire result spectrum has been fragmented into six groups, in accordance with the load change, at the instances mentioned in the Table:4.2 and corresponding Fig:4.13 through Fig:4.18. Each fragment carries a specific load type under the influence of all the scenarios of grid perturbation of $v_{ref} \pm 20\%$.

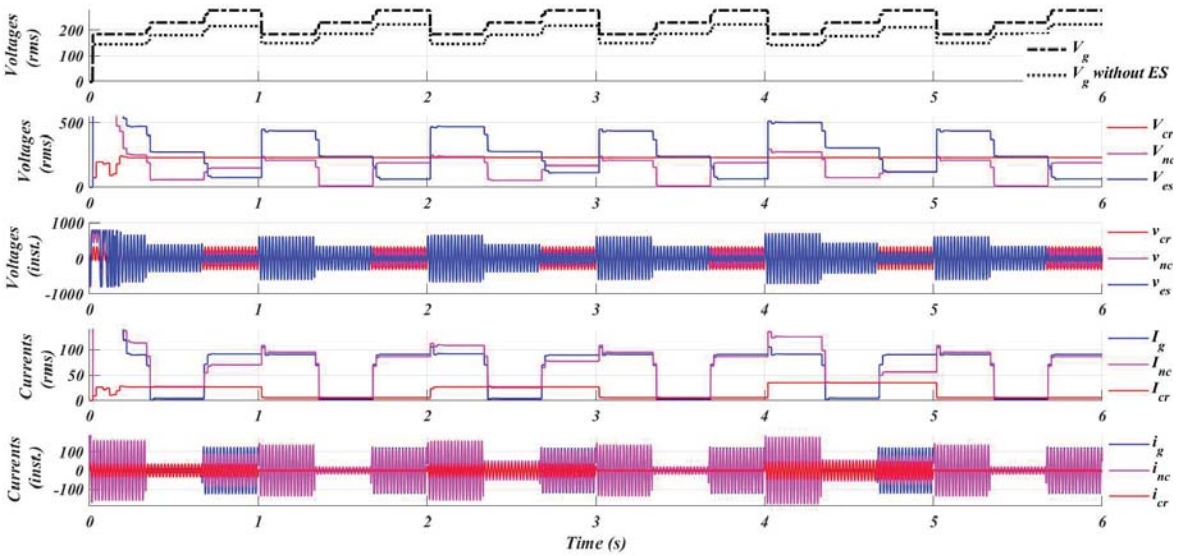

Figure 4.12: Results of Cascade Control having Step Changes Applied to v_g and Load.

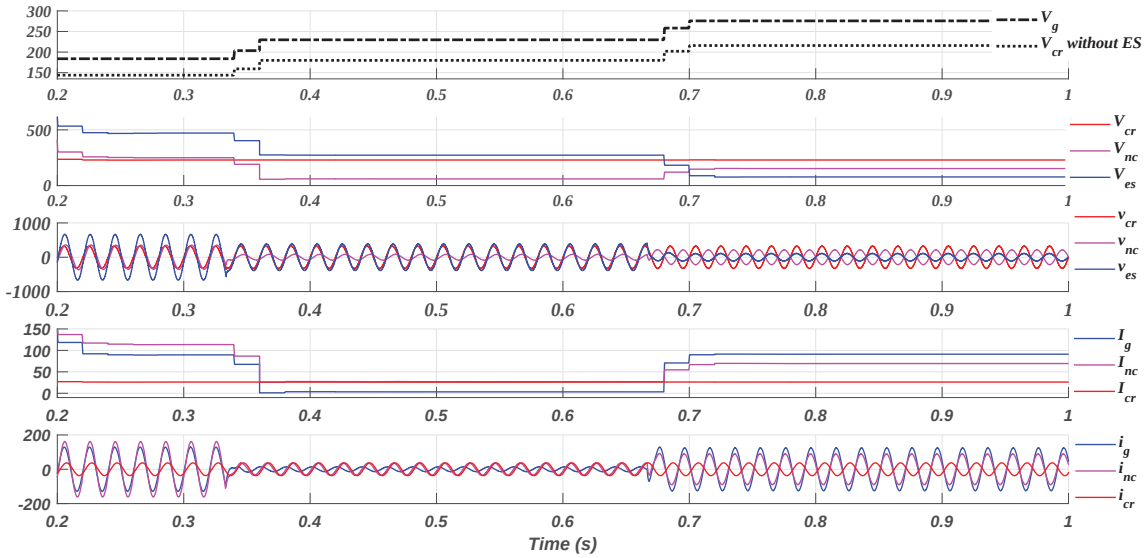

Figure 4.13: Results of Cascade Control having Step Changes in v_{cr}, for R_1-L Load.

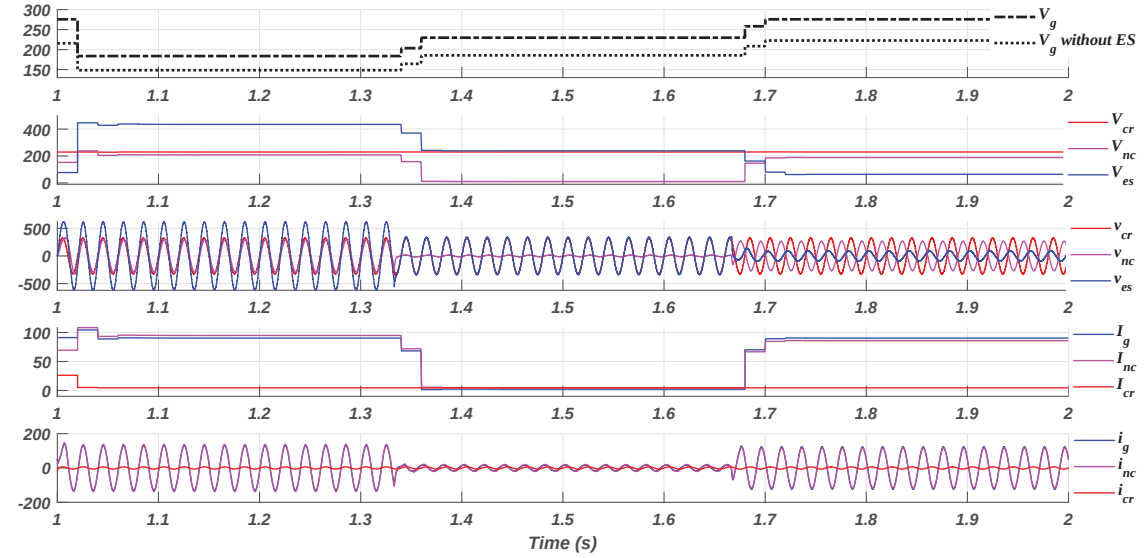

Figure 4.14: Results of Cascade Control having Step Changes in v_{cr}, for R_2-L Load.

A well regulated v_{cr} can be seen from results, justifying the appropriateness of the designed PI controllers for the application of ES.

Results of cascaded PI-control using feedback from i_{cf} have been compared with that of i_{lf}. The comparison can be seen from Fig:4.19 and Fig:4.20, and from Table:4.3. Worst regulation in the case of feedback from i_{cf} is 0.28%, and the best one is 0.02%, and the corresponding regulation form i_{lf} is 0.33%, and 0.01%. The results reveal that the voltage regulating the action of cascaded PI-controlled ES in both the variants is

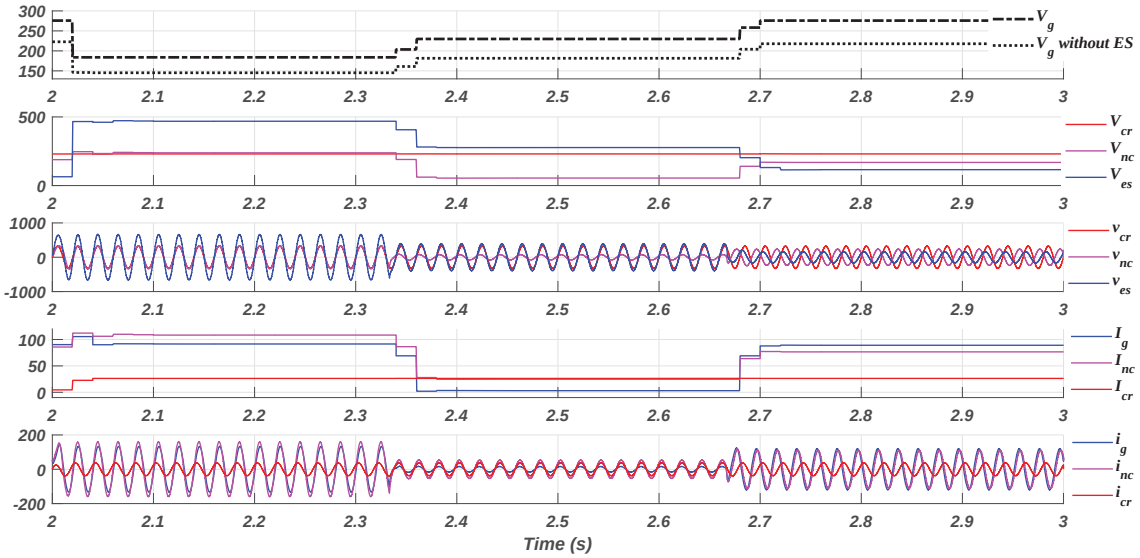

Figure 4.15: Results of Cascade Control having Step Changes in v_{cr}, for R_1-C Load.

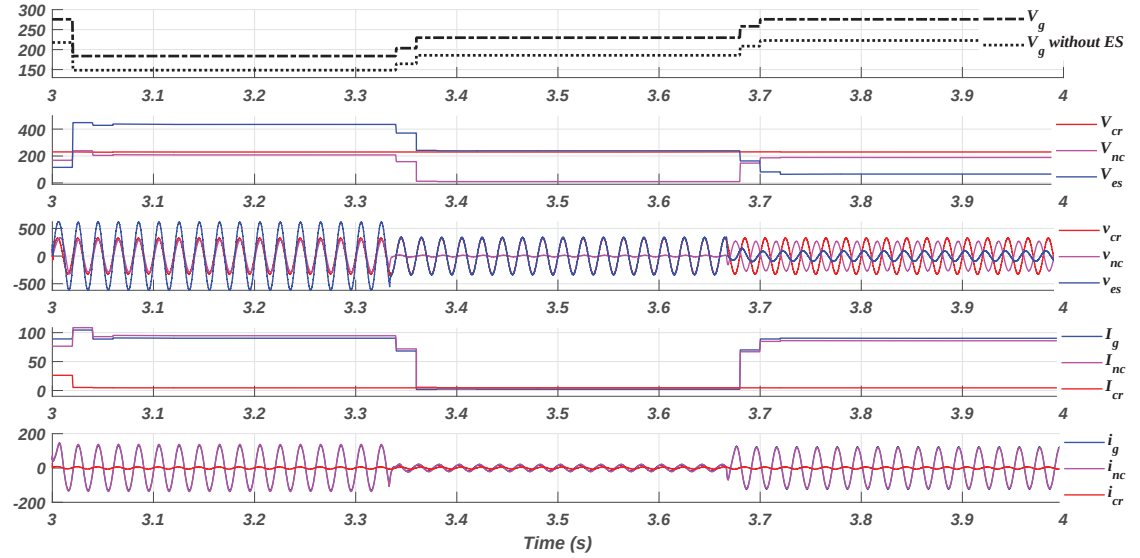

Figure 4.16: Results of Cascade Control having Step Changes in v_{cr}, for R_2-C Load.

executed with great efficacy. The voltage regulating abilities of the cascaded controller executed through the feedback form i_{cf}, show more accuracy and precision compared to that executed through the feedback form i_{lf} (seen in Fig:4.19). Table:4.3 and Fig:4.20 reveals almost a marginal difference in the performance of the cascaded controller being executed with these two different strategies. However, the feedback executed through i_{cf} works somewhat better and cost-effectively. The cost-effectiveness of strategy of feedback through i_{cf} can be proved from the variation of i_{cf} (largest variation has been under $3A$)

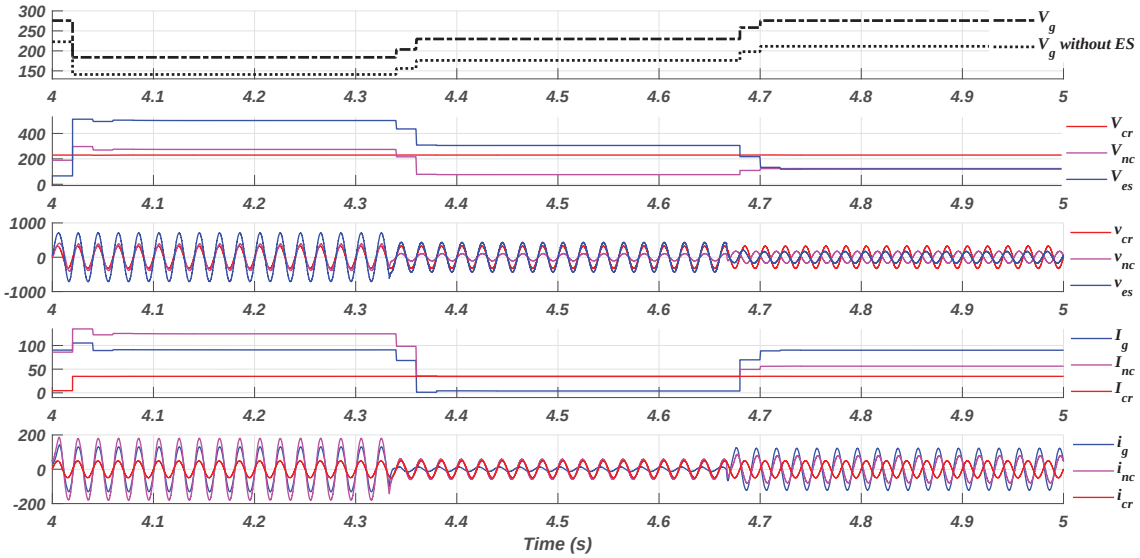

Figure 4.17: Results of Cascade Control having Step Changes in v_{cr}, for R_1 Load.

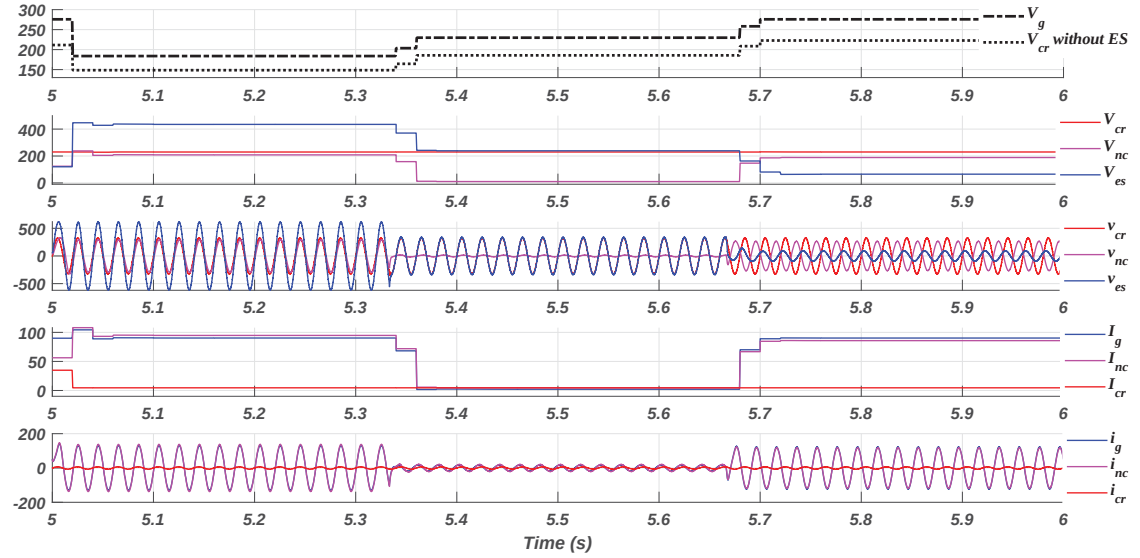

Figure 4.18: Results of Cascade Control having Step Changes in v_{cr}, for R_2 Load.

and i_{lf} (largest variation has been 300A considering the start-up transient, and little under $150A$ in steady-state) of the Fig:4.19. Larger current sensing element for the measurement of i_{lf} compared to that of i_{cf} requires costlier Hall-effect sensor, and corresponding signal stabilizing network.

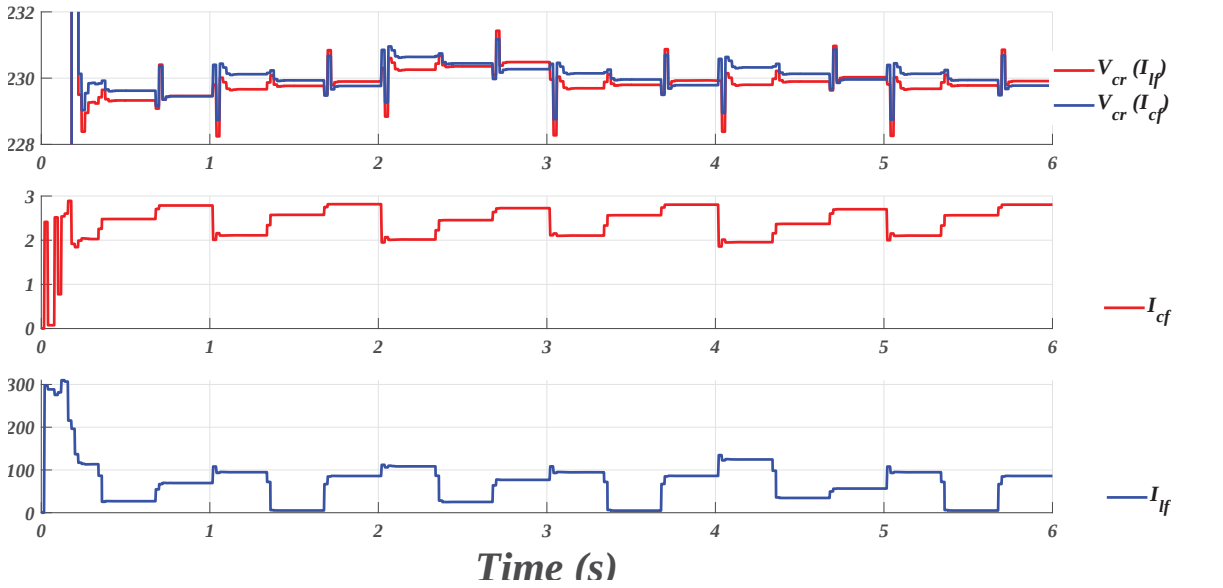

Figure 4.19: Performance Comparison of Cascade Control having feedback through i_{lf} and I_{cf} and Corresponding variation in i_{lf} and I_{cf}.

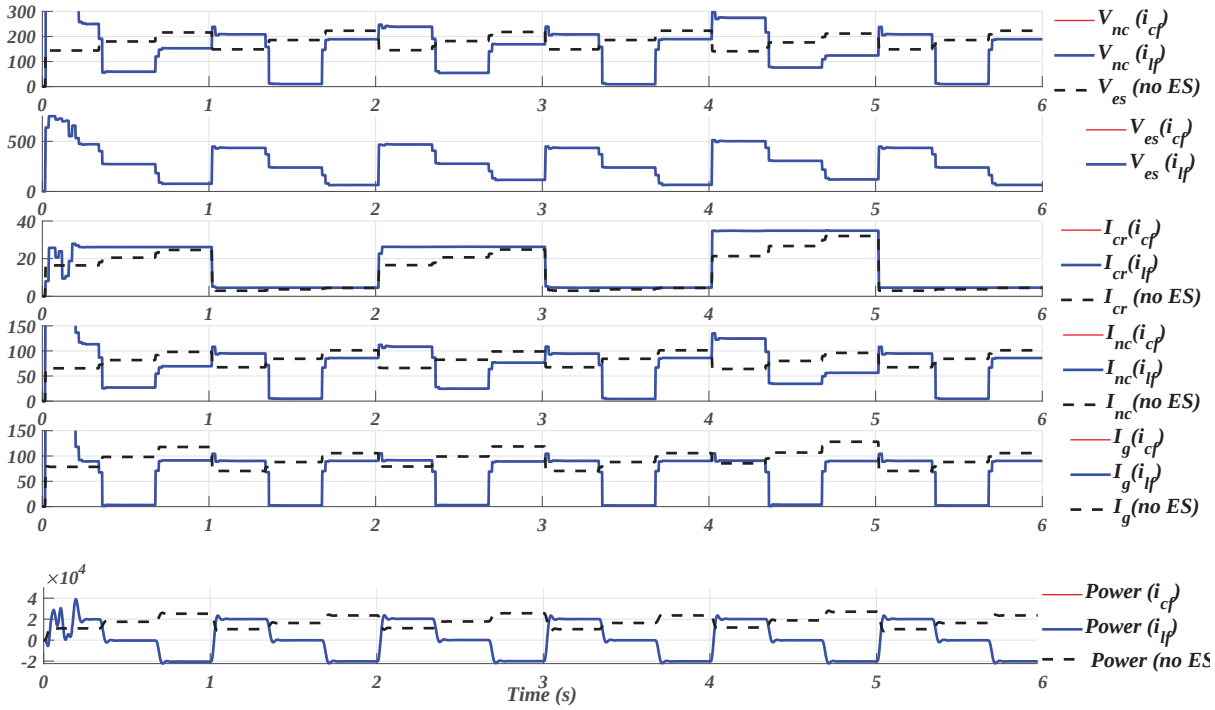

Figure 4.20: Comparison of Results of Cascade Control having feedback through I_{lf} and I_{cf}.

Table 4.2: Results of Cascade Controlled ES, having Current Feedback from I_{lf} and I_{cf}

Time (s)	Load (Ω)	V_g (V)	Feedback through I_{lf}									Feedback through I_{cf}								
			V_{nc} (V)	V_{es} (V)	I_{inv} (A)	I_g (A)	I_{nc} (A)	I_{cr} (A)	V_{cr} (V)	Power (W)	% Reg	V_{nc} (V)	I_{es} (A)	I_{inv} (A)	I_g (A)	I_{nc} (A)	I_{cr} (A)	V_{cr} (V)	Power (W)	% Reg
0.00-0.33	6.6 + j5.78	183.85	249.84	471.16	113.43	89.50	113.56	26.14	229.24	19442.11	-0.33	252.14	474.36	114.48	90.58	114.61	26.21	229.82	19778.26	-0.08
0.33-0.66	6.6 + j5.78	229.81	59.65	272.85	26.90	3.32	27.11	26.15	229.33	-365.44	-0.29	60.69	274.48	27.38	3.17	27.59	26.19	229.62	-234.09	-0.16
0.66-1.00	6.6 + j5.78	275.77	152.55	77.21	69.40	91.11	69.34	26.17	229.46	-20388.15	-0.23	152.96	76.62	69.59	91.10	69.53	26.17	229.45	-20436.78	-0.24
1.00-1.33	50 + j5.78	183.85	208.53	434.88	94.71	90.26	94.79	4.56	229.66	20037.90	-0.15	210.40	437.40	95.56	91.10	95.64	4.57	230.12	20307.34	0.05
1.33-1.66	50 + j5.78	229.81	10.52	238.66	5.18	2.14	4.78	4.56	229.77	-120.26	-0.10	11.24	239.52	5.47	2.21	5.11	4.57	229.93	-49.47	-0.03
1.66-2.00	50 + j5.78	275.77	188.64	64.08	85.89	90.28	85.75	4.57	229.90	-20177.61	-0.04	189.16	61.52	86.12	90.52	85.98	4.56	229.76	-20279.68	-0.10
2.00-2.33	6.6 - j5.78	183.85	238.43	468.50	108.37	91.49	108.38	26.25	230.25	20332.99	0.11	240.41	470.91	109.28	92.16	109.28	26.30	230.64	20577.71	0.28
2.33-2.66	6.6 - j5.78	229.81	54.53	276.73	25.15	3.07	24.79	26.26	230.35	115.04	0.15	55.36	277.43	25.53	2.82	25.16	26.27	230.45	169.62	0.19
2.66-3.00	6.6 - j5.78	275.77	168.41	115.70	76.81	89.08	76.55	26.28	230.48	-20003.54	0.21	168.77	113.46	76.96	89.48	76.71	26.25	230.27	-20116.88	0.12
3.00-3.33	50 - j5.78	183.85	208.12	434.78	94.52	90.33	94.60	4.56	229.69	20054.82	-0.13	209.98	437.29	95.38	91.15	95.45	4.57	230.14	20322.70	0.06
3.33-3.66	50 - j5.78	229.81	9.60	238.79	4.89	2.13	4.36	4.57	229.80	-105.40	-0.09	10.31	239.63	5.17	2.18	4.68	4.57	229.96	-35.63	-0.02
3.66-4.00	50 - j5.78	275.77	189.05	65.81	86.08	90.22	85.93	4.57	229.93	-20165.80	-0.03	189.56	63.23	86.31	90.47	86.16	4.57	229.79	-20269.08	-0.09
4.00-4.33	6.6 + j0.00	183.85	274.10	501.55	124.53	90.68	124.59	34.82	229.80	20059.89	-0.09	276.49	504.65	125.61	91.60	125.68	34.90	230.32	20379.57	0.14
4.33-4.66	6.6 + j0.00	229.81	75.88	305.42	34.52	3.92	34.49	34.83	229.90	-129.42	-0.04	77.03	306.87	35.05	3.53	35.01	34.87	230.13	-7.84	0.06
4.66-5.00	6.6 + j0.00	275.77	123.83	120.04	56.49	89.95	56.29	34.85	230.03	-20221.53	0.01	123.93	118.94	56.53	90.07	56.33	34.84	229.96	-20274.76	-0.02
5.00-5.33	50 + j0.00	183.85	208.45	434.96	94.67	90.30	94.75	4.59	229.68	20046.47	-0.14	210.32	437.48	95.53	91.13	95.60	4.60	230.13	20315.63	0.06
5.33-5.66	50 + j0.00	229.81	10.12	238.84	5.06	2.14	4.60	4.60	229.78	-113.97	-0.10	10.82	239.69	5.34	2.18	4.92	4.60	229.94	-43.44	-0.03
5.66-6.00	50 + j0.00	275.77	188.71	65.03	85.92	90.25	85.78	4.60	229.91	-20171.86	-0.04	189.22	62.47	86.15	90.49	86.01	4.60	229.77	-20274.10	-0.10

Table 4.3: Comparative Analysis through the Difference of the Results (I_{cf}-I_{lf}) of Cascade Controlled *ES*

Time (s)	Load (Ω)	V_g (V)	V_{nc} (V)	V_{es} (V)	I_{inv} (A)	I_g (A)	I_{nc} (A)	I_{cr} (A)	V_{cr} (V)	Power (W)	% Reg
0.00-0.33	6.6 + j5.78	183.85	2.30	3.20	1.05	1.08	1.05	0.07	0.58	336.14	0.25
0.33-0.66	6.6 + j5.78	229.81	1.04	1.63	0.48	-0.16	0.47	0.03	0.29	131.35	0.13
0.66-1.00	6.6 + j5.78	275.77	0.41	-0.59	0.18	-0.01	0.19	0.00	0.00	-48.64	0.00
1.00-1.33	50 + j5.78	183.85	1.88	2.52	0.86	0.84	0.85	0.01	0.46	269.44	0.20
1.33-1.66	50 + j5.78	229.81	0.72	0.86	0.29	0.07	0.33	0.00	0.17	70.80	0.07
1.66-2.00	50 + j5.78	275.77	0.52	-2.56	0.23	0.24	0.23	0.00	-0.13	-102.06	-0.06
2.00-2.33	6.6 - j5.78	183.85	1.98	2.42	0.90	0.67	0.90	0.04	0.39	244.73	0.17
2.33-2.66	6.6 - j5.78	229.81	0.83	0.70	0.38	-0.24	0.38	0.01	0.09	54.58	0.04
2.66-3.00	6.6 - j5.78	275.77	0.36	-2.25	0.16	0.40	0.16	-0.02	-0.21	-113.34	-0.09
3.00-3.33	50 - j5.78	183.85	1.87	2.51	0.85	0.83	0.85	0.01	0.45	267.88	0.20
3.33-3.66	50 - j5.78	229.81	0.70	0.84	0.28	0.05	0.32	0.00	0.16	69.78	0.07
3.66-4.00	50 - j5.78	275.77	0.51	-2.58	0.23	0.25	0.23	0.00	-0.14	-103.28	-0.06
4.00-4.33	6.6 + j0.00	183.85	2.38	3.10	1.09	0.93	1.08	0.08	0.52	319.68	0.23
4.33-4.66	6.6 + j0.00	229.81	1.15	1.45	0.53	-0.39	0.52	0.04	0.23	121.58	0.10
4.66-5.00	6.6 + j0.00	275.77	0.10	-1.10	0.04	0.12	0.04	-0.01	-0.07	-53.23	-0.03
5.00-5.33	50 + j0.00	183.85	1.87	2.52	0.85	0.83	0.85	0.01	0.45	269.17	0.20
5.33-5.66	50 + j0.00	229.81	0.70	0.85	0.28	0.04	0.32	0.00	0.16	70.53	0.07
5.66-6.00	50 + j0.00	275.77	0.51	-2.56	0.23	0.24	0.23	0.00	-0.14	-102.23	-0.06

Comparative Results of the two said feedback arrangements have been presented in the Table:4.3, in the form of difference of the corresponding parameter. Both the feedback mechanisms converge to similar and matching outcomes, showing a minimal difference, and same can also be depicted from Fig:4.20.

4.4 Comparison of the Results and Conclusion

Some eighteen distinct changes through the combination of variation in the v_g and load have been invoked in the form of step changes, can be visualized from Fig:4.21. Data pertaining to these variations can be seen from the Table:4.4 (scenario of operation of the system in the absence of *ES* has not been presented here, as it has already been presented in Table:2.3).

A review of the figures and data reveals the following facts:

- *PI* and Cascaded *PI* control strategies give good voltage regulating performance in the presence of perturbations in load and v_g, as far as the steady-state performance is concerned.

Table 4.4: Comparative Analysis of the Results of PI controlled and Cascade Controlled ES through Current Feedback using i_{lf} and i_{cf}

Time(s)	*Load (Ω)*	V_g *(V)*	I_{lf} *(A)*	I_{cf}*(A)*	I_g*(A)*		V_{cr}*(V)*			*% Reg. of* V_{cr}*(V)*		
							PI	*Cascade Control*		*PI*	*Cascade Control*	
					i_{cf} *as Feedback*	i_{lf} *as Feedback*	*Control*	i_{cf} *as Feedback*	i_{lf} *as Feedback*	*Control*	i_{cf} *as Feedback*	i_{lf} *as Feedback*
0.00-0.33	6.6 + j5.78	183.85	113.43	2.03	90.58	89.50	230.11	229.82	229.24	0.05	-0.08	-0.33
0.33-0.66	6.6 + j5.78	229.81	26.90	2.48	3.17	3.32	231.05	229.62	229.33	0.46	-0.16	-0.29
0.66-1.00	6.6 + j5.78	275.77	69.40	2.79	91.10	91.11	232.09	229.46	229.46	0.91	-0.24	-0.23
1.00-1.33	50 + j5.78	183.85	94.71	2.11	91.10	90.26	230.95	230.12	229.66	0.41	0.05	-0.15
1.33-1.66	50 + j5.78	229.81	5.18	2.57	2.21	2.14	232.00	229.93	229.77	0.87	-0.03	-0.10
1.66-2.00	50 + j5.78	275.77	85.89	2.82	90.52	90.28	232.96	229.76	229.90	1.29	-0.10	-0.04
2.00-2.33	6.6 - j5.78	183.85	108.37	2.02	92.16	91.49	231.84	230.64	230.26	0.80	0.28	0.11
2.33-2.66	6.6 - j5.78	229.81	25.15	2.45	2.82	3.07	232.82	230.45	230.35	1.23	0.19	0.15
2.66-3.00	6.6 - j5.78	275.77	76.81	2.73	89.48	89.08	233.84	230.27	230.49	1.67	0.12	0.21
3.00-3.33	50 - j5.78	183.85	94.52	2.10	91.15	90.33	231.00	230.14	229.69	0.43	0.06	-0.13
3.33-3.66	50 - j5.78	229.81	4.89	2.57	2.18	2.13	232.05	229.96	229.80	0.89	-0.02	-0.09
3.66-4.00	50 - j5.78	275.77	86.08	2.81	90.47	90.22	233.01	229.79	229.93	1.31	-0.09	-0.03
4.00-4.33	6.6 + j0.00	183.85	124.53	1.95	91.60	90.68	230.97	230.32	229.80	0.42	0.14	-0.09
4.33-4.66	6.6 + j0.00	229.81	34.52	2.37	3.53	3.92	231.88	230.13	229.90	0.82	0.06	-0.04
4.66-5.00	6.6 + j0.00	275.77	56.49	2.70	90.07	89.95	232.94	229.96	230.03	1.28	-0.02	0.01
5.00-5.33	50 + j0.00	183.85	94.67	2.10	91.13	90.30	230.97	230.13	229.68	0.42	0.06	-0.14
5.33-5.66	50 + j0.00	229.81	5.06	2.57	2.18	2.14	232.02	229.94	229.78	0.88	-0.03	-0.10
5.66-6.00	50 + j0.00	275.77	85.92	2.80	90.49	90.25	232.98	229.78	229.91	1.30	-0.10	-0.04

- Cascade control outperforms PI control of ES, with the least tracking error and better regulation of v_{cr}.

- Two PLL structures presented in Chapter:3 have been tested with both the control strategies (PI and Cascaded-PI control) presented here in this chapter. E-PLL has been used for deriving the phase information for PI-controlled ES, and SOGI-PLL for cascaded PI controlled ES.

  Following observations can be presented pertaining to these PLL implementations with ES:

  - E-PLL structure performs better than SOGI-PLL, as far as the start-up time is concerned. Synchronization of ES through E-PLL takes only one cycle, whereas SOGI-PLL achieves the same after 0.2s, i.e., 10 cycles. These results are simply in line with the concluded results of the PLL's, presented in Chapter:3.
  - Steady-state performances of the two PLL's are at par.

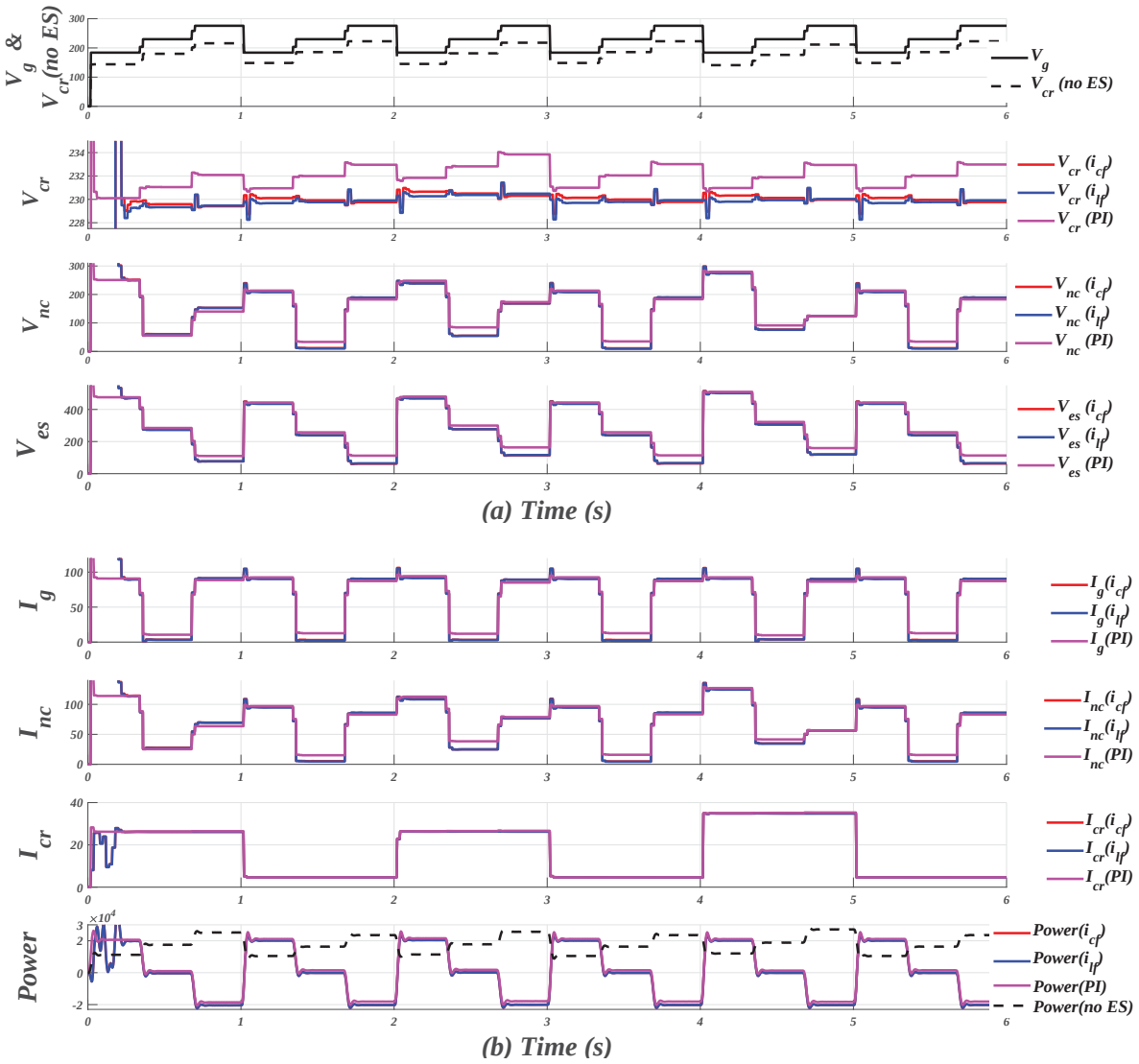

Figure 4.21: Comparison of Results, Achieved from Two Control Strategies, Pertaining to (a) Voltage Signals, (b) Current Signals and Power.

- Cascade control offers better voltage regulation with lesser and well-regulated inverter current (I_{inv}).
- Cascade control uses smaller DC-bus and hence smaller inverter output voltage (v_{es}).
- Above two points lead to the fact that cascade-controlled ES needs a smaller power rating of VSC for catering to the same load and grid conditions, and it performs better than PI-controlled ES. In other words, cascade-controlled ES offers better voltage regulation with lesser control effort and hence control energy.

- The maximum measured current flowing through I_{cf} is 2.82A compared to what has been flowing through is I_{lf} 124.53A (in steady state), and this shows a commendable reduction in the measured current and hence the cost of ES. Current flowing through I_{cf} is barely 2% of that flowing through I_{lf}.

Arguments presented above lead to a conclusion that a cascade controlled ES performs better then that using a single PI controller due to the additional degree of freedom available in the form of control of one more parameter i.e., either i_{inv} through i_{lf}, or i_{inv} and i_{nc} through i_{cf}, over and above the conventional control of voltage signal (v_{cr}) that has been present with both the control strategies of ES. The cascaded-PI controller could have a check on the i_{inv} through i_{lf} only, where as it could additionally regulate i_{nc} (and i_{inv}) through i_{cf}, and that has been the reason of better performance of cascade control executed through i_{cf}. The performance of cascaded-PI controlled ES (executed through the feedback of i_{cf}) proved cost effective by measuring only 2% current in the form of i_{cf} of that of i_{lf}.

This has further led to one more conclusion that the state-feedback control of ES with the observability of all the system's states might function even better.