Chapter 5

Control of Electric Spring: A Lead-Lag Controller Compensated Approach

5.1 Introduction

It is a classical frequency-domain control technique employed to get better steady-state accuracy by reducing the steady-state error due to the presence of *Lag* compensator. The large bandwidth and higher phase margin signifies faster response and good transient performance due to the inclusion of *Lead* compensation.

A *Lead* network satisfactorily complies to the specifications prescribed in the form of gain crossover frequency, or in other words, larger bandwidth, associated with robustness in control, against perturbations that leads to oscillatory response at the wake of transients and hence poor stability. Larger bandwidth and higher phase margin signify faster response speed and good transient performance, respectively, due to the inclusion of *Lead* compensator. A *Lead* compensator is designed through the Bode plot by adopting a philosophy wherein the phase plot is adjusted to get the desired phase merging at a stipulated gain crossover frequency without disturbing the magnitude plot, at the frequency of interest. The altered phase margin results in an unavoidable adversary in the form of altered gain crossover frequency required to be compensated by adding an appropriate phase shift through the phase margin, using an appropriate phase *Lead* compensator.

The limitations associated with increased bandwidth are that it makes the system susceptible to the noise, and higher frequency components go unattenuated, which causes attenuation in the performance of the system. Further, a *Lead* filter cannot alter the steady-state error.

Gain at low frequencies could be added, and the same can be reduced at high frequencies by introducing a *Lag* filter in the system, which causes a reduction in the steady-state error and improved stability.

The facts that has been discussed above, could be summarized [106] [95] [107] in the nutshell as,

- *Lead* compensator is to be used for improving stability margins.
- *Lag* compensator is used to improve the steady-state performance.
- *Lead* compensator achieves the desired result through the merits of its phase-lead contribution.
- *Lag* compensator accomplishes the result through the merits of its attenuation character at high frequencies.

A PI controller has been the most commonly used controller, in the available technical literature on ES, for the reason that it is simple to design and implement, but it altogether misses the accuracy and robustness, in following a sinusoidal reference, and the same has already been presented in the Chapter:4. Further, tracking of sinusoidal command with a PI controller introduces both, amplitude as well as angle error [95]. The introduction of angle and phase error has made us think of adapting a different control approach using loop shaping, known as *Lead-Lag* compensator [71].

This Chapter's prime objective is to present the *LeadLead-Lag* controller for the control of 1-ϕ ES, using Sinusoidal Pulse Width Modulation ($SPWM$) and Space Vector Modulation ($SVPWM$), as it offers excellent accuracy and robustness amidst the parametric variation and load excursions.

5.2 Control of Electric Spring using a *Lead-Lag* Controller

The state-space model (2.7) derived in Chapter:2, has been used to deduce the structure of the controller for controlling an ES.

The frequency response approach using loop shaping [95], through bode plot and root-locus, has been used for deriving the *Lead-Lag* controller [108] for the considered system of ES.

5.2.1 *Lead-Lag* Controller Design

Let the system given by (2.7), be represented by $G(s)$, and the controller, by $C(s)$. Its loop gain can be represented as,

$$\ell(s) = G(s) \times C(s) \tag{5.1}$$

$G(S)$ is subjected to track a sinusoidal command reference v_{ref},

$$v_{ref}(t) = V_m.sin(\omega t + \phi) \tag{5.2}$$

Steady-state response of sinusoidal command reference, while tracking v_{ref} through a closed-loop system having unity feedback, is represented by,

$$\frac{v_{ref}(t)}{v_s(t)} = V_m.sin(\omega t + \phi + \theta) \tag{5.3}$$

Where,

V_m is amplitude constant,

ϕ denotes the initial phase, and

θ is delay of sinusoidal command reference tracking, in the closed loop.

Steady-state error of the closed-loop system can be brought down to zero, if the magnitude of the loop-gain is made infinite at the frequency of the command reference. This has been achieved by adding a conjugate pair of poles at $(s \pm j\omega)$ in the controller, $C(s)$. To start with the design of a *Lead-Lag* controller, Let, $C(s)$ be:

$$C(s) = \frac{1}{s^2 + \omega^2} \tag{5.4}$$

Looking at the corresponding plot of Fig: 5.1, it is evident that loop gain, though it is

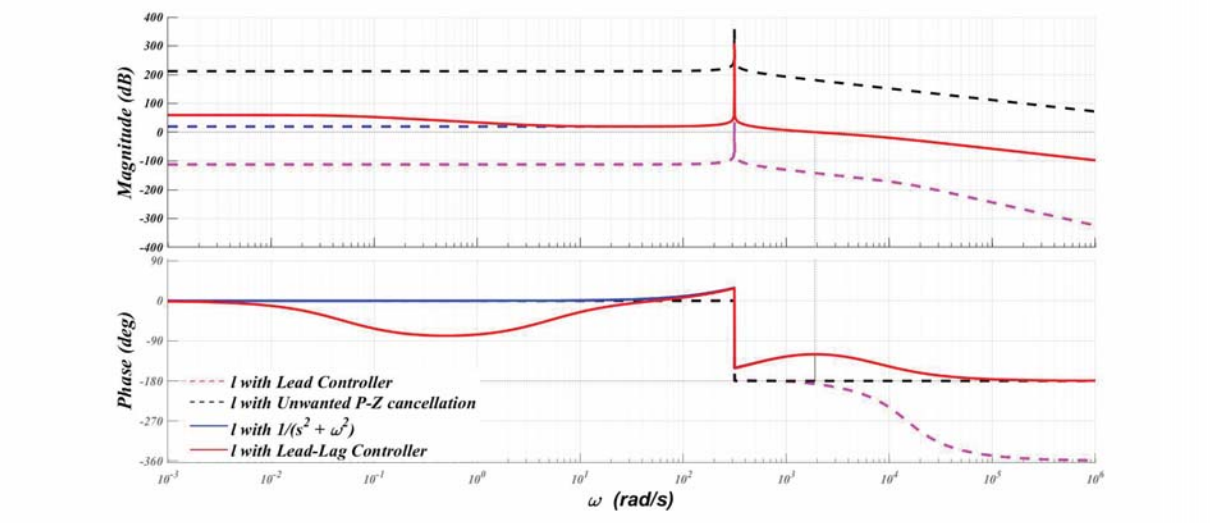

Figure 5.1: Frequency Response plot of *Lead-Lag* Controller, while Evolving through its Design.

small, is constant up to the resonant frequency of 314.15 rad/s, the corresponding phase continues to drop marginally by around 4°, and at resonance, it goes through a transition of −180°. This is an indication of an unstable system. For the stability of a closed-loop system, the phase of loop gain at the gain crossover frequency is to be made larger than −180°, also called phase margin. Further, looking at the same plot, at the points around the bandwidth (ω_b) of 2800 rad/s (around 9 to 10 times the ω) and corresponding cross over frequency (ω_c) of 1900 rad/s, the phase is found to be around −200°, which is yet another indication of an unstable closed-loop system.

Using (2.7), poles and zero of a system can be found as:

$Poles = [-1043; -10309.4 \pm 10548.5j)]$

$Zero = [-888.8]$

After cancellation of unstable poles and zeros, $C(s)$ (5.4) has been modified to,

$$C(s) = 6.25e07\frac{(s+1043)(s^2+2.062e04s+2.176e08)}{(s+888.9)(s^2+9.87e04)} \tag{5.5}$$

With the modified controller (5.5), the loop-gain (Fig: 5.1) can be seen to remain constant unto resonance. Then it continues to roll off at 20db/decade, the corresponding phase is zero unto resonance, and it goes through a transition of −180° after which it remains constant at −180°. This frequency response indicates an insufficient phase margin (zero) at ω_c. Hence, a *Lead* compensator has to be inculcated in the design of $C(s)$, to achieve

a considerate phase margin of around 60° at ω_c, leading to a desired steady-state and transient performance (having Peak overshoot $\leq 20\%$, steady-state (S.S.) error $\leq 10\%$ and settling time $\leq 10ms$).

The standard structure of the *Lead* compensator in [71], has been given as:

$$f_{Lead}(s) = \frac{s+z}{s+p} = \frac{s+(\frac{p}{\alpha})}{s+p} \tag{5.6}$$

for,

Maximum phase lead $\delta_{max} = 60° = sin^{-1}(\frac{\alpha-1}{\alpha+1})$, we can find
$\omega_c = \frac{p}{\sqrt{\alpha}}$, and $\alpha = 13.92$.

Substituting these values in (5.6), we get,

$$f_{Lead}(s) = \frac{s+509.1}{s+7091} \tag{5.7}$$

Inculcating (5.7) in (5.5), updates the overall transfer function of $C(s)$ as:

$$C(s) = 6.25e07\frac{(s+1043)(s^2+2.062e04s+2.176e08)}{(s+888.9)(s^2+9.87e04)} \times \frac{(s+509.1)}{(s+7091)} \tag{5.8}$$

Frequency response of the resulting loop gain ($\ell(s)$), shows a phase of $-120°$ and phase margin of 60° at ω_c (Fig: 5.1). The magnitude of $\ell(s)$ remains constant up to 314.15 rad/s. To make $\ell(s)$ larger at low frequency, a *Lag* filter has been introduced as part of the controller with,

$$f_{Lag}(s) = \frac{s+5}{s+0.05} \tag{5.9}$$

Incorporating (5.9) in (5.8), finally the controller has been evolved to,

$$C(s) = 6.25e07\frac{(s+1043)(s^2+2.062e04s+2.176e08)}{(s+888.9)(s^2+9.87e04)} \times \frac{(s+509.1)}{(s+7091)} \times \frac{(s+5)}{(s+0.05)} \tag{5.10}$$

Bode plot of the loop gain accommodating the final *Lead-Lag* controller (5.10), can be seen from the corresponding plot of Fig: 5.1, having $infinite\ G.M.$ and $P.M.\ of$ 59.9°.

Step response of the closed-loop system with unity feedback can be seen from the corresponding plot of Fig: 5.2, clearly satisfying all of the design precursors (having Peak overshoot of 20%, S.S. error of 3% and settling time of $5ms$).

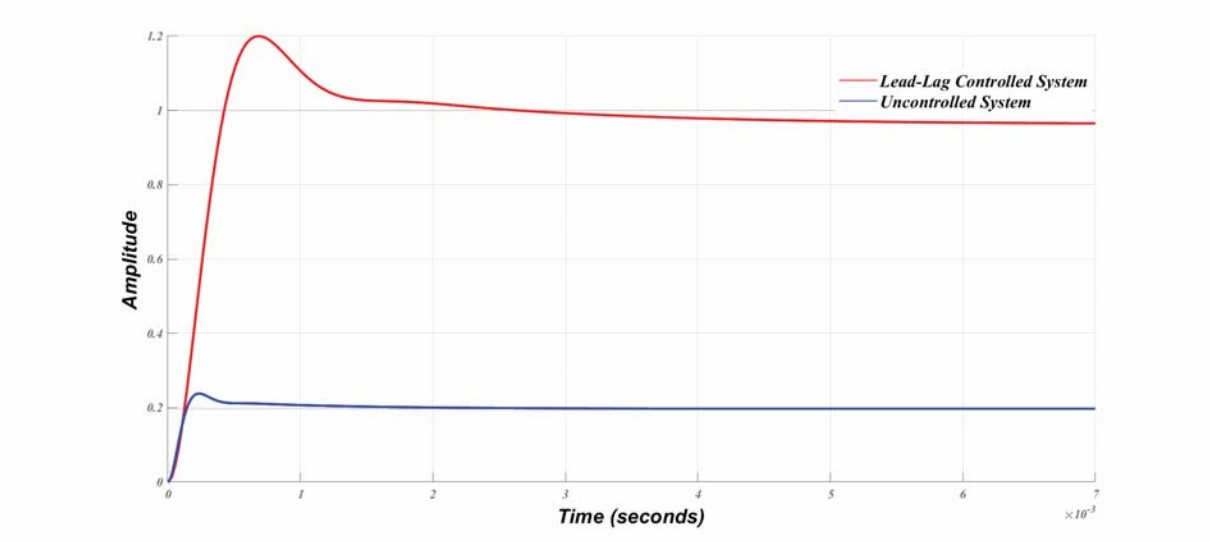

Figure 5.2: Step Response of the Uncontrolled System, and that being Controlled by a *Lead-Lag* Compensator.

5.3 Implementation of *Lead-Lag* Compensator with Sinusoidal Pulse Width Modulation Control of Electric Spring

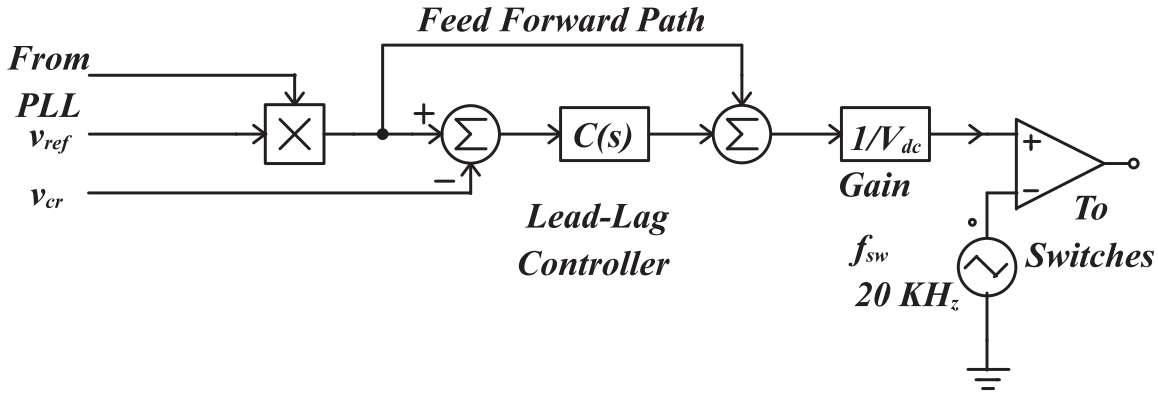

Figure 5.3: $SPWM$ Controled ES.

Simulation test bench, presented in Fig: 2.14 (incorporating parameters mentioned in TABLE. 2.1), has been used for testing the performance of the designed *Lead-Lag* Controller (5.10). The converter (VSC), acting as ES, has been designed with a rating

of 63.1 KVA for catering to the maximum load connected to the system. The heart of the setup-ES, is being controlled by its brain, the controller ($C(s)$), as has been designed in Sec: 5.2.1. Closed-loop control block (as shown in Fig: 5.3) using the designed *Lead-Lag* controller (5.10) generates the switching command signals (u_1 through u_4), governing the switches of the converter. Enhanced-Phase Lock Loop (E-PLL) has been used to synchronize the converter's output, for being there in the phase with that of v_g, as presented in the Sec: 3.6.3 of Chapter:3,. A feed-forward path has been incorporated in the control block to minimize the transients that could generate large overshoots in the presence of dynamics (at the wake of switching of load or excursions in the grid voltage).

5.3.1 Analysis of the Results

Table 5.1: Results of $SPWM$ Controlled ES

Time	*Load*	V_g	V_{nc}	V_{es}	I_g	I_{nc}	I_{cr}	I_{inv}	Power	V_{cr}	% Reg.	% Imp.	**% THD**	
(s)	(Ω)	(V)	(V)	(V)	(A)	(A)	(A)	(A)	(W)	(V)	V_{cr}	In Reg.	(v_{cr})	(i_{cr})
0.33995	6.6 + j5.78	183.85	250.69	475.38	90.64	113.95	26.23	113.90	20173.00	230.02	0.01	37.44	1.13	0.61
0.66995	6.6 + j5.78	229.81	57.43	276.76	0.82	26.11	26.22	25.97	82.34	230.02	0.01	21.80	1.92	0.35
0.99995	6.6 + j5.78	275.77	151.00	79.09	90.12	68.64	26.22	68.73	-20295.60	230.03	0.01	6.16	1.89	0.43
1.33995	50 + j5.78	183.85	209.39	437.68	90.62	95.18	4.57	95.20	20166.80	230.02	0.01	35.45	1.02	0.44
1.66995	50 + j5.78	229.81	10.96	240.94	0.86	4.98	4.57	5.62	89.57	230.02	0.01	19.31	2.12	0.41
1.99995	50 + j5.78	275.77	188.07	59.20	90.04	85.49	4.57	85.63	-20280.10	230.03	0.01	3.17	1.94	0.47
2.33995	6.6 - j5.78	183.85	239.58	469.58	90.63	108.90	26.22	108.99	20169.40	230.01	0.00	36.87	0.69	1.18
2.66995	6.6 - j5.78	229.81	59.38	277.18	1.49	26.99	26.22	27.42	87.01	230.02	0.01	21.09	1.38	2.05
2.99995	6.6 - j5.78	275.77	169.15	110.03	90.04	76.89	26.23	77.15	-20284.20	230.01	0.01	5.31	1.57	2.18
3.33995	50 - j5.78	183.85	208.99	437.49	90.62	95.00	4.57	95.03	20166.50	230.01	0.01	35.43	0.96	0.96
3.66995	50 - j5.78	229.81	11.33	240.96	1.07	5.15	4.57	5.85	89.60	230.02	0.01	19.29	1.89	1.88
3.99995	50 - j5.78	275.77	188.53	60.68	90.03	85.69	4.57	85.84	-20279.00	230.03	0.01	3.15	1.56	1.55
4.33995	6.6 + j0.00	183.85	275.20	504.14	90.65	125.09	34.85	125.08	20173.30	230.01	0.00	38.72	1.28	1.28
4.66995	6.6 + j0.00	229.81	77.61	307.59	1.36	35.28	34.85	35.38	84.84	230.01	0.01	23.40	1.42	1.42
4.99995	6.6 + j0.00	275.77	123.90	118.73	90.09	56.32	34.85	56.57	-20293.60	230.01	0.01	8.08	1.73	1.73
5.33995	50 + j0.00	183.85	209.32	437.72	90.62	95.14	4.60	95.18	20166.80	230.01	0.01	35.44	1.42	1.42
5.66995	50 + j0.00	229.81	11.21	241.09	0.94	5.09	4.60	5.76	89.67	230.02	0.01	19.31	2.03	2.03
5.99995	50 + j0.00	275.77	188.16	60.03	90.03	85.53	4.60	85.67	-20279.10	230.03	0.01	3.17	1.92	1.92

The simulation test-bench, presented in Fig: 2.14, has been used to justify the submitted claims pertaining to controller design and its efficacy (shown in Sect. 5.2.1). The critical load has been altered in terms of its rating and configuration by switching it in a manner specified in TABLE. 5.1 keeping R_{nc} fixed at 2.2 Ω. The operating scenario of the system without ES is not repeated here, as it has already been presented in Table:2.3. Dynamic variation in the grid voltage has been emulated by varying v_g (as mentioned in

TABLE. 5.1, in the range of $230 \pm 20\%$), solely to verify the robustness and accuracy of the presented *Lead-Lag* controller, under the influence of diverse and extensive excursions in the system parameters.

Grid voltage v_g, has been varied in the range of $184V$ to $276V$ (rms) along with the variation in Z_c, and keeping Z_g fixed at $0.5 + j0.1\Omega$ as specified by the different time instances and corresponding magnitudes, in the TABLE. 5.1). These perturbations can also be depicted from Fig: 5.4 through Fig: 5.11.

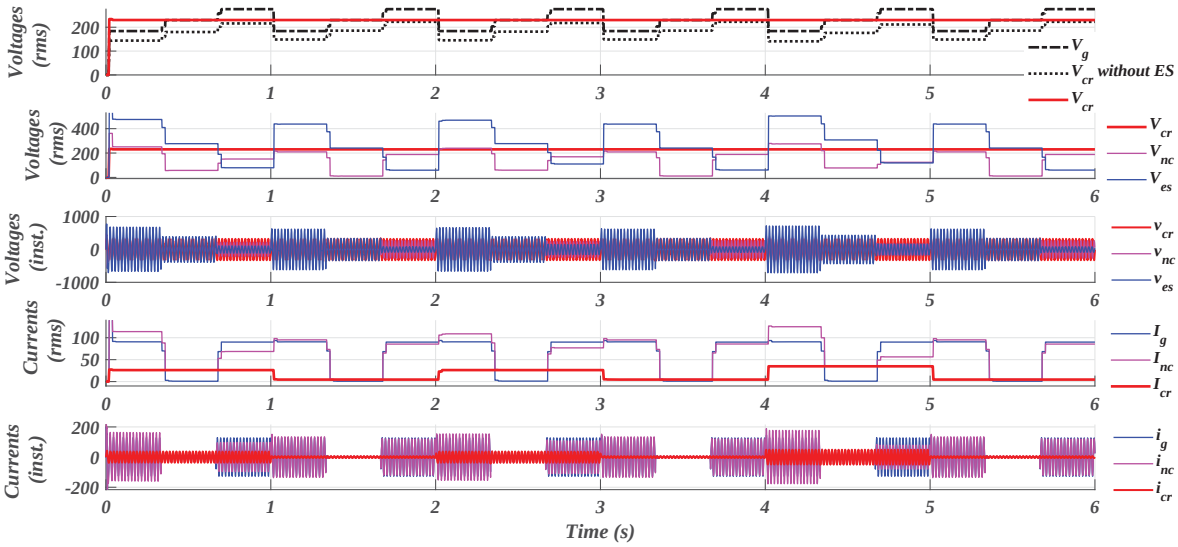

Figure 5.4: Results of *Lead-Lag* (SPWM) Control having Step Changes Applied to v_g and Load.

Fig: 5.4 represents the complete spectrum of simulation (0-6s), depicting the variation of different voltages and currents. Details with much a clear perspective, about the variation in the parameters for a specific load change, can be visualized from the Fig: 5.5 through Fig: 5.11. These parametric variations could have been resulted into the variations in v_{cr}, in the absence of ES (with a range-bound variation presented in Fig:2.15, of $140.95V$ to $222.76V$, with a corresponding regulation of 3.18% to 38.72%), but is remaining constant in the presence of ES, when being controlled by a *Lead-Lag* controller (with a variation of $230.01V$ to $230.03V$, with a corresponding regulation of 0.00% to 0.01%).

As it concerns to the critical load current (i_{cr}), without ES ($2.96A$ to $32A$), and with ES ($4.57A$ to $34.85A$, of a *Lead-Lag* controller), indicating a marginal increase in i_{cr} in the presence of ES. Current i_{cr} remains almost constant even in the presence of variations in v_g, as long as the load remains constant, when the ES is being controlled by a *Lead-Lag*

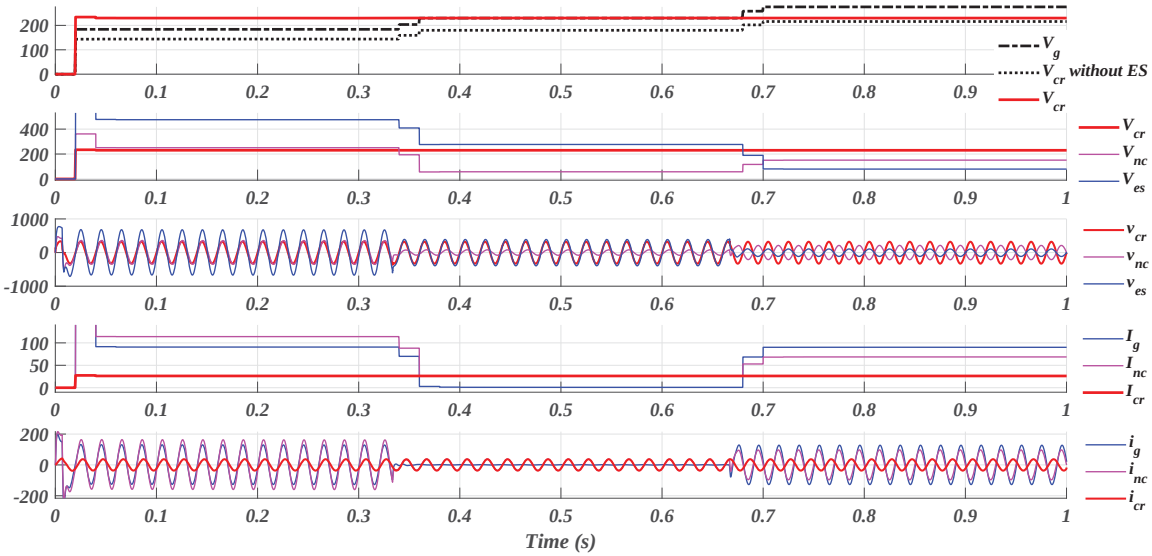

Figure 5.5: Results of *Lead-Lag* (SPWM) Control having Step Changes in v_{cr}, for R_1-L Load.

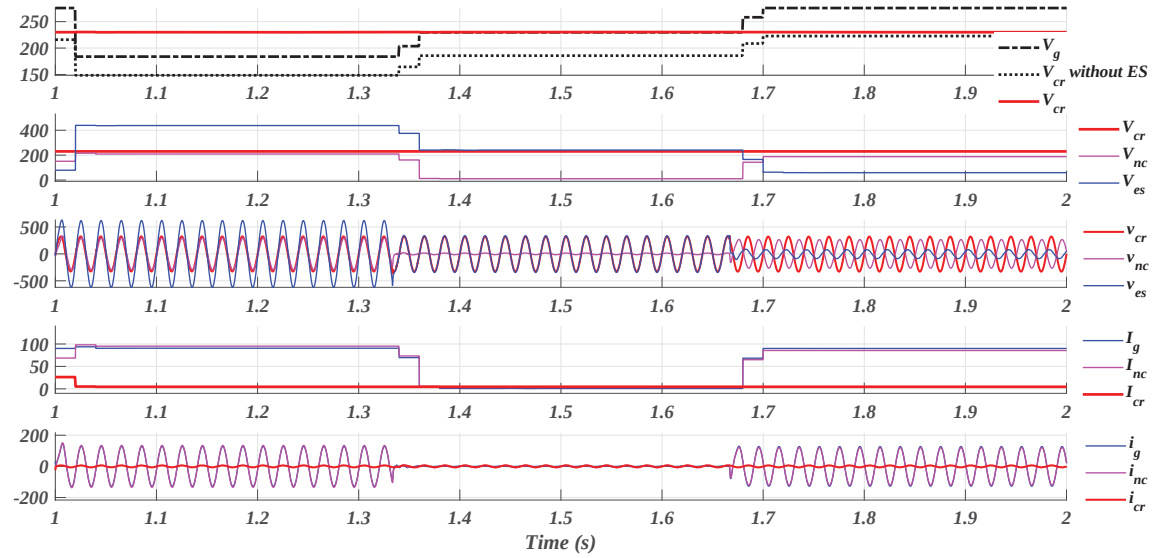

Figure 5.6: Results of *Lead-Lag* (SPWM) Control having Step Changes in v_{cr}, for R_2-L Load.

controller.

The variations of i_{nc} (4.98A to 125.09A with ES, which otherwise was 64.1A to 101.26Ain the absence of ES) can be seen from the same figures. Looking at the figures, it is evident that ES damps out alterations in the current i_{cr} which otherwise would have been facing variations due to change in v_g and load Z_c. This however results in

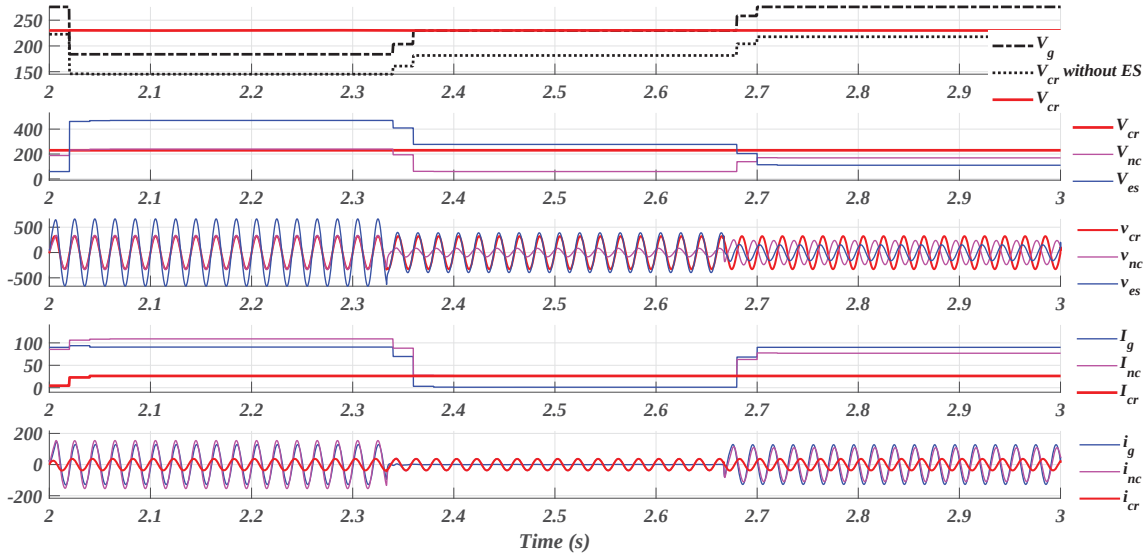

Figure 5.7: Results of *Lead-Lag* (SPWM) Control having Step Changes in v_{cr}, for R_1-C Load.

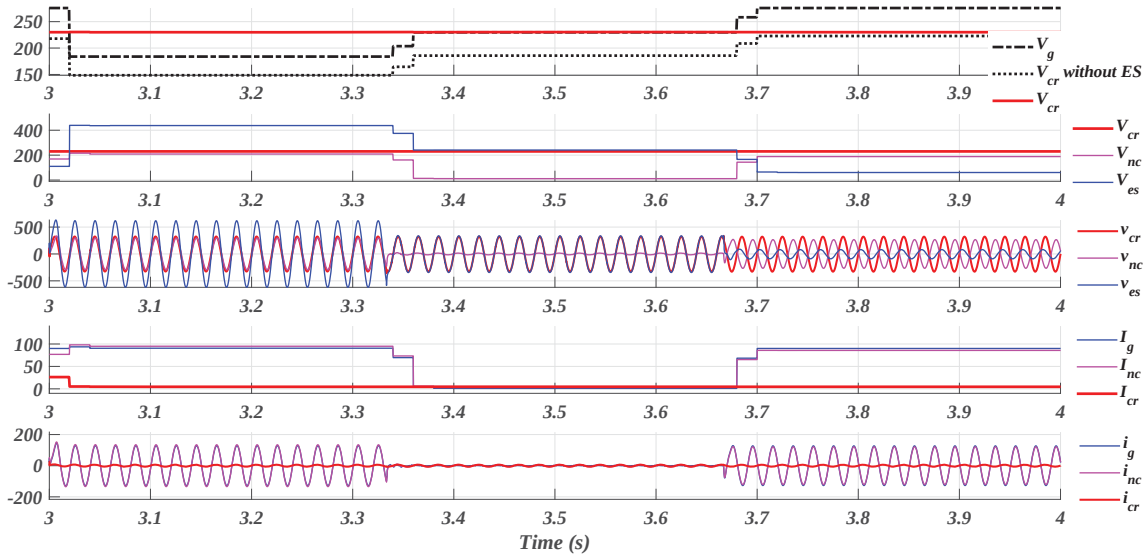

Figure 5.8: Results of *Lead-Lag* (SPWM) Control having Step Changes in v_{cr}, for R_2-C Load.

slightly larger variations in i_{nc}.

Fig: 5.11 exhibits the variations in *Power*, being drawn from the grid, in the absence of *ES* ($8.6KW$ to $28.03KW$), and with *ES* ($-20.3KW$ to $+20.2KW$ by a *Lead-Lag* controller). *Power* marked with "$+Ve$" sign signifies that the power demanded by the load is being catered by *ES* and grid simultaneously, and "$-Ve$" sign signifies the power

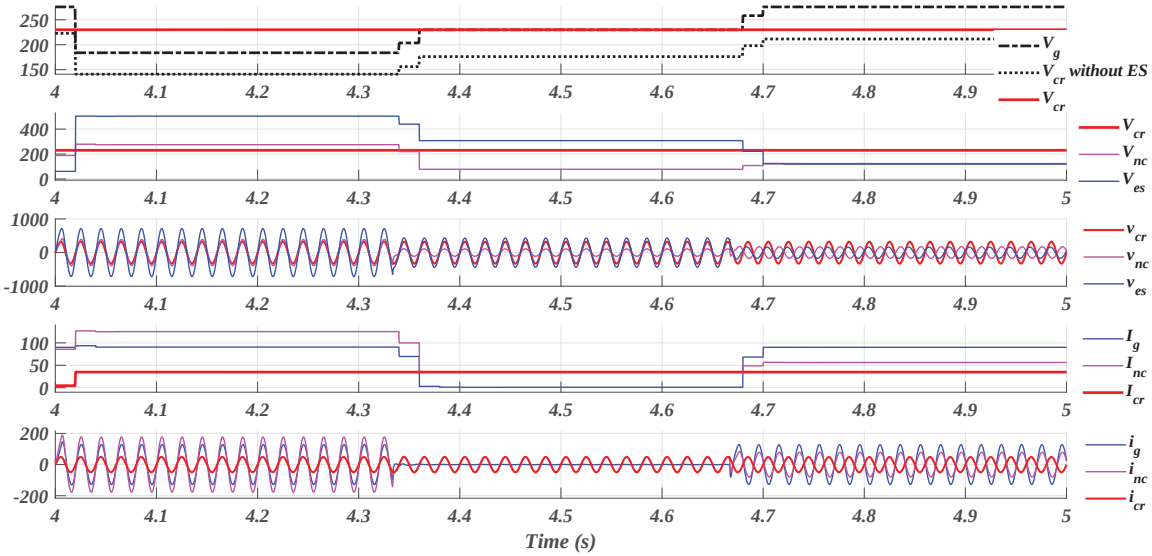

Figure 5.9: Results of *Lead-Lag* (SPWM) Control having Step Changes in v_{cr}, for R_1 Load.

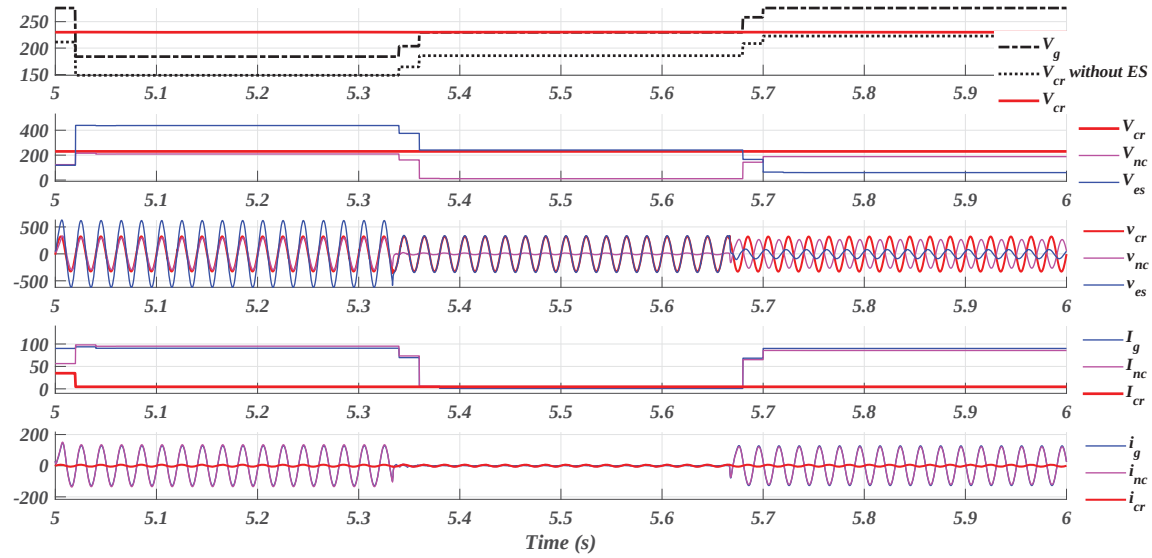

Figure 5.10: Results of *Lead-Lag* (SPWM) Control having Step Changes in v_{cr}, for R_2 Load.

flow from the grid. An ES supports active as well as reactive power, being delivered by it in the case of $v_g < v_{ref}$ and the same being absorbed partially by noncritical load and rest by ES when $v_g > v_{ref}$, so as to regulate v_s by tracking v_{ref} $(230V)$. Fig: 5.11 reveals a comprehensive peak power shaving (of about 8 KW) establishing an ES as a valid contender of Demand-Side Management (DSM). The vector summation (and not the

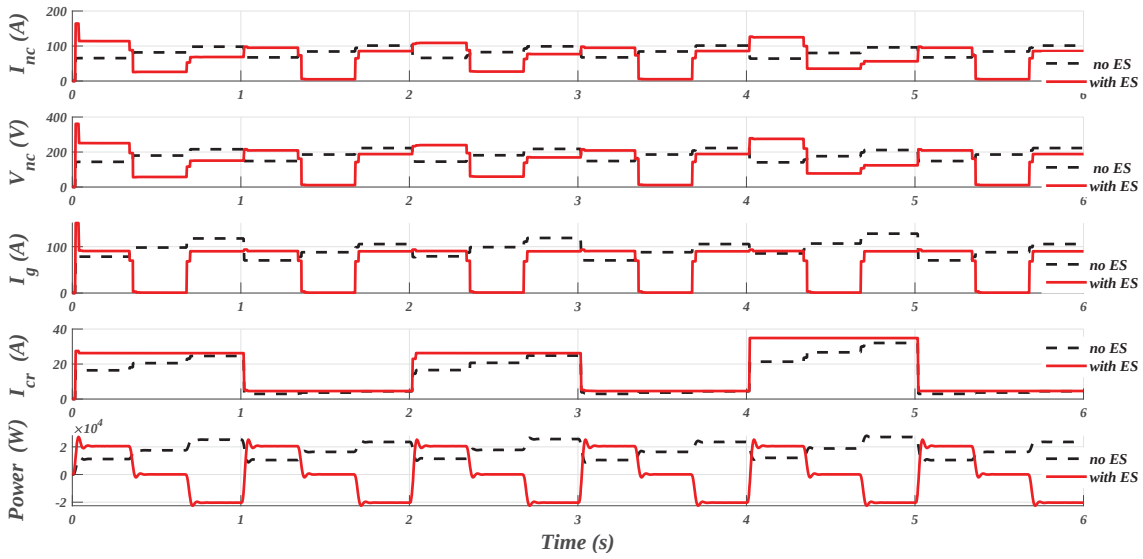

Figure 5.11: Comparison of Results of *Lead-Lag* Controlled ES and that with no ES, under the influence of Step Changes in v_g and Load.

algebraic sum) of v_{nc} and v_{es} resulting in the regulation of v_{cr} (revealed by TABLE. 5.1), by exchanging the active and/or reactive power, as demanded by the system. Another important fact that can be verified from the data of i_g is that it remains shallow ($0.82A$ to $1.49A$) at some six instances (when v_g is set to emanate the voltage somewhere in the vicinity of v_{ref}, i.e., $230V$). A minimal amount of power (82.34W to 87.01W) is required to be catered by ES, at those instances, to compensate for the voltage drop taking place across the connecting cable's impedance. The rest is taken care of by the grid voltage v_g, and the same can be depicted from the corresponding variation of I_{inv} (5.62A to 27.42A). The smooth and quick transition of v_{cr}, as has been envisaged in Sec: 5.2.1, can also be depicted from these figures, revealing and justifying the appropriateness of the controller's design aspect pertaining to $t_s < 10ms$, i.e., half of the cycle of the supply frequency. Considerable improvement in the voltage regulation (38.72%) could be verified from the Table:5.1, justifying the efficacy of the designed controller and hence ES.

5.4 Control of Single Phase Electric Spring through Space Vector Modulation

Numerous advantages of $SVPWM$ over $SPWM$ controlled VSC have been presented in the available technical literature [109][110][111], for the $3-\phi$ systems. These advantages have been summarized in the abstract form as:

- It inherently is having a (pseudo) third harmonic injection mechanism [110], whose peak happens to be always less than its fundamental (one being used with $SPWM$).
- $SVPWM$ give $2/\sqrt{3}$ times (approximately 15%) more output using the same DC-bus (V_{dc}) [109], compared to $SPWM$. The same could be explained as:

$$V_{LL(max)}(SPWM) = \frac{\sqrt{3}}{2\sqrt{2}}V_{dc} = 0.612V_{dc}$$
$$V_{LL(max)}(SVPWM) = \frac{V_{dc}}{\sqrt{2}} = 0.707V_{dc}$$

- $SVPWM$ has lesser harmonic content [112] of 3.66%, as that compared to 6.05% with $SPWM$.
- $SVPWM$ offer better efficiency due to reduced number of switching and hence switching losses, compared to $SPWM$.

It has been decided to implement $SVPWM$ control for 1-ϕ VSC, i.e., for the control of ES, considering the advantages as mentioned above of $SVPWM$ control. However, a little has been said in the available literature for the application of speed control of $2-\phi$ motor drives [113]. The work on the motion control of 2-ϕ induction motor [114] has provided the motivation and impetus to apply this concept of $SVPWM$ in the application of ES. The designed *Lead-Lag* controller (5.10) has been used to let the system follow the reference signal (v_{ref}) with minimum possible error.

Inherently, $SVPWM$ strategy is meant to be used for the control of 3-ϕ VSC. A lot of research and corresponding publications can be witnessed on 3-ϕ inverters, implemented with $SVPWM$ control. Lack of availability of 3-ϕ supply network in residential and/or commercial buildings, as they are conventionally equipped with 1-ϕ supply, has been the key driving factor in the implementation of 1-ϕ $SVPWM$ technique of converter control.

Further, the purview of this work has been restricted to 1-ϕ ES only, for the reason that ES is a custom power device having a small to moderately rated VSC.

The implementation of 1-ϕ $SVPWM$ has been made possible through the stationary reference frame using Clarke's transformation [115] i.e., α-β to a-b-c transformation. The orthogonal signal β has been generated by delaying the signal α by a quarter of the cycle ($\omega t - \pi/2$), considering 1-ϕ controlled signal available at the output of the *Lead-Lag* controller as α. The required information of the ω has been gathered from the E-PLL structure. The block diagram explaining the control structure has been presented in Fig:5.12

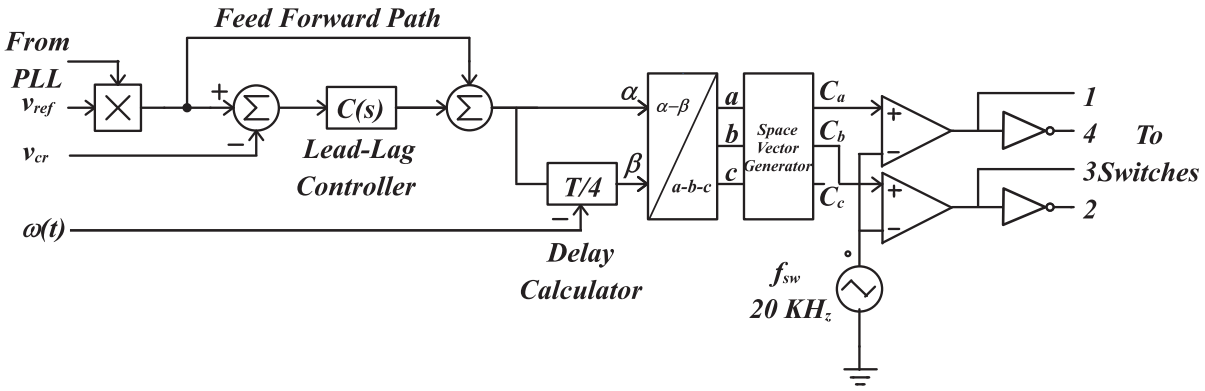

Figure 5.12: $SVPWM$ Controled ES using *Lead-Lag* Compensator.

$SVPWM$ control has been implemented by comparing the control signal with the fixed frequency triangular wave, in a manner similar to that of $SPWM$ control, by using the concept presented in [109]. Two of the control signals (C_a and C_b), generated from the space vector generator block (implemented using the technique mentioned in [111], for the 3-ϕ converters, by applying necessary changes required to be taken for the implementation of the same with the 1-ϕ system), has been used to switch the inverter by dropping the third one (C_c) for the reason that we need to trigger the 1-ϕ inverter possessing two lags, comprising of four switches only.

5.4.1 Analysis of the Results

The $SVPWM$ controlled ES using *Lead-Lag* conmpensator has been implemented on to the test bench presented in Fig: 2.14, with the load parameters of the system being 15% higher than those considered in the SPWM case ($Z_{nc} = 1.9\Omega$, $Z_{cr1} = 5.7 \pm j5.78\Omega$, $Z_{cr2} =$

Table 5.2: Results of $SVPWM$ Control

Time	*Load*	V_g	V_{nc}	V_{es}	I_g	I_{nc}	I_{cr}	I_{inv}	Power	V_{cr}	% Reg.	% Imp.	**% THD**	
(s)	(Ω)	(V)	(V)	(V)	(A)	(A)	(A)	(A)	(W)	(V)	V_{cr}	In Reg.	(v_{cr})	(i_{cr})
0.33995	5.7 + j5.78	183.85	153.52	372.58	54.39	80.80	28.35	80.63	11647.20	230.02	0.01	47.38	2.20	0.39
0.66995	5.7 + j5.78	229.81	53.97	271.42	1.55	28.40	28.35	28.07	76.94	230.29	0.13	34.33	5.01	0.44
0.99995	5.7 + j5.78	275.77	58.50	171.71	53.91	30.79	28.35	30.79	-11630.90	230.04	0.02	21.07	2.14	0.44
1.33995	42.5 + j5.78	183.85	113.36	339.60	54.40	59.66	5.36	59.56	11647.20	230.02	0.01	44.83	2.17	0.61
1.66995	42.5 + j5.78	229.81	11.50	241.12	2.05	6.05	5.36	5.96	81.87	230.29	0.12	31.14	4.71	1.15
1.99995	42.5 + j5.78	275.77	92.50	147.74	53.91	48.69	5.36	48.85	-11631.90	230.01	0.00	17.23	1.18	0.49
2.33995	5.7 - j5.78	183.85	135.55	365.50	54.39	71.34	28.34	71.40	11647.00	230.00	0.00	46.19	0.46	0.42
2.66995	5.7 - j5.78	229.81	55.05	271.53	2.61	28.98	28.36	29.25	83.15	230.09	0.04	32.78	2.67	3.68
2.99995	5.7 - j5.78	275.77	93.82	186.60	53.92	49.38	28.34	49.72	-11632.30	230.00	0.00	19.29	0.58	0.70
3.33995	42.5 - j5.78	183.85	112.54	339.32	54.40	59.23	5.36	59.14	11647.30	230.02	0.01	44.78	1.34	1.35
3.66995	42.5 - j5.78	229.81	11.45	240.91	1.78	6.03	5.36	6.08	81.58	230.08	0.03	31.00	2.53	2.55
3.99995	42.5 - j5.78	275.77	93.54	148.38	53.91	49.23	5.36	49.40	-11632.20	230.00	0.00	17.16	0.62	0.62
4.33995	5.7 + j0.00	183.85	177.56	405.73	54.39	93.45	40.35	93.40	11645.10	230.01	0.00	49.22	0.88	0.88
4.66995	5.7 + j0.00	229.81	77.44	307.44	1.80	40.76	40.36	40.73	78.43	230.06	0.02	36.54	2.38	2.38
4.99995	5.7 + j0.00	275.77	40.52	213.55	53.97	21.33	40.36	21.71	-11629.70	230.07	0.03	23.85	2.07	2.07
5.33995	42.5+ j0.00	183.85	113.12	339.64	54.39	59.54	5.41	59.44	11647.10	230.02	0.01	44.81	1.23	1.23
5.66995	42.5+ j0.00	229.81	11.52	241.12	1.84	6.06	5.41	6.06	81.38	230.10	0.04	31.05	2.71	2.71
5.99995	42.5+ j0.00	275.77	92.84	148.23	53.91	48.86	5.41	49.03	-11632.20	230.00	0.00	17.21	0.51	0.51

$42.5 \pm j5.78\Omega$ and $Z_g = 0.8 + j0.3\Omega$), just to prove the worth of a SVPWM control. Grid voltage v_g, has been varied in the range of $184V$ to $276V$ (rms) along with the variation in Z_c, as specified by the different time instances and corresponding magnitudes, in the TABLE. 5.2). These perturbations can also be depicted from Fig: 5.13 through Fig: 5.23.

Fig: 5.13 represents the complete spectrum of simulation (0-6s), depicting the variation of different voltages and currents. The variation in the parameters for a specific load change can be visualized from the Fig: 5.14 through Fig: 5.19, with a much clear perspective. These parametric variations could have been resulted in the variations in v_{cr}, in the absence of ES (with a range-bound variation of $116.8V$ to $190.5V$), but is remaining constant in the presence of ES, when being controlled by a *Lead-Lag* controller (with a variation of $230.00V$ to $230.3V$).

Results pertaining to $SVPWM$ controlled ES, using a *Lead-Lag* compensator, has been presented in Fig.5.13 through Fig.5.23. Fig.5.20 shows the RMS values of the parameters associated with the performance of $SVPWM$ controlled ES. The critical and non-critical load of the system has been increased by 15% to prove that $SVPWM$ can give 15% more output, and the same can be seen from the data presented in Table: 5.2.

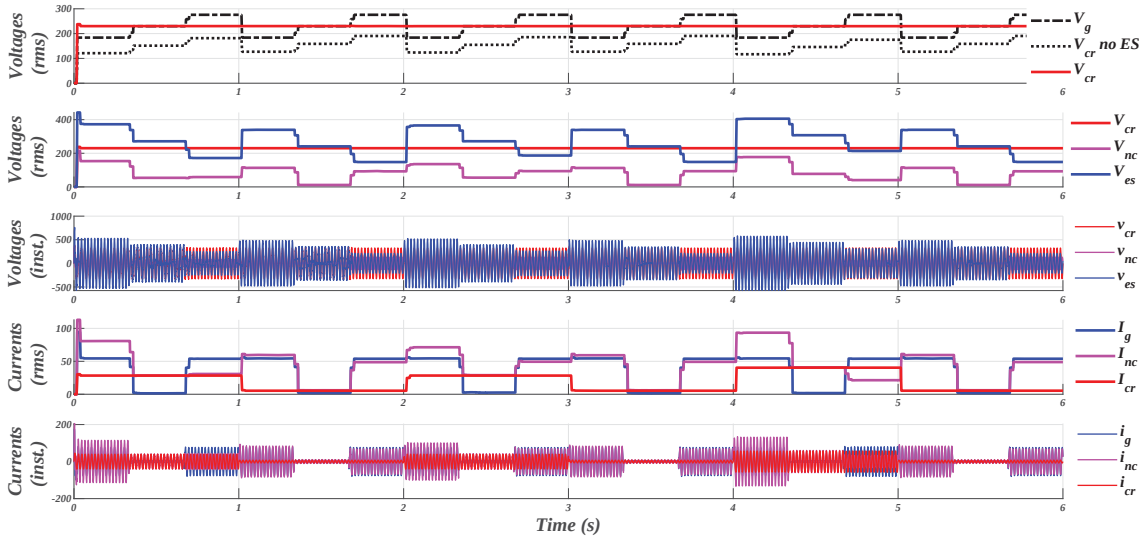

Figure 5.13: Results of *Lead-Lag* (SVPWM) Control having Step Changes Applied to v_g and Load.

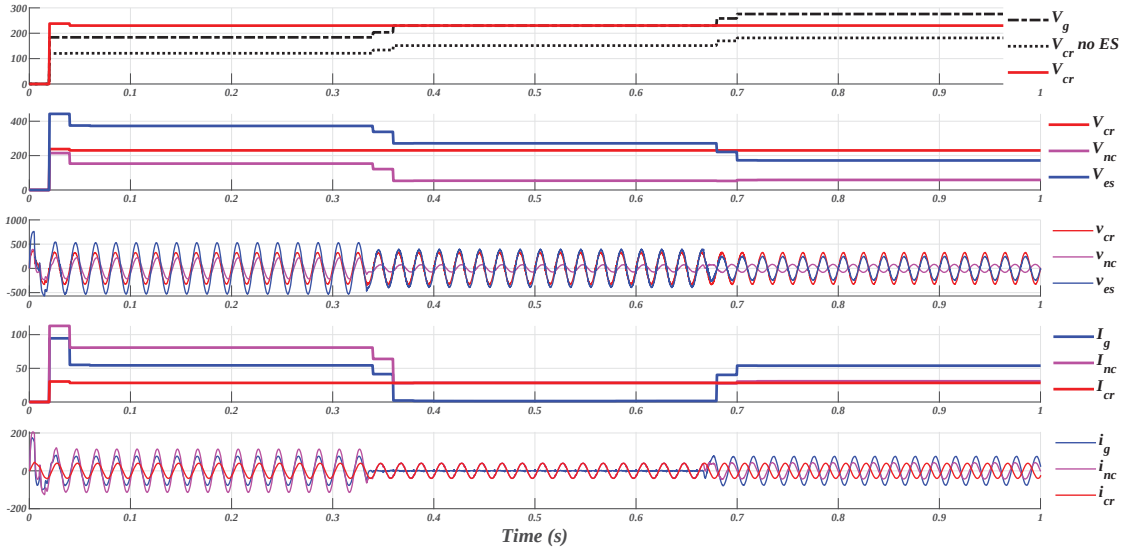

Figure 5.14: Results of *Lead-Lag* (SVPWM) Control having Step Changes in v_{cr}, for R_1-L Load.

No visible difference could be noticed when this performance is compared with an $SPWM$ controlled ES. Nicely regulated v_{cr} can be detected from Fig.5.20, showing no transients at the instances of transiting load and grid voltage. The instances of these transitions and corresponding parameters could also be seen from the Table:5.2.

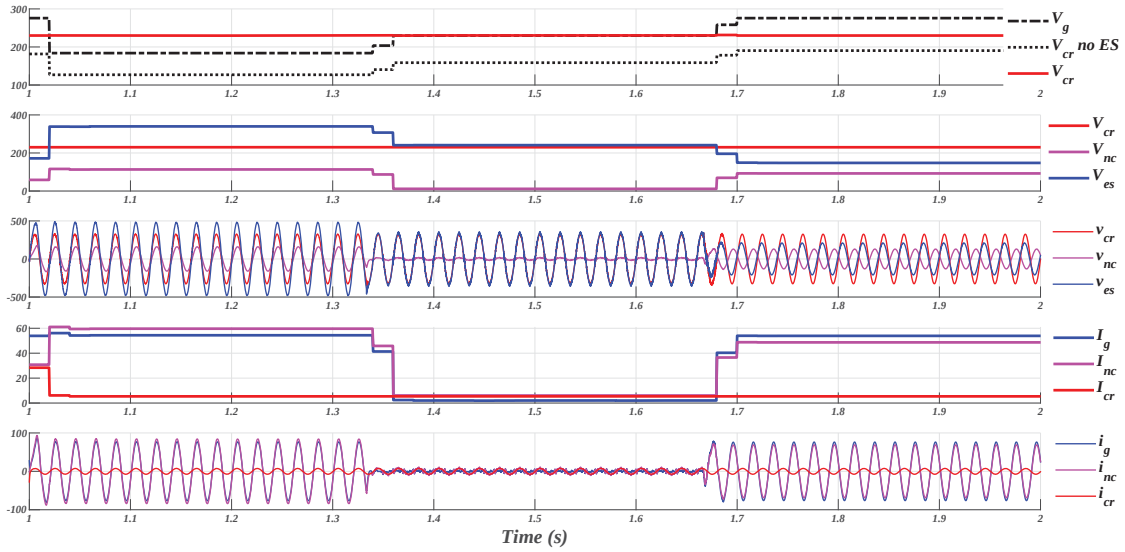

Figure 5.15: Results of *Lead-Lag* (SVPWM) Control having Step Changes in v_{cr}, for R_2-L Load.

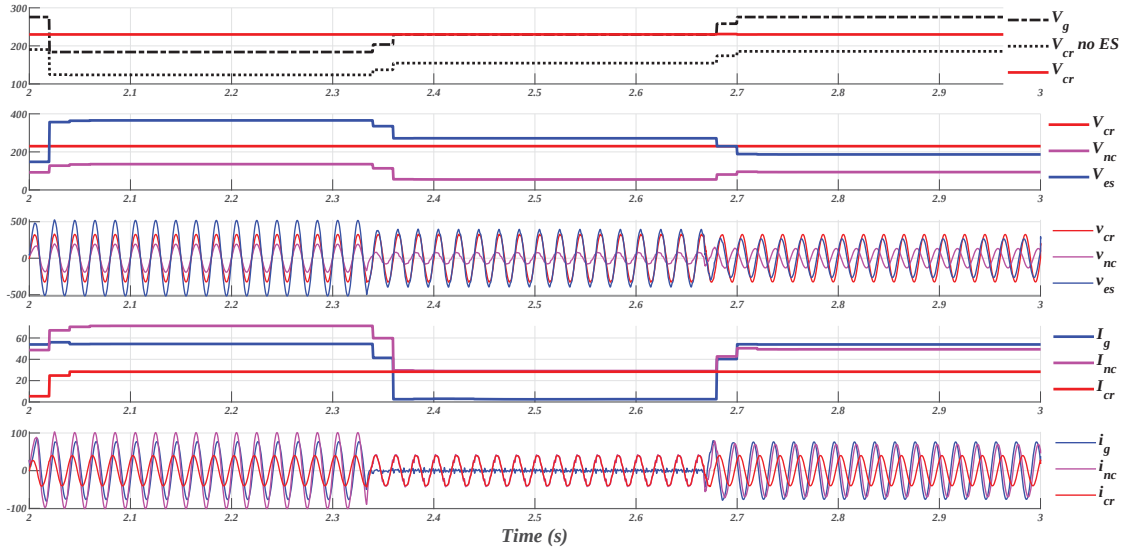

Figure 5.16: Results of *Lead-Lag* (SVPWM) Control having Step Changes in v_{cr}, for R_1-C Load.

Fig.5.21 shows the complete spectrum of variation in the instantaneous values of parameters associated with the $SVPWM$ controlled ES. Well-regulated v_{cr} could also be noticed from here. Current i_{cr} found to remain constant for a typical load even in the presence of grid voltage variation.

Parameters associated with the control aspect of ES has been presented in Fig:5.21

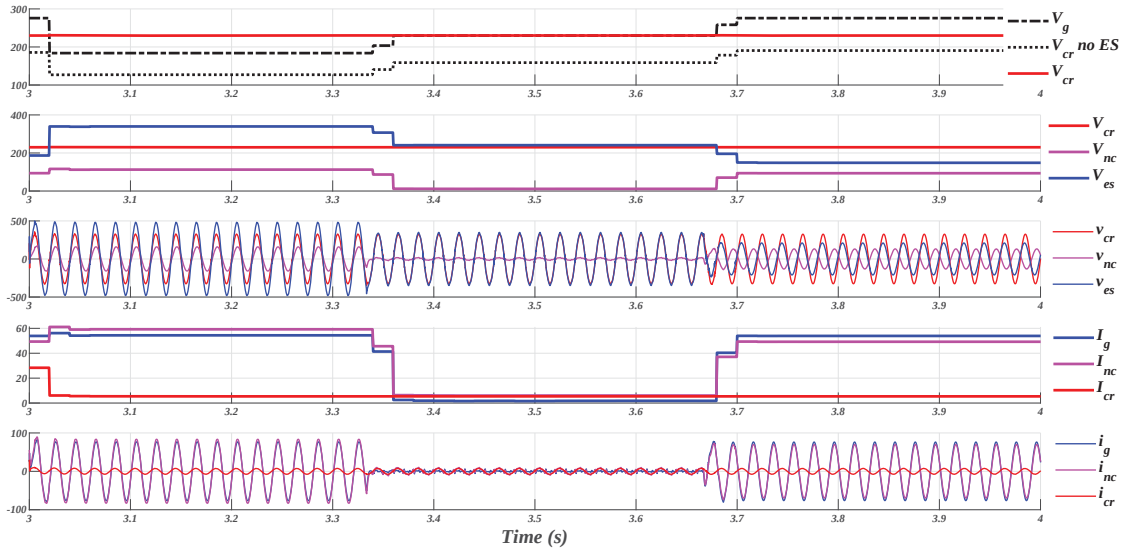

Figure 5.17: Results of *Lead-Lag* (SVPWM) Control having Step Changes in v_{cr}, for R_2-C Load.

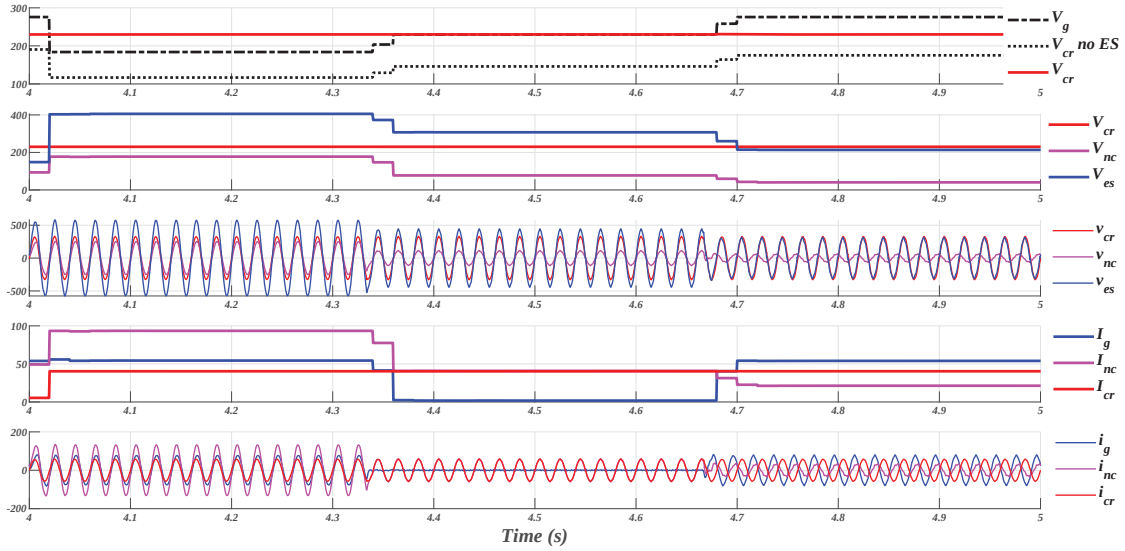

Figure 5.18: Results of *Lead-Lag* (SVPWM) Control having Step Changes in v_{cr}, for R_1 Load.

and its magnified view for the period (4s to 5s) showing the largest possible load on the system has been presented in Fig:5.22 and corresponding FFT spectrum from Fig.5.23. The FFT analysis of the results showing only the fundamental components (except in v_{ca} and v_{cb}). v_{cr} shows a peak of 325V (corresponding to 230V (rms). 3^{rd} harmonic has been found to be present in v_{ca} and v_{cb}, as has been discussed in the advantages of $SVPWM$

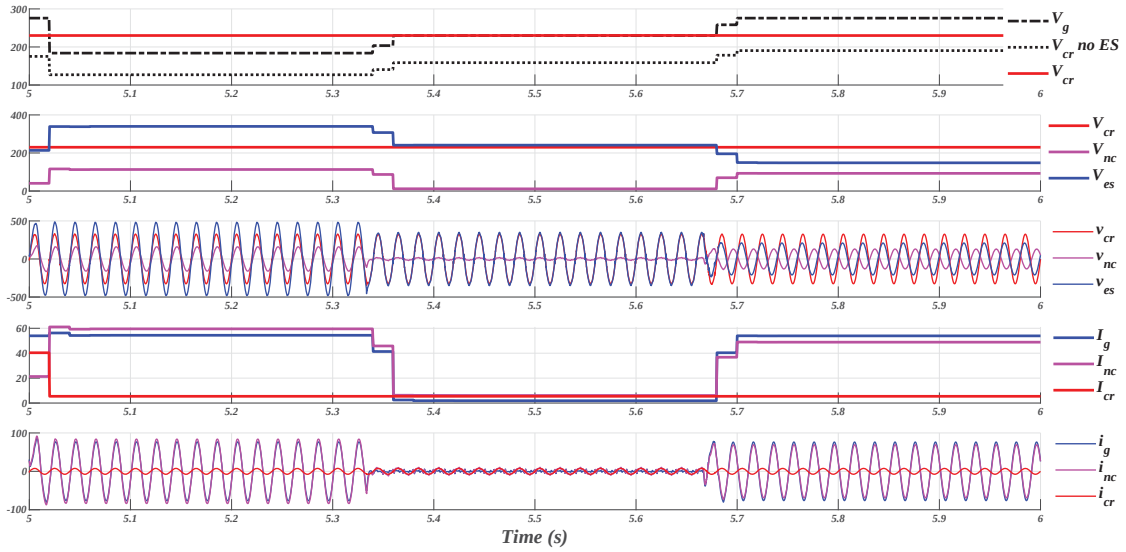

Figure 5.19: Results of *Lead-Lag* (SVPWM) Control having Step Changes in v_{cr}, for R_2 Load.

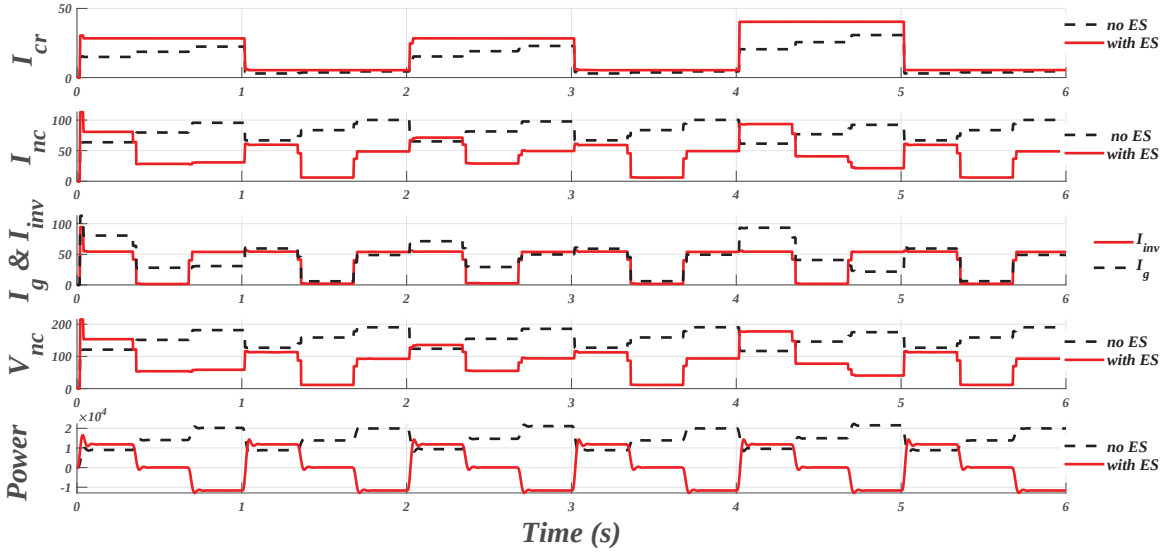

Figure 5.20: Results (RMS values) of $SVPWM$ Controlled ES, using *Lead-Lag* Compensator, being Compared with the Scenario of Absence of ES, in the presence of Step Changes Applied to v_g and Load.

in Sec:5.4. Further, THD of v_{cr} and i_{cr}, for this entire spectrum has been found to be 0.53%.

Fig.5.22 reveals the magnified spectrum of the instantaneous values presented in Fig.5.21 (for a period of 4s to 5s). It reveals a minimum overshoot in v_α, v_β. , v_a,

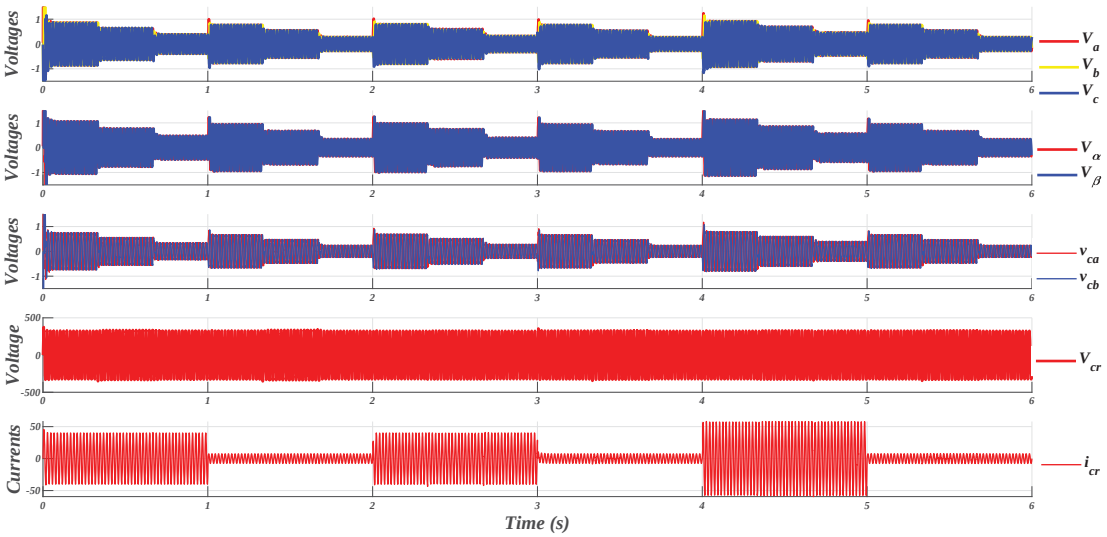

Figure 5.21: Control Parameters (Instantaneous Values) of $SVPWM$ Controlled ES

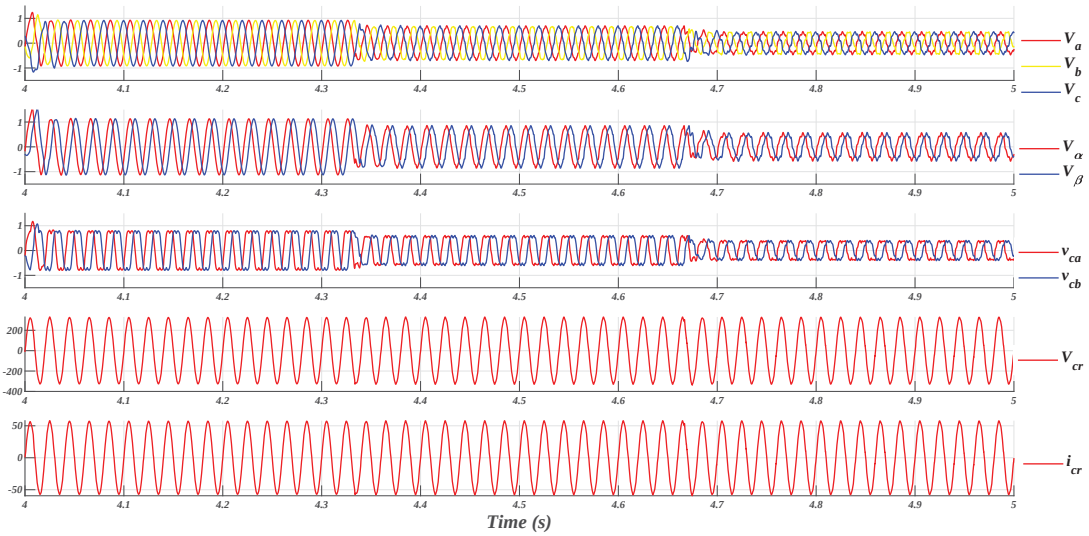

Figure 5.22: Magnified Spectrum of the Control Parameters (Instantaneous Values) of $SVPWM$ Controlled ES, Showing R_1 Load and Step Changes Applied to v_g.

v_b, and v_c. It also reveals the absence of any overshoot in v_{cr} and i_{cr}, in the presence of changing load and perturbing grid voltage. The THD for this duration is found to be 2.17%.

Fig.5.23 shows the corresponding FFT spectrum of Fig.5.22. It shows the presence of fundamental at 50 Hertz, with corresponding peaks and 3^{rd} harmonics in v_{ca} and v_{cb}. Table:5.2 reveals the %THD for a typical load pertaining to a specific v_g, along with the

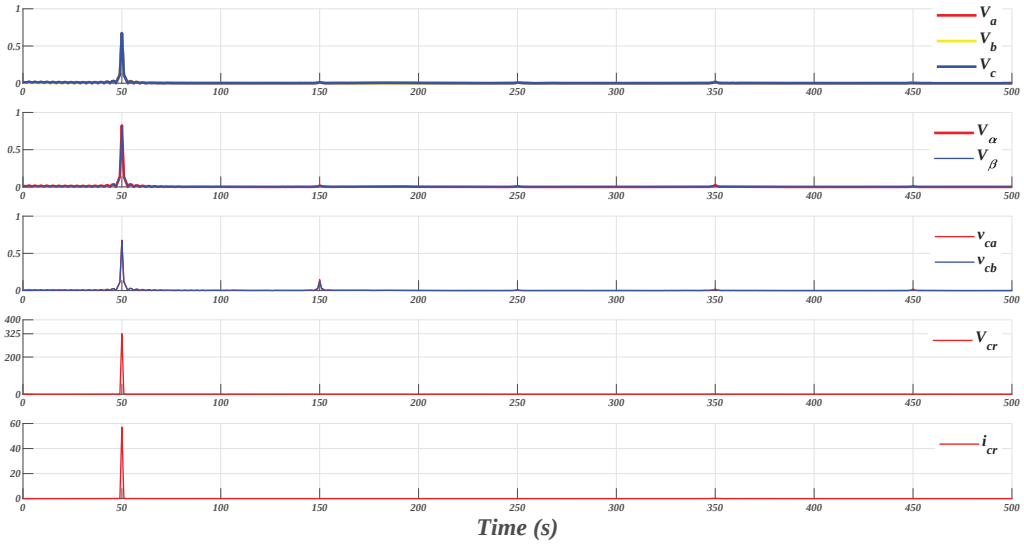

Figure 5.23: FFT Spectrum of Results presented in Fig:5.22.

% regulation that has been offered by ES to the v_{cr}. A vast range of % improvisation (17.16 % to 49.22 %) in the regulation in v_{cr} through ES, when being compared with unregulated v_{cr} in the absence of ES, can be seen from the same data.

5.5 Comparison of the Results achieved through Sinusoidal Pulse Width Modulation and Space Vector Pulse Width Modulation

Results of $SVPWM$ and $SPWM$ controlled ES, has been reflected through the Fig:5.24 and Fig:5.25 and the same have been tabulated in Table:5.3. Fig:5.24 gives the comparative analysis of the voltages(V_g, V_{cr}, V_{nc} and V_{es}). It can be said that the two results associated with V_{cr}, go hand in hand. V_{cr} remains at a slightly higher side with the case of $SVPWM$ control, when v_g is staying in the vicinity of $230V$, for all the types of load. $SVPWM$ controlled system is incorporated with a 15% higher load than $SPWM$ control, even though it needs lesser voltage to be injected by ES, and the same could be evident from the smaller power rating of ES. Fig:5.25 shows the comparative results of the two strategies pertaining to the current signal (I_g, I_{cr}, I_{nc} and I_{es}). Higher current, I_{cr} in the case of $SVPWM$ control signifies the 15% higher loads than the $SPWM$ controlled

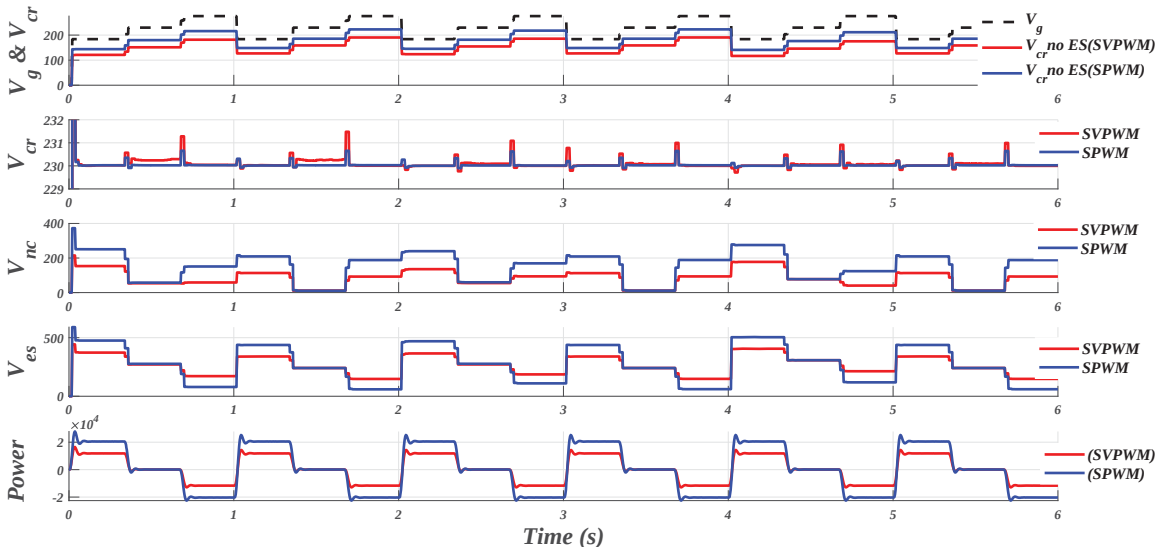

Figure 5.24: Comparative Results (RMS values of Voltages) of $SVPWM$ and $SPWM$ Controlled ES, using *Lead-Lag* Compensator, having Step Changes Applied to v_g and Load.

system. Looking at the comparative results of currents, it is evident that $SVPWM$ controlled ES operates with higher loads, though it has been drawing smaller current from the grid and from the VSC, compared to $SPWM$ controlled ES.

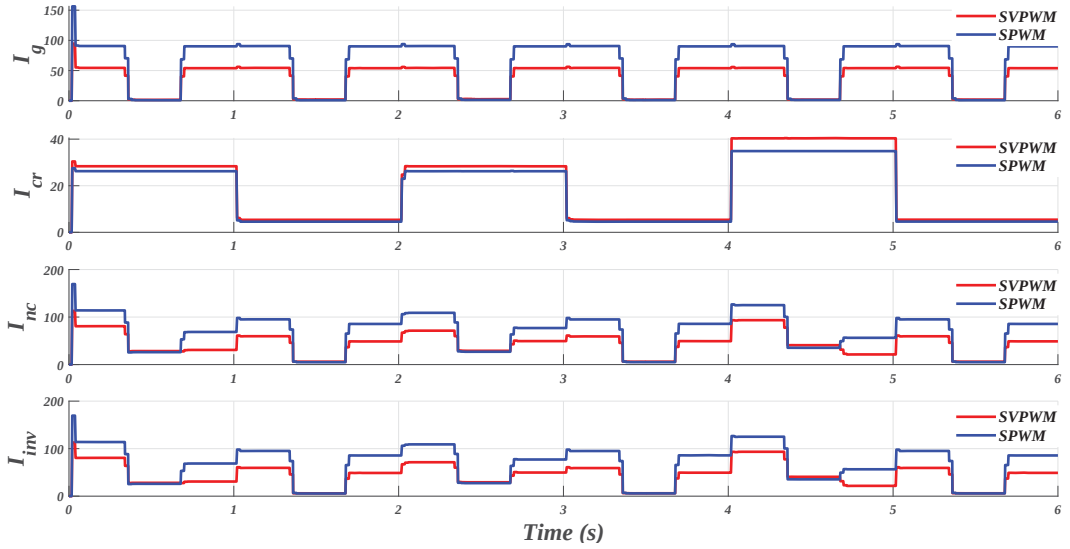

Figure 5.25: Comparative Results (RMS values of Currents and Power) of $SVPWM$ and $SPWM$ Controlled ES, using *Lead-Lag* Compensator, having Step Changes Applied to v_g and Load.

Table 5.3: Comparison of the Results Between $SVPWM$ and $SPWM$ Control

Time	*Load(Ω)*		V_g	V_{nc}*(V)*		I_{nc}*(A)*		V_{cr}*(V)*		*%Reg.*	
(s)	***SVPWM***	***SPWM***	*(V)*	***SVPWM***	***SPWM***	***SVPWM***	***SPWM***	***SVPWM***	***SPWM***	***SVPWM***	***SPWM***
0.33995	5.7 + j5.78	6.6 + j5.78	183.85	153.52	250.69	80.80	113.95	230.02	230.02	0.01	0.01
0.66995	5.7 + j5.78	6.6 + j5.78	229.81	53.97	57.43	28.40	26.11	230.29	230.02	0.13	0.01
0.99995	5.7 + j5.78	6.6 + j5.78	275.77	58.50	151.00	30.79	68.64	230.04	230.03	0.02	0.01
1.33995	42.5 + j5.78	50 + j5.78	183.85	113.36	209.39	59.66	95.18	230.02	230.02	0.01	0.01
1.66995	42.5 + j5.78	50 + j5.78	229.81	11.50	10.96	6.05	4.98	230.29	230.02	0.12	0.01
1.99995	42.5 + j5.78	50 + j5.78	275.77	92.50	188.07	48.69	85.49	230.01	230.03	0.00	0.01
2.33995	5.7 - j5.78	6.6 - j5.78	183.85	135.55	239.58	71.34	108.90	230.00	230.01	0.00	0.00
2.66995	5.7 - j5.78	6.6 - j5.78	229.81	55.05	59.38	28.98	26.99	230.09	230.02	0.04	0.01
2.99995	5.7 - j5.78	6.6 - j5.78	275.77	93.82	169.15	49.38	76.89	230.00	230.01	0.00	0.01
3.33995	42.5 - j5.78	50 - j5.78	183.85	112.54	208.99	59.23	95.00	230.02	230.01	0.01	0.01
3.66995	42.5 - j5.78	50 - j5.78	229.81	11.45	11.33	6.03	5.15	230.08	230.02	0.03	0.01
3.99995	42.5 - j5.78	50 - j5.78	275.77	93.54	188.53	49.23	85.69	230.00	230.03	0.00	0.01
4.33995	5.7 + j0.00	6.6 + j0.00	183.85	177.56	275.20	93.45	125.09	230.01	230.01	0.00	0.00
4.66995	5.7 + j0.00	6.6 + j0.00	229.81	77.44	77.61	40.76	35.28	230.06	230.01	0.02	0.01
4.99995	5.7 + j0.00	6.6 + j0.00	275.77	40.52	123.90	21.33	56.32	230.07	230.01	0.03	0.01
5.33995	42.5+ j0.00	50 + j0.00	183.85	113.12	209.32	59.54	95.14	230.02	230.01	0.01	0.01
5.66995	42.5+ j0.00	50 + j0.00	229.81	11.52	11.21	6.06	5.09	230.10	230.02	0.04	0.01
5.99995	42.5+ j0.00	50 + j0.00	275.77	92.84	188.16	48.86	85.53	230.00	230.03	0.00	0.01

Table:5.3 reflect the data so as to compare the two strategies of control. The last two columns of the results reveal the % Regulating capabilities exhibited by $SVPWM$ and $SPWM$ control.

5.6 Conclusion

The combination of electric spring and non-critical load has been acting as a smart load to maintain a constant voltage (v_{cr}) across the critical load and reduce the storage requirement by the extent to which the non-critical load supports the voltage regulation possible. Results reveal greater accuracy of *Lead-Lag* (the two instances of best regulation is 0.0% with $SPWM$ control, compared to six instances of 0.0% with $SVPWM$ control) controlled ES. On the contrary, $SVPWM$ controlled ES gives better compliance to harmonic reduction and makes the output distortion-free and, at the same time, reduced switching losses and efficiency compared to $SPWM$ control. $SVPWM$ controlled ES gives more output (approximately 15% more). The same has been verified by increasing the critical and non-critical loads by 15% and even then getting the same performance achieved through $SPWM$ controlled ES, being compensated by a *Lead-Lag* compensator. The *Lead-Lag* controller proved to work better with SVPWM, compared

to $SPWM$ controlled ES. The presence of a feed-forward path has helped the controller reduce the peak overshoot (maximum of $1V$) due to the dynamics introduced by the parametric variation in the load and changes taking place in the grid conditions. A significant amount of power shaving of $7.73KW$ in $SPWM$ control and even better $9.9KW$ of power shaving in $SVPWM$ control can improve the demand-supply mismatch and thereby act as a perfect mechanism of DSM in a real-time basis, without demanding any communication ICT support. A *Lead-Lag* controlled ES is smartly manipulating the presence of non-critical load to maintain the voltage of critical load with absolute precision and thereby alleviating the issue of voltage regulation. $SVPWM$ controlled *lead-Lag* compensated ES outperforms its $SPWM$ counterpart in terms of % Regulation in V_{cr}, smaller rating of the VSC acting as ES, lesser distortion and hence best overall performance.