Chapter 7

Comparative Performance Analysis of Controllers

7.1 Introduction

A detailed comparative analysis of the control structures derived in the previous Chapters has been presented here in the form of comparative analysis. Results pertaining to ES being controlled through PI, *Cascaded-PI* (executed feedback through i_{lf} or i_{cf}), *Lead-Lag* ($SPWM$ and $SVPWM$), and Optimal LQI compensator, have been critically compared to judge the best performing controller. The pros and cons of all the mentioned controllers have already been presented in the corresponding chapters, and the same have been summarized here as:

- As per Chapter:4, the PI controller is an ideal choice for tracking DC reference, due to its simplicity in the design. While tracking a sinusoidal command, the phase error is introduced.
- Chapter:4 presented the loop-in-loop (cascaded structure) PI controller, due to its dual state controlling capabilities, in the form of inner loop current (executed through sensing of either i_{lf} or i_{cf}) control and outer loop voltage control (v_{cr}). This has help to limit the inverter current in the case of faults and transients.
- Chapter:5, has been presented with the *Lead-Lag* compensator, being controlled through $SPWM$ and $SVPWM$ control of ES (both being incorporated with fixed

switching frequency). *Lead-Lag* compensator is used for better accuracy and precision, through improvised G.M. and P.M., which ultimately converge to higher bandwidth and greater robustness. $SPWM$ control is known for its simplicity, and $SVPWM$ control (primarily being employed for 3-ϕ systems) for 15% higher output using the same DC-bus , that is being used with $SPWM$ control.

- State feedback control of ES using LQR, being optimized through $LMIs$, possessing an integrator, has been presented in Chapter:5 for its robustness against the parametric excursions.

The detailed analysis and outcomes of the comparison have been presented in the following section.

7.2 Performance Comparison of the PI, $Cascaded$-PI, $Lead$-Lag and Optimal-LQI Controllers

Table 7.1: Comparative Analysis of the Results Obtained from PI, $Cascaded$-PI, $Lead$-Lag and LQI Controlled ES (with Limited Uncertainties)

Time (s)	Load (Ohms)		V_g (V)	V_{cr} (V)						% Regulation in V_{cr}					
	Rest	SVPWM$_{LL}$		PI	Cas. PI$_{i_1 f}$	Cas. PI$_{i_{cf}}$	SPWM$_{LL}$	SVPWM$_{LL}$	LQI	PI	Cas. PI$_{i_1 f}$	Cas. PI$_{i_{cf}}$	SPWM$_{LL}$	SVPWM$_{LL}$	LQI
0.00-0.33	6.6 + j5.78	5.7 + j5.78	183.85	230.11	229.24	229.82	230.02	230.02	230.00	0.05	-0.33	-0.08	0.01	0.01	0.00
0.33-0.66	6.6 + j5.78	5.7 + j5.78	229.81	231.05	229.33	229.62	230.02	230.29	229.95	0.46	-0.29	-0.16	0.01	0.13	-0.02
0.66-1.00	6.6 + j5.78	5.7 + j5.78	275.77	232.09	229.47	229.46	230.03	230.04	229.89	0.91	-0.23	-0.24	0.01	0.02	-0.05
1.00-1.33	50 + j5.78	42.5 + j5.78	183.85	230.95	229.68	230.12	230.02	230.02	230.20	0.41	-0.14	0.05	0.01	0.01	0.09
1.33-1.66	50 + j5.78	42.5 + j5.78	229.81	232.00	229.76	229.93	230.02	230.29	230.12	0.87	-0.11	-0.03	0.01	0.12	0.05
1.66-2.00	50 + j5.78	42.5 + j5.78	275.77	232.96	229.91	229.76	230.03	230.01	230.05	1.29	-0.04	-0.10	0.01	0.00	0.02
2.00-2.33	6.6 - j5.78	5.7 - j5.78	183.85	231.84	230.27	230.64	230.01	230.00	230.41	0.80	0.12	0.28	0.00	0.00	0.18
2.33-2.66	6.6 - j5.78	5.7 - j5.78	229.81	232.82	230.37	230.45	230.02	230.09	230.36	1.23	0.16	0.19	0.01	0.04	0.16
2.66-3.00	6.6 - j5.78	5.7 - j5.78	275.77	233.84	230.49	230.27	230.01	230.00	230.29	1.67	0.21	0.12	0.01	0.00	0.13
3.00-3.33	50 - j5.78	42.5 - j5.78	183.85	231.00	229.70	230.14	230.01	230.02	230.17	0.43	-0.13	0.06	0.01	0.01	0.07
3.33-3.66	50 - j5.78	42.5 - j5.78	229.81	232.05	229.78	229.96	230.02	230.08	230.13	0.89	-0.09	-0.02	0.01	0.03	0.06
3.66-4.00	50 - j5.78	42.5 - j5.78	275.77	233.01	229.93	229.79	230.03	230.00	230.05	1.31	-0.03	-0.09	0.01	0.00	0.02
4.00-4.33	6.6 + j0.00	5.7 + j0.00	183.85	230.97	229.80	230.32	230.01	230.01	230.25	0.42	-0.09	0.14	0.00	0.00	0.11
4.33-4.66	6.6 + j0.00	5.7 + j0.00	229.81	231.88	229.93	230.13	230.01	230.06	230.18	0.82	-0.03	0.06	0.01	0.02	0.08
4.66-5.00	6.6 + j0.00	5.7 + j0.00	275.77	232.94	230.03	229.96	230.01	230.07	230.13	1.28	0.01	-0.02	0.01	0.03	0.06
5.00-5.33	50 + j0.00	42.5+ j0.00	183.85	230.97	229.69	230.13	230.01	230.02	230.17	0.42	-0.14	0.06	0.01	0.01	0.07
5.33-5.66	50 + j0.00	42.5+ j0.00	229.81	232.02	229.77	229.94	230.02	230.10	230.12	0.88	-0.10	-0.03	0.01	0.04	0.05
5.66-6.00	50 + j0.00	42.5+ j0.00	275.77	232.98	229.92	229.78	230.03	230.00	230.05	1.30	-0.04	-0.10	0.01	0.00	0.02

Results assimilated through the implementation of PI, $Cascaded$-PI, $Lead$-Lag and optimal LQI controller for the control of the system of ES presented in Chapter:2 through Chapter:6, have been compared graphically (Fig:7.1 through Fig:7.9) and also these results have been presented in the abstract form in Table:7.1, to justify the comparative analysis.

Critical-load and grid voltage has been varied, keeping $V_{dc} = 750V$, $Z_g = 0.5 + j0.1\Omega$, and $Z_{nc} = 2.2 + j0\Omega$ fixed, at the instances presented in Table:7.1 for testing the performance of the controllers (except SVPWM Controlled system using *Lead-Lag* compensator, which is possessing 15% higher load).

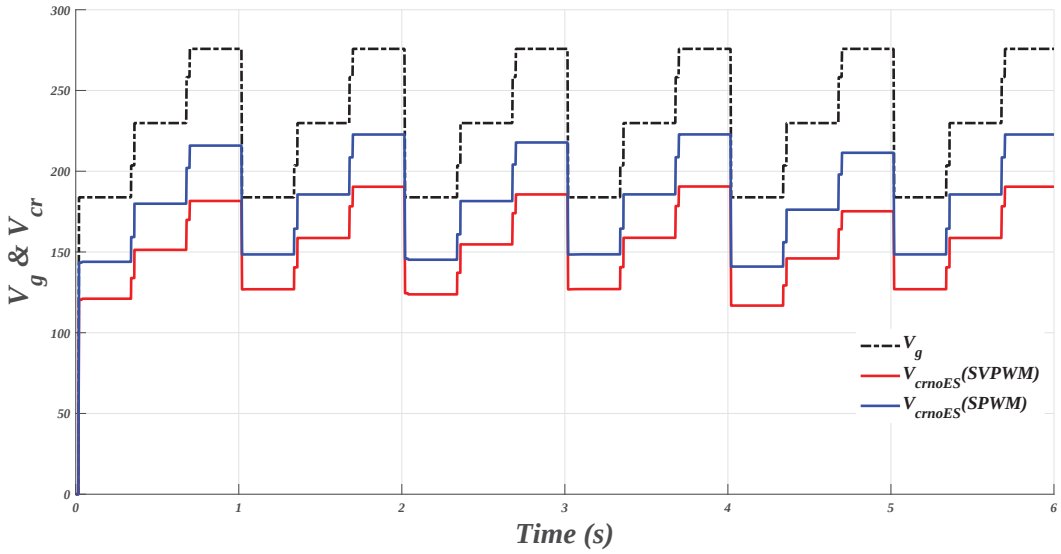


Figure 7.1: Results (RMS values) of having Step Changes Applied to V_g and Load, and corresponding V_{cr} in the absence of ES.

The alterations in the grid voltage, V_g and variations in V_{cr} (in the absence of ES), in the presence of fixed impedance of the cable, can be depicted from Fig:7.1, and the corresponding variation in the critical load can be witnessed from the plot of I_{cr} in Fig:7.7.

The performance of a typical controller can best be judged through the consistency and closeness of the quantity being controlled, i.e., V_{cr}, in following the reference signal (v_{ref}). The performance of V_{cr}, in tracking v_{ref}, can be depicted from Fig:7.2 and Table:7.1. The corresponding finding are:

- A *Lead-Lag* compensator exhibits the best performance, possessing a great accuracy in the case of $SVPWM$ controlled ES (seven instances of 0% regulation) and best precision in $SPWM$ controlled ES (sixteen instances of 0.01% regulation) along with good accuracy.

- As anticipated, the *Cascaded-PI* controller performs better than a PI controller, with a variation of -0.33% to 0.21% (in the case of feedback through i_{lf}) and -0.02%

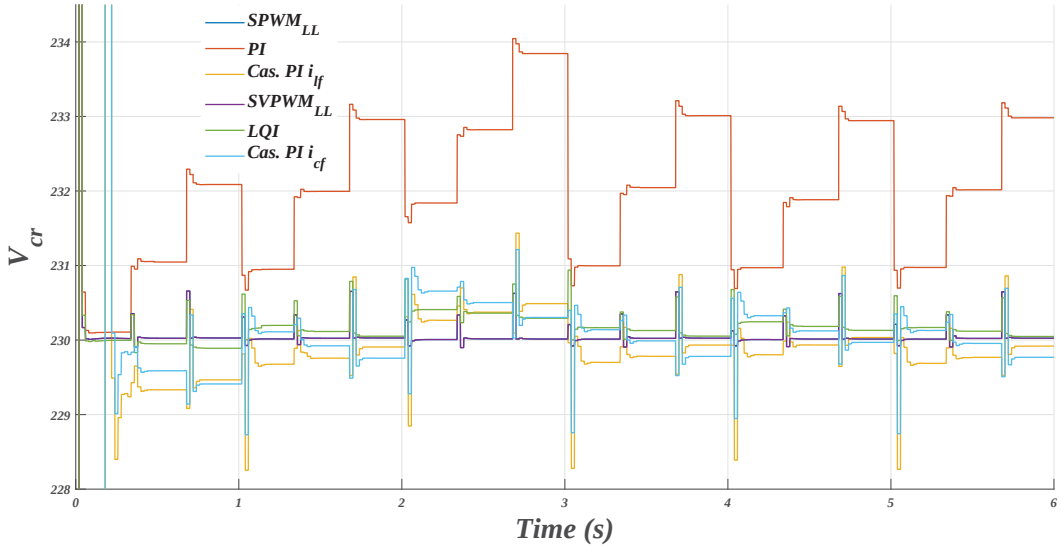


Figure 7.2: Variation in V_{cr} in the Presence of PI, $SPWM_{LL}$, $Cascaded\text{-}PI$, $SVPWM_{LL}$, and optimal-LQI Controlled ES, having Step Changes Applied to V_g and Load.

to 0.28% (in the case of feedback through i_{cf}), in the voltage regulation. $Cascaded\text{-}PI$ control executed through i_{cf} performs beter compared to that executed with i_{lf}.

- Performance of state feedback control of ES, using optimal LQI controller, is pretty close to that of a *Lead-Lag* controlled ES in terms of accurately following a sinusoidal command reference, as its voltage regulation varies in the very tight range of -0.05% to 0.16%.

- Worst performer amongst all is a PI controller, having a variation of 0.05% to 1.67%, in the voltage regulation.

- Worst transient performance can be seen from the $Cascaded\text{-}PI$ (through the feedback if i_{lf}) controller, in the wake of load change and grid voltage variation ($230 \pm 1.5V$). Further, a large start-up time is seen to be taken due to the inherently inferior start-up characteristic of $SOGI\text{-}PLL$ structure compared to what has been used with the rest of the controllers ($E\text{-}PLL$).

Looking at the variations in V_{nc} from Fig:7.3, a PI-controlled ES happens to extract the best voltage support through the non-critical load, in the case of Undervoltage situation ($V_g < 230V$). Voltage support provided through V_{nc} in $SVPWM$ controlled ES,

seems to be looking inferior. This so-called inferior performance is due to the presence of 15% higher non-critical load and higher Z_g, than other strategies, which is drawing more current and hence lesser voltage across it. In the rest of the conditions, all the strategies are at par, as far as the voltage support emanated by the non-critical load is concerned.

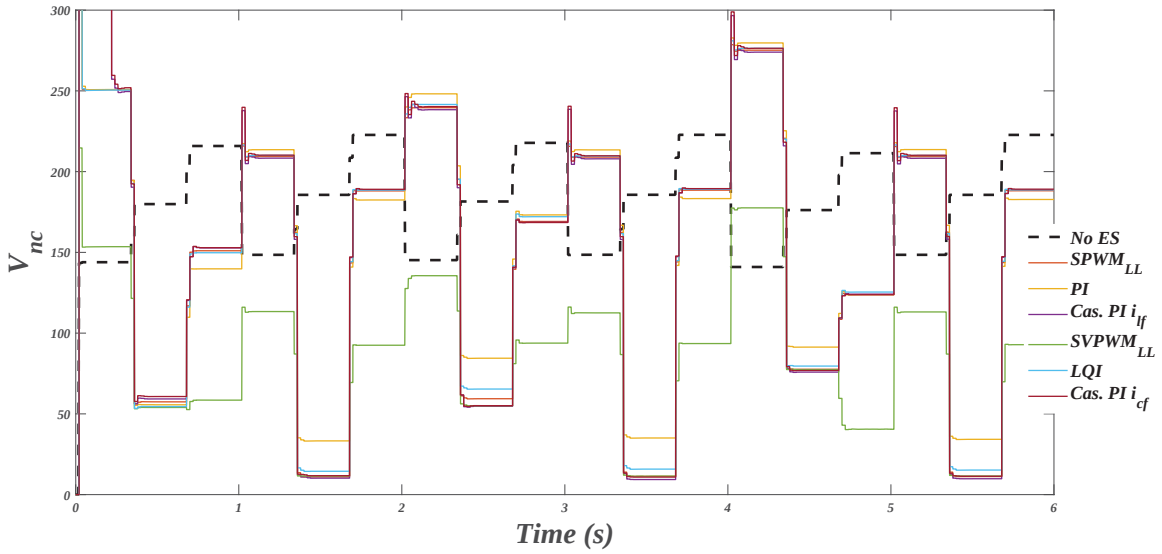


Figure 7.3: Variation in V_{nc} in the Presence of PI, $SPWM_{LL}$, $Cascaded\text{-}PI$, $SVPWM_{LL}$, and optimal-LQI Controlled ES, having Step Changes Applied to V_g and Load..

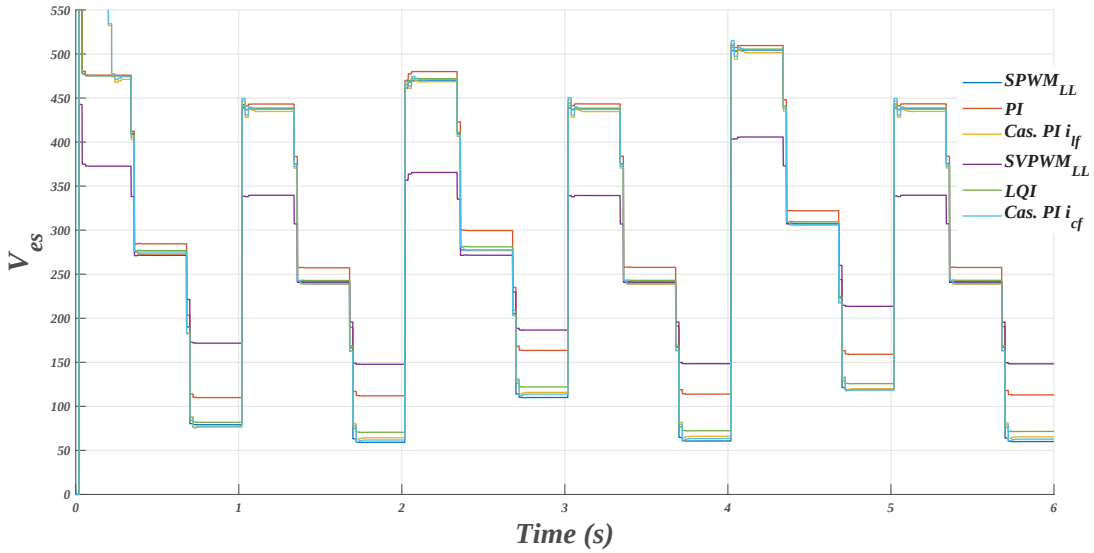


Figure 7.4: Variation in V_{es} in the Presence of PI, $SPWM_{LL}$, $Cascaded\text{-}PI$, $SVPWM_{LL}$, and optimal-LQI Controlled ES, having Step Changes Applied to V_g and Load.

Cohesively, non-critical load and ES, through the regulation of V_{nc} and V_{es}, is constituting a smart load by contributing towards the excellent regulation of voltage across the critical load. More the voltage support provided by the non-critical load, the lesser will be the effort required by ES and vice-a-versa. This could easily be seen from the complimentary behavior of Fig:7.4 and Fig:7.3. SVPWM controlled ES emanates the least voltage of all the strategies.

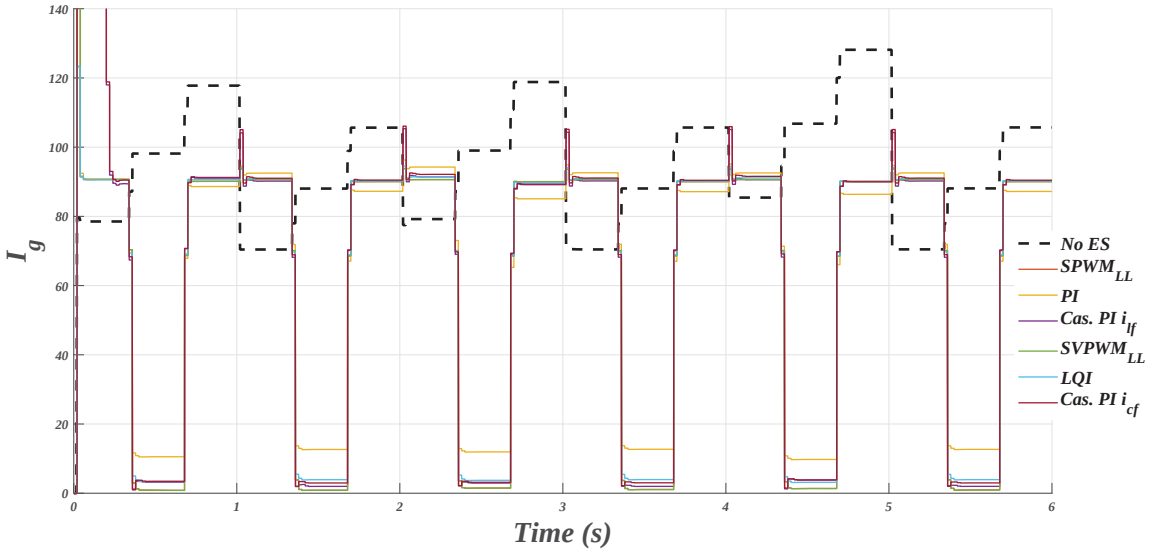


Figure 7.5: Variation in I_g in the Presence of PI, $SPWM_{LL}$, $Cascaded\text{-}PI$, $SVPWM_{LL}$, and optimal-LQI Controlled ES, having Step Changes Applied to V_g and Load.

Fig:7.5 shows the variation in I_g, with different control strategies of ES. I_g remains almost flat, in the under-voltage and over-voltage conditions, compared with a situation wherein the ES is not administering (large variation can be seen in I_g in the absence of ES) the voltage regulation. PI controlled system is drawing slightly higher current from the grid than the other strategies, in the case where v_g is close to v_{ref} indicating the crudeness of the control.

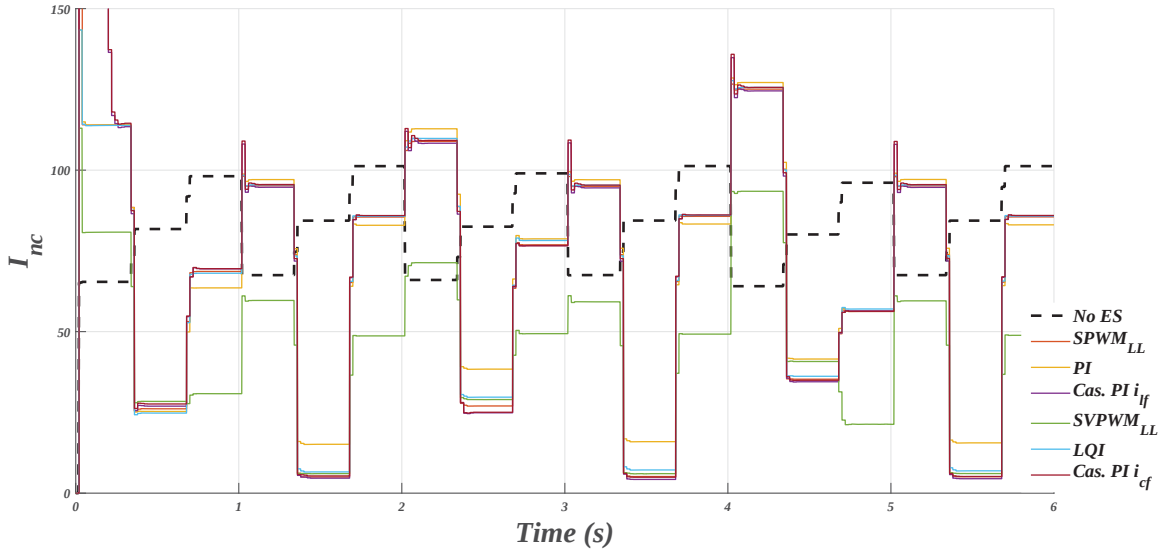


Figure 7.6: Variation in I_{nc} in the Presence of PI, $SPWM_{LL}$, $Cascaded\text{-}PI$, $SVPWM_{LL}$, and optimal-LQI Controlled ES, having Step Changes Applied to V_g and Load.

I_{nc} is complimenting the response of V_{nc}, due to constant power characteristic of non-critical load, and the same can be reflected from Fig:7.6

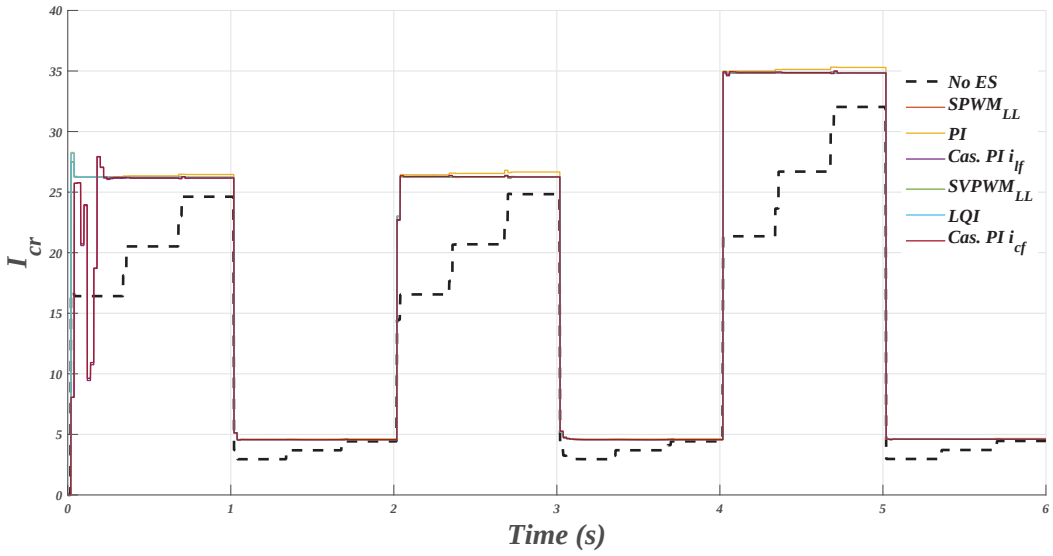


Figure 7.7: Variation in I_{cr} in the Presence of PI, $SPWM_{LL}$, $Cascaded\text{-}PI$, $SVPWM_{LL}$, and optimal-LQI Controlled ES, having Step Changes Applied to V_g and Load.

Current I_{cr}, remains constant for a typical load variant as depicted from the Fig:7.7, contrary to the large variations of the same in the absence of ES amidst perturbing grid

voltage.

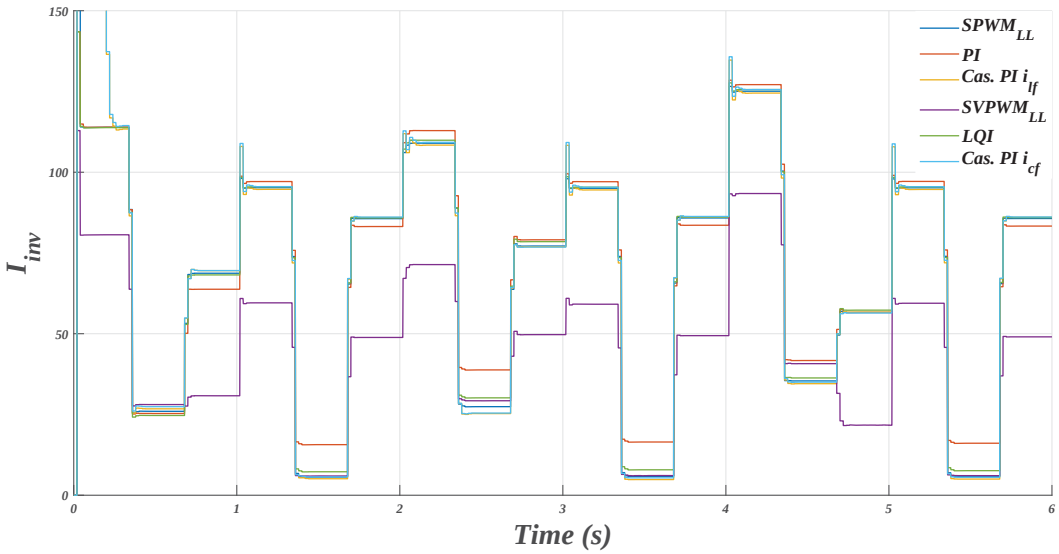


Figure 7.8: Variation in I_{inv} in the Presence of PI, $SPWM_{LL}$, $Cascaded\text{-}PI$, $SVPWM_{LL}$, and optimal-LQI Controlled ES, having Step Changes Applied to V_g and Load.

A minimal inverter current I_{inv} can be seen to be flowing (shown in Fig:7.8), in the case where grid voltage is close to the reference voltage. ES merely compensates for the voltage drop that is taking place across the grid impedance Z_g. Least I_{inv} can be noticed to be there in the case of SVPWM Lead-Lag controlled ES, witnessing the lowest VSC's rating.

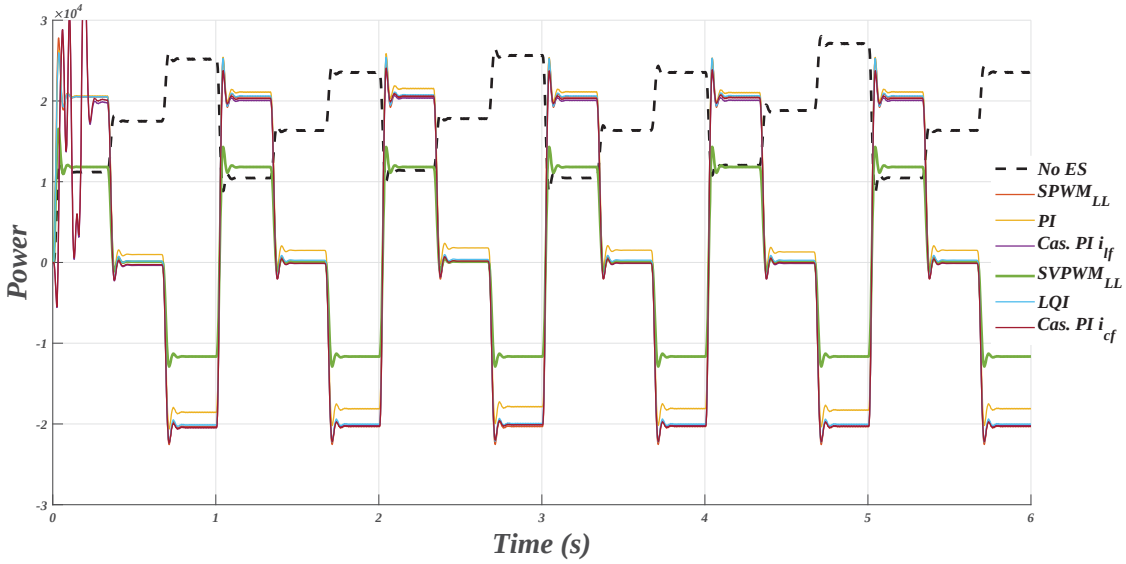


Figure 7.9: Variation in *Power* in the Presence of PI, $SPWM_{LL}$, *Cascaded-PI*, $SVPWM_{LL}$, and optimal-LQI Controlled ES, having Step Changes Applied to V_g and Load.

Fig:7.9 shows the exchange of power that is taking place between the grid, load, and ES. "$+Ve$" sign signified the injection of power from ES, and "$-Ve$" sign signifies the absorption of power through ES, in the under-voltage and over-voltage scenarios, respectively. The performance of ES in all the control strategies, except $SVPWM$-controlled ES, is at par. The highest peak power shaving ($9.9KW$ compared to around $7KW$ in the rest of the strategies) could be seen to be earmarked by $SVPWM$ control, though it has been incorporated with the 15% higher load and the larger grid impedance compared to the others.

7.3 Testing the Robustness of PI, *Cascaded-PI*, *Lead-Lag* and Optimal-LQI Controllers

Robustness of the system, against the parametric excursions, has been made more stringent by adding two more uncertainties in the form of step changes applied to V_{dc} and Z_g over and above the pre-existent uncertainties, and the same have been tested with all the six control strategies. The simulation test-bench presented in 2.14 has been updated with switchable DC-bus, and Z_g as could be seen from Fig:7.10. The operational source of

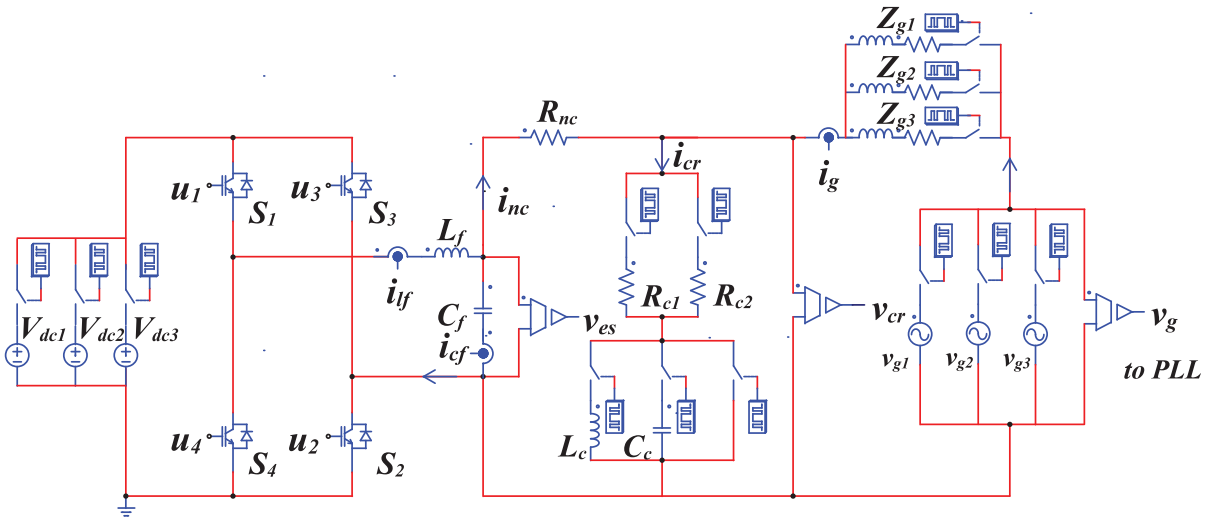


Figure 7.10: Simulation Test Bench for Testing the Performance of ES and hence Controller.

second-generation *ES* is dependent on the battery potential, which is dependent on the Load and its state of charging. V_{dc} has been made to very in the range of 550V to 750V with a step change of 100V applied at an interval of every 18s.

Grid impedance (Z_g), as mentioned in Sec:2.6, is primarily dependent on the connecting length of the conductor and the amount of the connected load. In the urban load condition, the secondary distribution system's feeder length is not exceeding 1KM. "Dog" conductor has been considered for the assumed load having a conductor length less than 1KM. Z_g has has been varied in the steps as $Z_{g1} = 0.5 + j0.1\Omega$, $Z_{g2} = 0.65 + j0.2\Omega$ and $Z_{g3} = 0.8 + j0.3\Omega$, with a periodicity of 6s.

The system possessing all these possibilities of parametric variations, as can be seen from Fig:7.11, has been tested with all the four controllers (having two sub variants of *Cascaded-PI* and *Lead-Lag* control) presented in Chapter:4, Chapter:5, and Chapter:6. The corresponding results pertaining to the variation in V_{cr}, has been presented in the Fig:7.12 through Fig:7.17, to evaluate the robustness of *ES* under all the possibilities of parametric excursions presented in Sec:2.4.1.

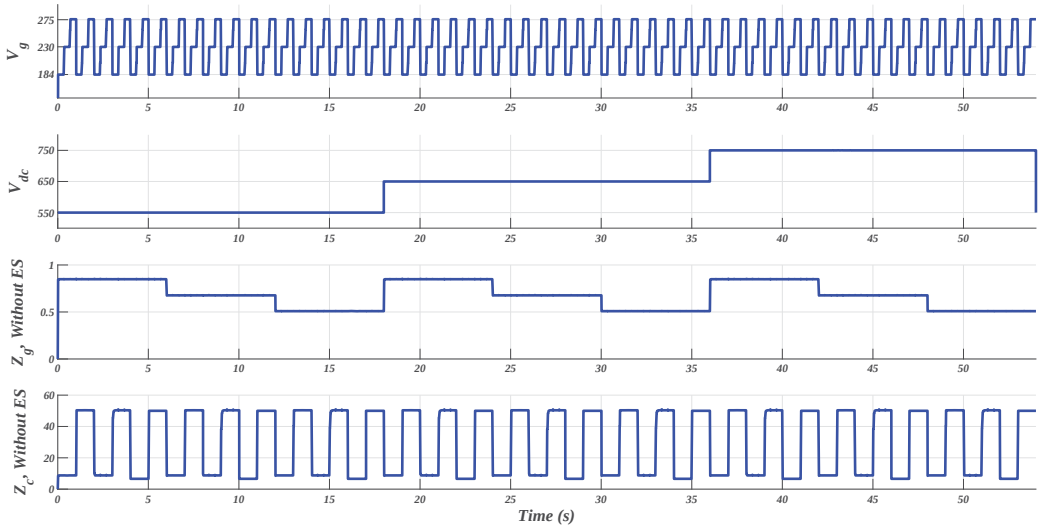


Figure 7.11: Variations Applied to V_g, Z_g, V_{dc} and Critical Load (Z_c).

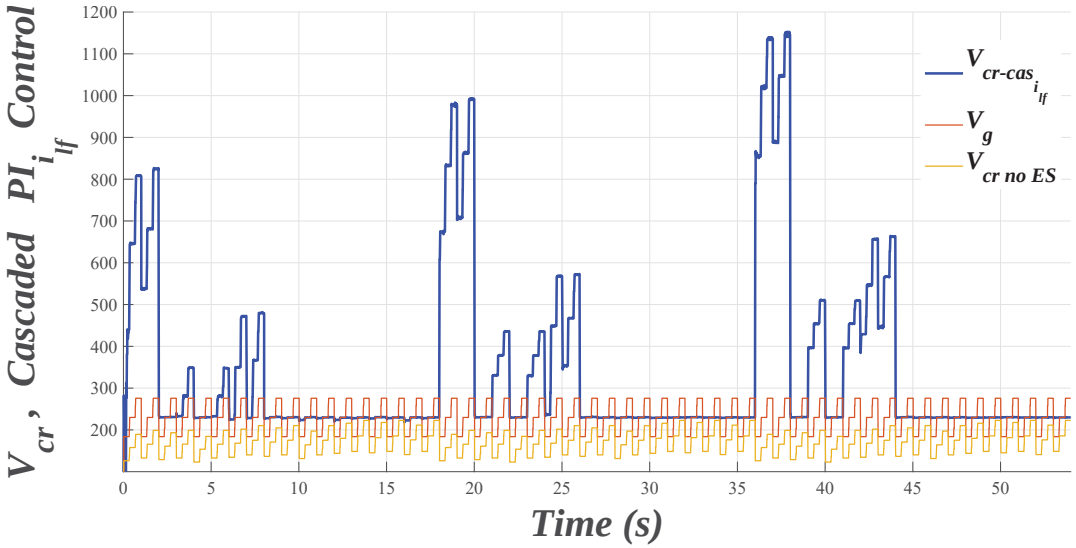
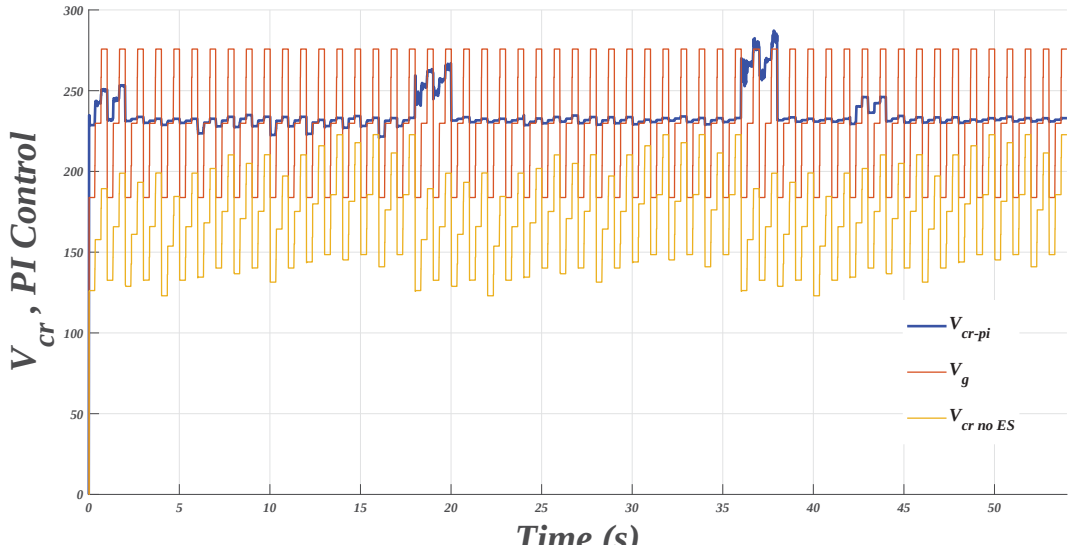


Figure 7.12: Performance Evaluation of $Cascaded\text{-}PI$ Controlled ES (inner loop feedback from i_{lf}), through V_{cr}, having Step Changes Applied to V_g, Z_g, V_{dc} and Z_c.



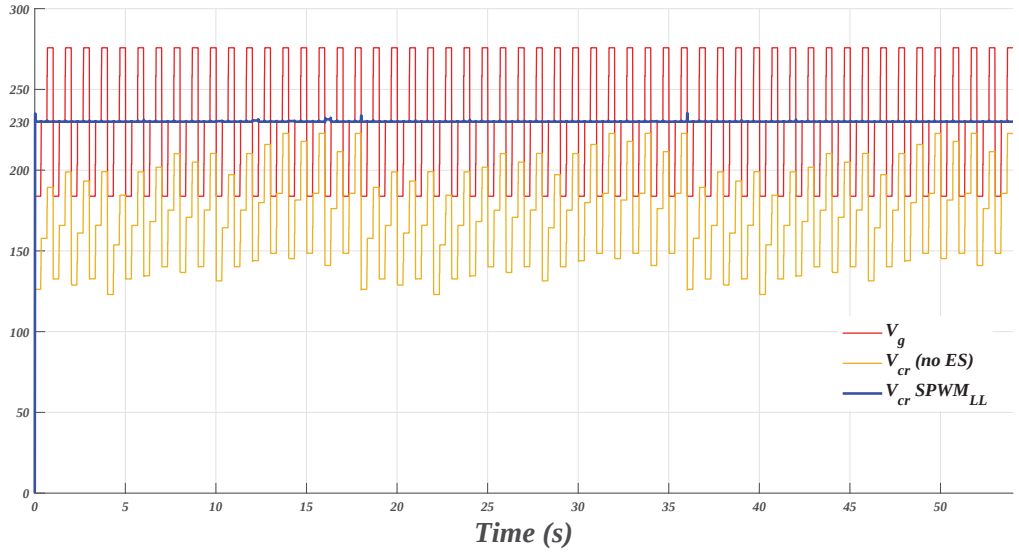


Figure 7.14: Performance Evaluation of *Lead-Lag* compensated and $SPWM$ Controlled ES, through V_{cr}, having Step Changes Applied to V_g, Z_g, V_{dc} and Z_c.

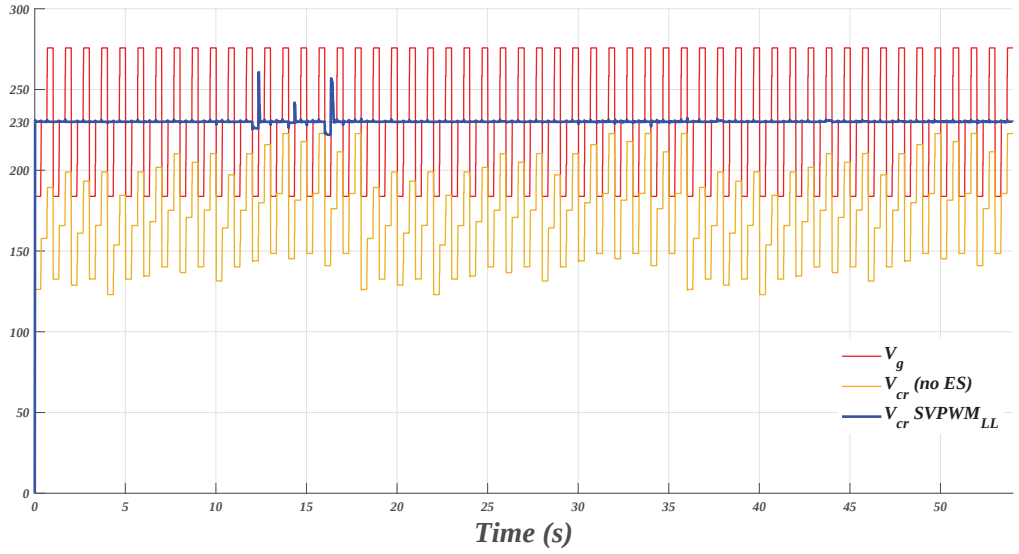


Figure 7.15: Performance Evaluation of *Lead-Lag* compensated and $SVPWM$ Controlled ES, through V_{cr}, having Step Changes Applied to V_g, Z_g, V_{dc} and Z_c.

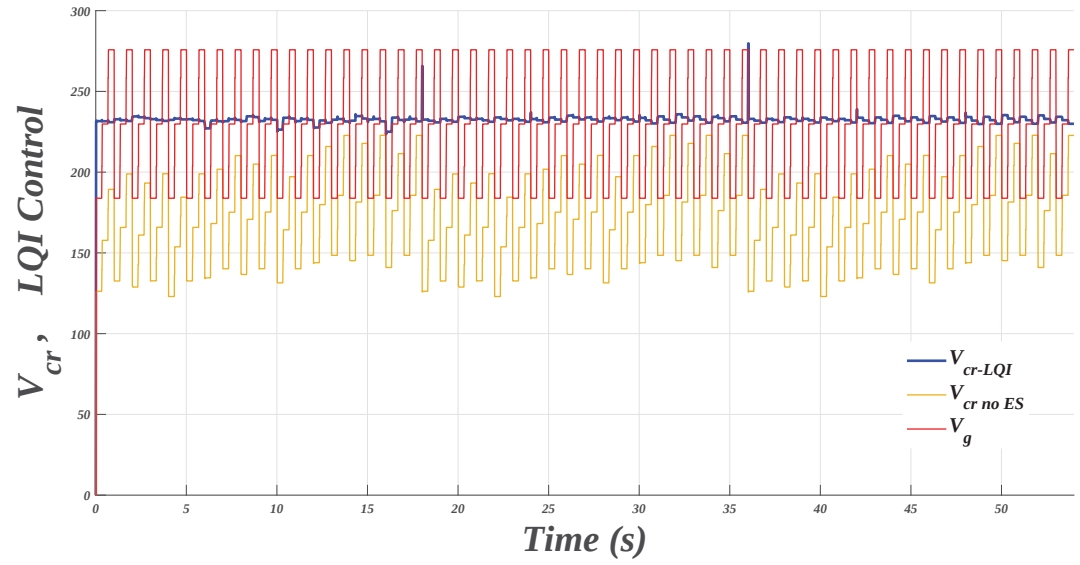


Figure 7.16: Performance Evaluation of Optimal LQI Controlled ES, through V_{cr}, having Step Changes Applied to V_g, Z_g, V_{dc} and Z_c.

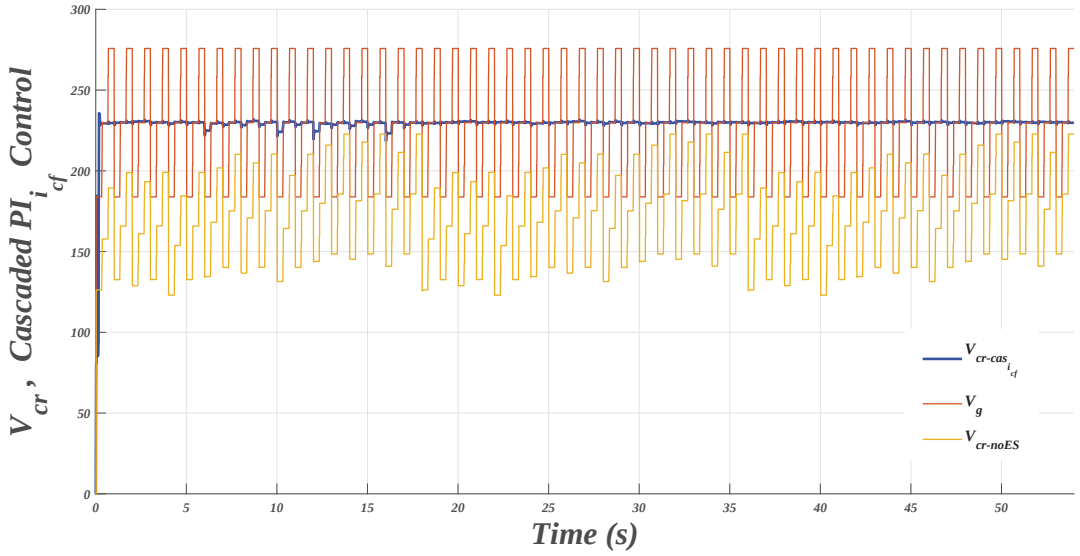


Figure 7.17: Performance Evaluation of $Cascaded\text{-}PI$ Controlled ES (inner loop feedback from i_{cf}), through V_{cr}, having Step Changes Applied to V_g, Z_g, V_{dc} and Z_c.

7.4 Performance Analysis of Robustness

Robustness of the proposed controllers (PI, $Cascaded\text{-}PI$, $Lead\text{-}Lag$, and Optimal LQI) have been tested through the application of variations in V_g, Z_g, V_{dc} and Z_c, mimicking the

uncertainties in the parameters of the system of ES presented in Fig:7.10. Analyzing the results (Fig:7.12 through Fig:7.17, showing the variation in V_{cr}, with and without ES), achieved through the test-bench, following significant observations can be summarized:

- $SPWM$ controlled *Lead-Lag* compensated ES gives out smoothest performance as can be seen from Fig:7.14. The voltage, V_{cr} could be seen to be varying in the range of 229.5V to 235.2V with a corresponding voltage regulation of -0.22% to 2.26%. The result shows no transient spikes, in the presence of applied step changes leading to parametric alterations.

- The next good performer is $SVPWM$ controlled *Lead-Lag* compensated ES gives out smoothest performance as can be seen from Fig:7.15. Three spikes (the largest one having a peak of 260.7V) could be seen between 12s to 17s. The voltage, V_{cr} could be seen to be varying in the range of 229.3V to 230.7V (in steady-state) with a corresponding voltage regulation of -0.3% to 0.3%.

- *Cascaded-PI* controller, having feedback for inner loop being received from the current flowing through the filtering capacitor (i_{cf}) of ES, exhibits the smooth and robust performance as can be seen from Fig:7.17, amidst the uncertainties presented in Sec:7.3, in the form of parametric excursions. The performance of this controller has no significant spikes. The voltage, V_{cr} could be seen to be varying in the range of 223.2V to 230.8V with a corresponding voltage regulation of -2.95% to 0.40%.

- State feedback control executed through Optimal LQI controller, exhibits the anticipated robustness in its performance as can be seen from Fig:7.16, amidst the uncertainties presented in Sec:7.3, in the form of parametric excursions. The only change that has been made in the controller is in the form of $K_i = 2500$ (whose Bode plot and Step response plot have been presented in Fig: 6.3 and Fig: 6.4, respectively), to expand the bandwidth of the controller. Though the performance of the controller is not that smooth as the one presented in Table:6.2 and Fig:6.5 (in the form of variation in V_{cr}). Neglecting the two larger spikes (of 265V and 280V respectively) at the transition of V_g, Z_g, V_{dc} and Z_c, at 18^{th}s and 36^{th}s, the variation in V_{cr}) could be seen to be varying in the range of 226V to 236V (corresponding voltage regulation is -1.74% to 2.61%).

- PI controller performed somewhat better than $Cascaded\text{-}PI$ control (executed through i_{lf}), though it fails to comply with the robustness test, and the same can be envisaged from Fig:7.13.
- Worst performance of all, can be witnessed through Fig:7.12, of the $Cascaded\text{-}PI$ control executed through the feedback of i_{lf}, showing spikes at almost all transitioning instances and utterly fails to comply with the robustness test.

7.5 Conclusion

Comparative performance analysis of PI, $Cascaded\text{-}PI$ (inner loop executed through i_{lf} and i_{cf}), $Lead\text{-}Lag$ ($SPWM$ and $SVPWM$), and Optimal LQI controllers have been presented here in this chapter, considering two distinct situations of parametric excursions, as (a) varying critical-load and grid voltage, keeping $V_{dc} = 750V$, and $Z_g = 0.5 + j0.1\Omega$ fixed, and $Z_{nc} = 2.2 + j0$, and (b) applying variations in V_g, Z_g, V_{dc} and Z_c. All the controllers have performed satisfactorily, under the limited parametric variation presented in condition (a), where the $Lead\text{-}Lag$ controlled ES emanated the best performance of all. Robustness of the designed controllers has been tested through the application of condition (b), in which all the controllers (except PI and $Cascaded\text{-}PI$ control executed through i_{lf}) performed robust enough, against full range of parametric excursions. $SPWM$ control emanated the best performance, followed by $SVPWM$ control, $Cascaded\text{-}PI$ control executed through i_{cf} and optimal LQI control, by giving satisfactory compliance to the norm of robustness, and sufficient bandwidth, against a broader range of parametric variations. The PI and $Cascaded\text{-}PI$ controller executed through i_{lf} has failed to qualify the robustness test.