Chapter 8

Conclusion and Future Work

8.1 General

The development of custom power device, ES, its controllers and its use in the secondary distribution networks can provide the voltage regulation and hence giving compliance to the notion of DSM in the real-time, in the presence of intermittent RES. This thesis has addressed the design and development of different controllers, that could be used with the ES, to furnish the voltage regulation to the critical load of an individual consumer, amidst perturbing grid and load conditions. The main contribution of the thesis includes the development of,

- the converter acting as ES along with its test-bench and the mathematical model. The developed mathematical model and test-bench could be used to develop the controller and its performance evaluation through the implementation of different control strategies, amidst parametric variations. This has been the subject mater of Chapter: 2.

- Phase-locked-loop structure, which happens to be a component of great significance in the control of grid-tied converters, such as ES. Two of the diverse and robust PLL structures, (a) $SOGI\text{-}PLL$ and (b) $E\text{-}PLL$, have been designed and implemented with the control of ES in Chapter: 3.

- the classical and commonly used controller, i.e., a PI controller, which happens to be a contender being used for the control of DC quantities, has been presented in

Chapter:4. Based on the foundation of a PI controller's design, a Loop-in-loop construct called $Cascaded\text{-}PI$ controller (employing two different feedback mechanism of inner current loop, through i_{lf} and i_{cf}) has been developed for enhancing the controllability of the current through observation of an additional state.

- a *lead-Lag* compensator employing *pole-zero* cancellation and pole placement technique has been introduced in Chapter:5. The designed $Lead - Lag$ compensator has been tried with the 1-ϕ ES being controlled using (a) $SPWM$ control, and (b) $SVPWM$ control, by deploying a fixed frequency switching technique.

- LQR control, and the steady-state error minimization through addition of an integrator to it, in Chapter:6. To achieve the optimal controllability of ES, the LQR has been optimized through the concept of convex numerical optimization technique of Linear Matrix inequalities. Thus optimized LQR controller with an integrator, has been implemented using state-feedback control with an assumption of observability of all the states, so as to get robustness in control, against the numerous possibilities of parametric variations.

- a comparative analysis in Chapter:7, comparing the performance of the different benchmark parameters associated with the performance of ES. The robustness of the developed controllers have also been verified, in the presence of largest possible spectrum of parametric uncertainties that might exist in a real distribution system.

The findings of the work executed in the previous chapters, have been summarized in this chapter, and the suggestive enhancements that could be executed by extending the prevailing research, have been proposed in the form of scope for future research.

8.2 Summary of the Important Findings

The findings of the work that has been carried out, has been summarized as follows:

- In Chapter: 2, a basic system of the ES comprising the converter acting as ES, catering regulated voltage to the critical load, has been developed through the support extended by the non-critical load. A state-space model of the system of ES has been derived, which could be used to design the controllers. The VSC supposed to

act as ES is evaluated for its compliance to the harmonics standards, in the absence of a closed loop controller. To investigate the voltage regulating functionality of the ES, the developed system has been simulated in the absence of ES. The results of the test system reveal following facts:

1. Improvisation in the % regulation that is needed to be furnished through ES is 3.13% to 38.72%, in the presence of variation in Load and grid voltage.
2. Variation in the grid voltage is causing variation in I_{cr}, for a typical load type, which may be yet another issue to be addressed.

- PLL structure is of paramount importance in a grid-tied converter's satisfactory operation, such as ES, and the same has been the subject matter of Chapter: 3, and the findings pertaining to that are:

  1. Design and implementation of $SOGI\text{-}PLL$ are far more complicated as it represents a 5^{th} order controller, as that compared to a 2^{nd} order controller in the case of $E\text{-}PLL$.
  2. $SOGI\text{-}PLL$ is taking a significantly larger start-up time ($0.1s$) than compared to $E\text{-}PLL$ ($< 40ms$).
  3. $E\text{-}PLL$ is a better choice for ES application and has been successfully implemented with the PI, *Lead-Lag* and *Optimal-LQI* controlled ES.
  4. $SOGI\text{-}PLL$ has been implemented with the $Cascaded\text{-}PI$ controlled ES, for the sake of performance evaluation of the said PLL and comparison, and the corresponding results signify a considerable start-up delay in the case of $SOGI\text{-}PLL$.

- A PI controller is the most presented controller, for the control of ES. It is simple to design and implement and hence the same has been chosen to be the founding basis and the subject mater of the Chapter: 4. Following are the findings of the results associated with the PI and $Cascaded\text{-}PI$ controlled ES:

  1. PI-controlled ES gives regulation in the range of 0.05% to 1.67%, which happens to be the inferior most performance of all.
  2. A $Cascaded\text{-}PI$-controlled ES performs better than a classical and single PI-controlled ES, in terms of its voltage regulating capabilities, through a smaller

converter (ES) rating. This better performance of cascaded PI-controlled ES has been made possible due to the additional degree of freedom available in the form of control of one more parameter (i_{inv} through i_{lf}) of the ES, over and above the conventional control of voltage signal (v_{cr}) that has been present with both the control strategies of ES.

3. Another possibility of the inner loop has been explored through the filter capacitor's current feedback in the form of i_{cf}. Feedback for the inner-loop received from i_{cf} gives better voltage regulation, as average regulation is 0.005%, compared to -0.074%, in the case of feedback received in the form of i_{lf}. The better performance is the end result of control over i_{inv} and i_{nc} through the control of i_{cf}, and this also has been the reason of its cost-effectiveness, as it achieves this by measuring only 2% current in the form of i_{cf} of that of i_{lf}.
4. Further, a *Cascaded-PI* controller with feedback received from i_{cf} proves to be satisfying the criterion of robustness, whereas its counterpart (having feedback through i_{lf}) fails to prove the same in the presence of a complete spectrum of the parametric variation, and same is the case with a PI controlled ES.

- In Chapter: 5 a *Lead-Lag* compensator has been prsented, with following outcomes:

1. A $Lead - Lag$ compensator offers the most incredible accuracy in the case of $SVPWM$ controlled ES (seven instances of 0% regulation)
2. $SPWM$ controlled ES offers best precision (sixteen instances of 0.01% regulation) along with reasonable accuracy.
3. $SVPWM$ controlled ES gives better compliance to harmonic reduction and makes the output distortion-free, and, at the same time, reduced switching losses and efficiency, compared to $SPWM$ control.
4. $SVPWM$ controlled ES gives more output (approximately 15% more), and the same has been verified by increasing the critical and non-critical loads by 15% and even then getting the same performance that has been achieved through $SPWM$ controlled ES.
5. As far as the controller's robustness is concerned, both $SVPWM$ and $SPWM$ control perform well, with the absolute test of robustness. $SPWM$ control is at its best in terms of % Regulation. $SVPWM$ control performs as well,

except at gross three instances of transients presented in the form of spikes (largest one is of 260V).

6. $SVPWM$ control offers excellent peak power shaving ($9.9Kw$), though it has been operating with 15% higher load, and also been operating with smaller rated ES.

- In Chapter: ch6:LQR-LMI, state feedback control of ES has been designed using *Optimal-LQI* controller, having following findings:

  1. It exhibits excellent robustness against absolute parametric excursions (spectrum of variation in all the parameters, i.e., v_g, V_{DC}, Z_g and Load) with limited accuracy.
  2. The same controller offers excellent accuracy in the case of limited parametric variations (in v_g and Load only), and small demand for control energy. This satisfies the challenging task of negotiating with the conflicting controller requirements, thanks to numerical convex optimization of state feedback controller gain, being carried out through a simple method of LMIs.

- Chapter: 7 has been accommodated with the comparative analysis of the results gathered through the implementation of PI, $Cascaded\text{-}PI$, *Lead-Lag*, and *Optimal-LQI* controlled ES (presented in Chapter: 4 through Chapter: 6), having,

  1. limited uncertainties presented in the form of variation in v_g and *Load*, and
  2. absolute range of uncertain parametric variations, comprising of variation in v_g, V_{dc}, Z_g and *Load*.

  Concise, steady-state results associated with both the above mentioned uncertain conditions has been assimilated in Table:8.1 (with an appropriate condition number marked as superscript), depicting the performance of ES as a voltage regulator, and as a mechanism complying the real-time DSM. ES being controlled by $SPWM$ and $SVPWM$ control executed through *Lead-Lag* compensator, $Cascaded\text{-}PI$ controller (having feedback through i_{cf}), and *Optimal-LQI* controller, are satisfactorily complying with the condition of robustness amidst absolute range of uncertain parametric variations (condition 2).

Table 8.1: Abstract Concluding Remarks of Results gained through Different Controllers.

Controller	% Regulation (v_{cr})		Power Shaving (W)	Robustness
	Lower Limit	Upper Limit		
No ES[1]	-3.13	38.72	-	-
No ES[2]	-3.13	46.52	-	-
PI[1]	0.05	1.67	5845	-
Cascaded PI[1] (i_{lf} as feedback)	-0.33	0.21	6644	-
Cascaded PI[1] (i_{cf} as feedback)	-0.24	0.28	6612	-
Lead-Lag (SPWM)[1]	0.00	0.01	7730	-
Lead-Lag (SVPWM)[1]	0.00	0.10	9908	-
Optimal LQI[1]	-0.05	0.18	6671	-
Lead-Lag (SPWM)[2]	-0.22	2.26	5690	$\surd$
Lead-Lag (SVPWM)[2]	-0.3	0.3	6530	$\surd$
Optimal LQI[2]	-1.60	2.54	2330	$\surd$
Cascaded PI[2] (i_{cf} as feedback)	-2.95	0.40	6463	$\surd$

*Note**: Subscript [1] indicates Limited parametric variation (i.e., in v_g and Z_{cr}), and Subscript [2] indicates absolute range of uncertain parametric variations (i.e., in v_g, Z_{cr}, V_{dc}, and Z_g).

8.3 Scope for Future Research

Consequent to investigations carried out in this thesis, the following points could be marked as the work that could not be furnished in the prevalent work due to time constraints and could be executed with new research as an extension of this work by considering this work as a founding basis.

- The presented controllers have been designed, keeping in view the stiff grid conditions. The same work could be extended for the weak grid through freshly designed controllers and PLL structures.

- the $SOGI\text{-}PLL$ structure, being used with the cascaded PI control of ES (case with the feedback received from i_{cf}), has proved its worth through satisfactorily providing the compliance to the criterion of robustness. This has proven the merit of $SOGI\text{-}PLL$, but is having a larger start-up delay, and this needs some fresh way or redesign of said PLL structure with improved start-up time.

- Constraint, due to unavoidable circumstances has not permitted us to implement the presented controllers to be implemented with the hardware. This aspect of

hardware implementation could be addressed in some new research by extending this work.