Chapter 4
Modeling and Analysis of Active Power Filters

Chapter provides a comprehensive study of the work done by the researchers for the modeling and analysis of active power filter.

4.1 DC **model of a Series Active Filter**

The section includes transient analysis of a series active filter integrated with a double-series diode rectifier. A dc model is described [1] with the help of the p-q coordinate transformation, which can be used to accurately and simply analyze transient characteristics around the fundamental frequency of the integrated system.

Pulse width-modulated (PWM) rectifiers consisting of the same power circuit topology as PWM inverters have shown promise in meeting the guidelines for harmonic mitigation [2-5]. The increased cost and switching loss caused by PWM, however, would make a high-power PWM rectifier rated at 1–10 MW economically impractical. The authors have proposed a new ac/dc power conversion system providing a solution to the above-mentioned problems hidden in PWM rectifiers [6]. A small-rated series active filter for the purpose of achieving harmonic compensation is integrated with a large-rated double-series diode rectifier for the purpose of performing ac/dc power conversion. The active filter enables the diode rectifier to draw three-phase sinusoidal currents from the utility. In addition, the active filter based on supply current detection is characterized by closed-loop control with a relatively high feedback gain.

Appropriate control parameters of the series active filter have to be designed to achieve a stable and reliable system. The transient response of the integrated system should also be taken into consideration to avoid over voltage at the dc side. The over voltage may cause magnetic saturation of matching transformers and voltage breakdown of switching devices. The system consisting of a diode rectifier exhibits nonlinear property, and therefore it is an extremely tough work to directly analyze it. A simple and effective approach is required. The stability analysis of the active filter has been discussed in [7]. Nothing in the literature, however, has been published regarding transient analysis of the integrated system of a series active filter with a diode rectifier during a dc-load change.

The model [1] is developed with the help of the p–q coordinate transformation. It can be used to accurately and simply analyze transient characteristics at the dc side of the system around the fundamental frequency, instead of achieving the analysis taking into account the behavior of switching devices. Moreover, it is useful for parameters design in the controller of the active filter. This analysis makes the following assumptions; the system is balanced, and the three-phase supply currents are continuous; the supply current harmonics are not so large as to affect transient characteristics; the dc load is resistive; and the three-phase power system is stiff. Analytical results conclude that either increasing the active filter gain or decreasing the cutoff frequency of low-pass filters in the harmonic detector results in a slow response, and cause a large and long transient of the dc voltage.

4.1.1 Dynamic Models for Power Electronic Systems

A great deal of research on analytical dynamic models for power electronic systems has been carried out over the past three decades. Modeling and analysis of the power electronic systems are very complicated because of their switching behavior. This difficulty, however, has brought a great challenge and interest to theoretical researchers, control engineers, practical engineers, and/or even mathematicians. The so-called state-space averaging method has become one of the most popular tools for the modeling and analysis. This method has been discussed theoretically in much of the literature [8-11]. References [12-13] have applied the method to transient analysis and control system design. Besides the averaging method, a sampled-data approach [14], a Fourier-analysis-based approach [15], a frequency-domain analytical model [16], and a harmonic-neglecting-based approach [17-18] have been also proposed for analysis and design.

In addition, the effort of overcoming the difficulty in frequency difference between the ac and dc sides of an ac/dc converter has resulted in analysis based on phasor transformation [19] or d–q transformation [20-22]. These methods have been actually used to analyze and design the dynamic behavior of power electronic systems effectively. It should be noted that this paper replaces the d-q transformation with the p-q transformation. The "p –q " may be used to avoid any confusion with the subscript "d" that is used to refer to dc-side circuit parameters. [8-22] have discussed a single-converter system. Moreover, the resultant circuits, and/or mathematics models from those works are still too difficult to be directly applied to transient analysis or control system design of a large system, because of their complexity. It seems that no literature has been published regarding a dynamic model of multiconverter systems such as an integrated system of a 12-pulse diode rectifier with a series active filter. The system is much more complex than a single-converter system, because it includes two converters with different switching frequencies; a line-frequency- based diode rectifier and a high-frequency-based active filter. A design of a 12-pulse diode rectifier system has also been discussed in the literature [23]. However, the design is still based on simulation.

4.1.2 System Configuration

Fig. 4.1 shows a harmonic-free ac/dc power conversion system [6]. It consists of a combination of a double-series diode rectifier rated at 20 kW and a series active filter with a peak voltage and current rating of 22 kVA. The series active filter consists of three single-phase matching transformers and three single-phase H-bridge voltage-fed PWM inverters. The ac terminals of each PWM inverter are connected in series with a power line through a single-phase matching transformer. The double-series diode rectifier consists of three phase Y- Δ- and Δ –Δ connected transformers and two three phase diode rectifiers. The primary windings of the transformers are connected in series with each other. The dc terminals of the diode rectifiers and the active filter form a common dc bus equipped with an electrolytic capacitor. This results not only in eliminating any electrolytic capacitor from the active filter but also in reducing current ripples flowing into the electrolytic capacitor across the common dc bus.

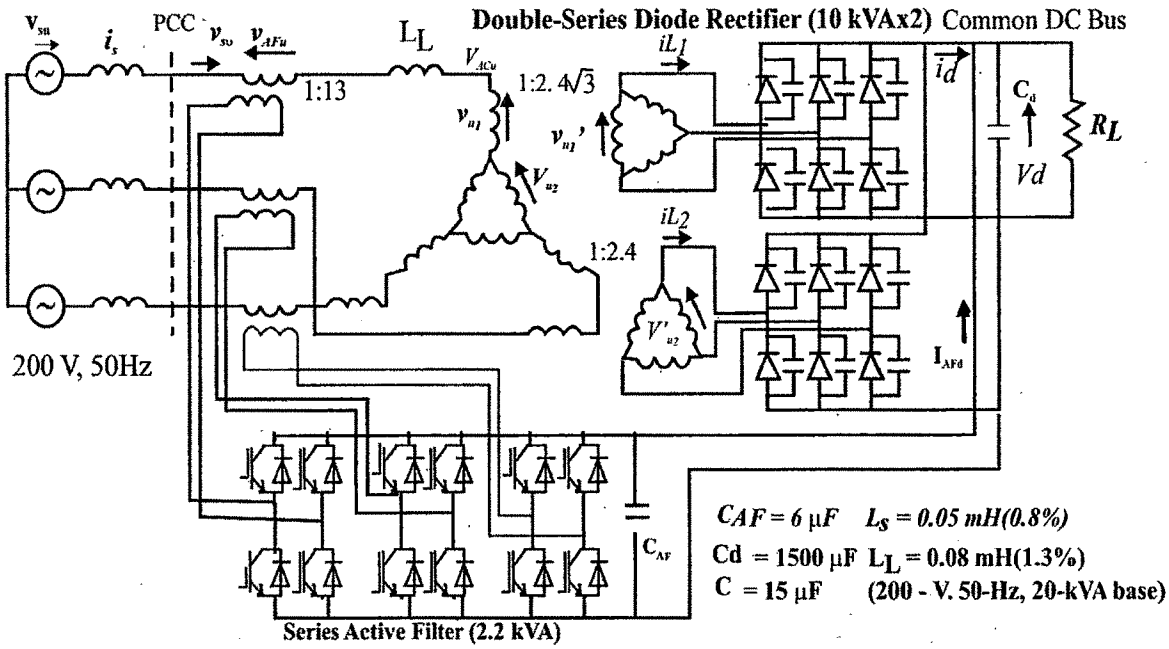


Fig 4-1 Harmonic Current –free ac/dc Power Conversion System

The active filter of Fig 4.2 is controlled so as to offer zero impedance for the fundamental frequency and to act as a resistor with high resistance of K(Ω) for harmonic frequencies [24].

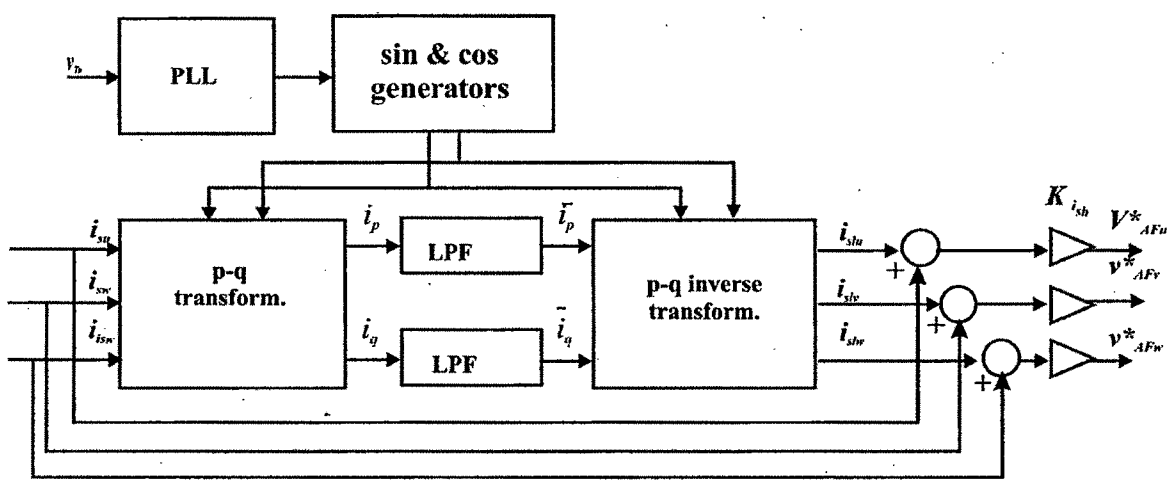


Fig 4-2: Control Circuit of Series Active Filter

Fig 4.3 depicts the equivalent circuit of the system [1]. The model simplifies the system so that the transient characteristics of the system can be calculated, which is useful for the design in control parameters of the active filter.

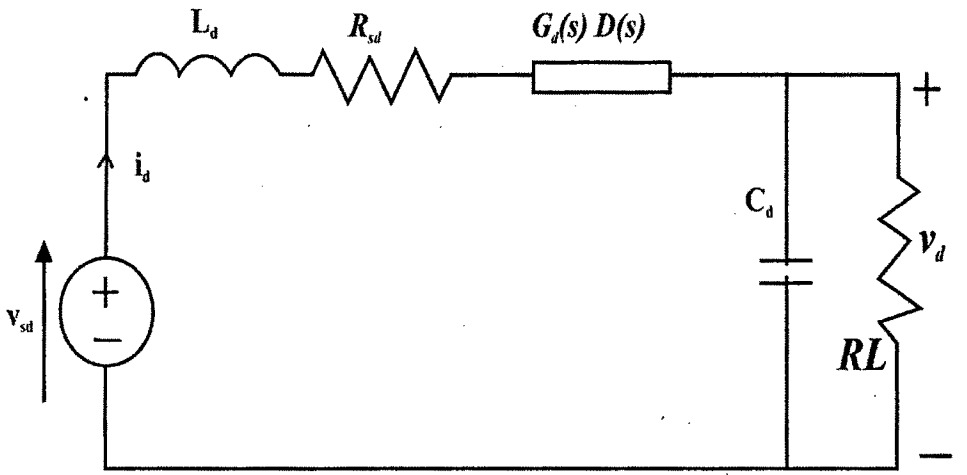


Fig 4.3 Simplified Equivalent Circuit of System

Analysis [1] tells us that either increasing the active filter gain or decreasing the cutoff frequency of low-pass filters in the harmonic detector results in a slow response, and causes a large and long transient dc voltage.

In addition, it has been shown [1] that the common-dc-bus system has a slower response time to a step change in the dc load than the separated-dc-bus system, whereas a larger overvoltage occurs in the separated system. The common system does not require any additional large dc capacitor for the active filter and is more economical and practical than the separated system.

4.1.3 Stability Analysis

.The stability of the active filter based on feedback control is discussed theoretically [25], taking into account delay time in the control circuit. As a result, it is revealed that the delay time may produce a bad effect on stability, especially when the power conversion system is installed on a stiff power system with low system inductance. [24] presents a viable way of reducing the effect of delay time on the system stability. Analysis in the frequency domain enables us to know-how much the system stability is improved in terms of gain and phase margins. A switching-ripple filter is designed to obtain good filtering performance without affecting the system stability. Experimental results obtained from a 20-kW laboratory system [52] verify the validity of the developed theory, and confirm the viability and effectiveness of the proposed control circuit.

Harmonic current-free rectifiers capable of operating at unity power factor are required as utility interfaces for inverter-based industrial loads such as adjustable-speed motor drives and uninterruptible power supplies in a range of 1–10 MW. Recently, pulse-width-modulated (PWM) rectifiers consisting of the same power circuit topology as PWM inverters have shown promise

in meeting the guidelines for harmonic mitigation [26-29]. The increased cost and switching loss caused by PWM, however, would make a high-power PWM rectifier rated at 1–10 MW economically impractical. The reason is that GTO thyristors or IGBTs used for the PWM rectifier are subject to high-frequency switching of the full amount of active power. In [25] ac/dc power conversion system is presented for providing a solution to the above-mentioned problems hidden in PWM rectifiers [30].

A small-rated series active filter for the purpose of achieving harmonic compensation [31-32] is integrated with a large-rated double-series diode rectifier for the propose of performing ac/dc power conversion. The active filter enables the diode rectifier to draw three-phase sinusoidal currents from the utility. In addition, the active filter based on supply current detection is characterized by closed-loop control with a relatively high feedback gain.

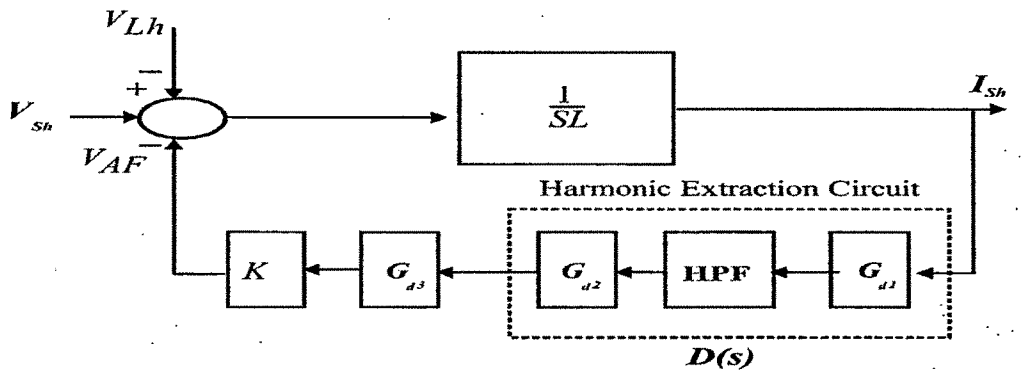


Fig 4.4 Control System Diagram: first-generation Circuit

The stability of the ac/dc power conversion system characterized by integration of a series APF with a double-series diode rectifier is studied taking into account delay time in the harmonic current-extracting circuit Fig 4.4. The analysis points out that even a delay time as short as 40 μs may make the active filter unstable when the ac/dc power conversion system is installed on a "stiff" power system.

The major time delay is caused by coordinate transformation in the harmonic current-extracting circuit. A configuration of the harmonic extraction circuit capable of eliminating the effect of delay time on the system stability is presented which reduces the phase delay in the extracted harmonic current even when the proposed configuration has the same delay time in the coordinate transformation as a conventional configuration does. The effect of the filter on the system stability is also discussed. Experimental waveforms obtained from a 20-kW laboratory system show stable operation even though the coordinate transformation circuit has a delay time of 40 μs.

4.2 APF Analysis using Quad Series VS-PWM CONVERTERS

The modeling, analysis, and design of an active power filter using quad-series voltage source pulse width modulated (PWM) converters [32] are presented using instantaneous space vectors of voltage and current. A vector differential equation derived in this paper makes it easy

to achieve the analysis and design of the active power filter. Experimental waveforms obtained from a prototype active power filler of rating 7 kVA, along with simulation waveforms, are included to verify the theory presented in [32].

Over the last five to ten years, a remarkable progress of fast switching devices such as power transistors and static induction thyristors has generated interest in the study of active power filters for harmonic compensation [33-37].

In addition to sophisticated pulse width modulated (PWM) control technology, the development of the theoretical study has made it possible to put them into a practical testing stage. Nowadays, an active power filter using voltage source PWM converters is considered as a new harmonic compensator in the coming generation. It is far superior in the compensation performance to a conventional passive **LC** filter, because a distinct difference exists in the compensation principle between the two.

Fig.4.5 depicts the basic compensation system configuration of the active power filter which is controlled in a closed loop manner to actively shape the source current $\mathbf{i_s}$ into the sinusoid. That is, it injects the compensating current **ic** into the source to cancel the harmonics contained in the load current i_L. Accordingly, any finite amount of impedance in the power system, which is usually predominantly inductive, does not influence the compensation characteristics.

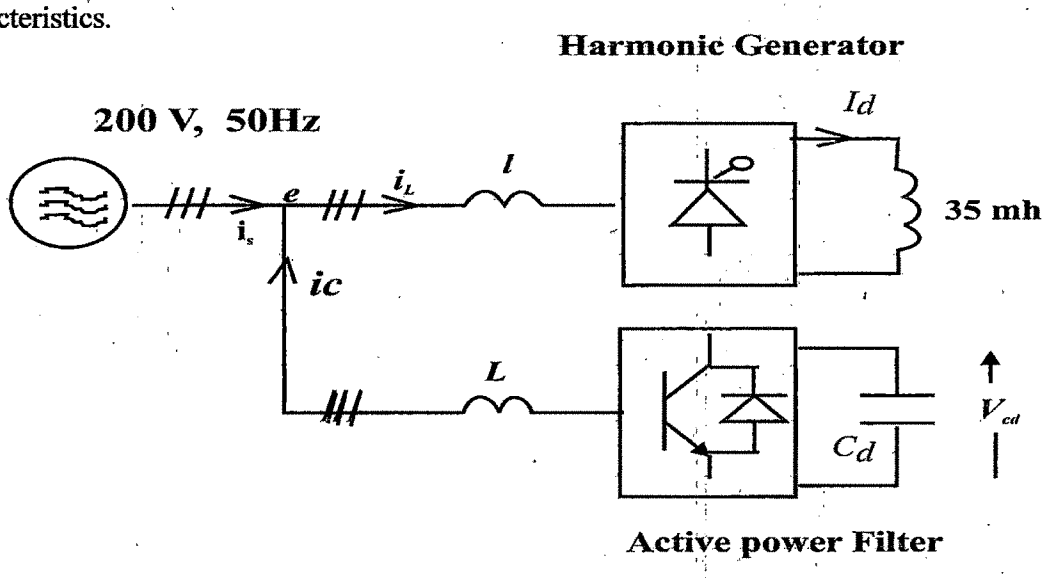


Fig 4.5 Basic Compensation System

The analysis of a voltage source PWM inverter for ac motor drives has been shown in many papers. When it is used as an active power filter, it is quite same in the power circuit as the active power filter. It is, however, different in the behavior because the active power filter acts as a non-sinusoidal current source. Therefore, the analysis and design of such an inverter are not available in the literature. In [32] model of the active power filter is developed for the analysis leading to the design. It is shown that one can find a satisfactory design, based on an interesting graph which relates the performance to various design parameters.

4.2.1 System Configuration

Fig. 4.6 shows the detailed system configuration of an active power filter using quad series voltage source PWM converters of rating 7 kVA.

The power circuit consists of four three-phase transformers for quad series connection, four three-phase voltage source PWM converters using 24 power transistors and a dc capacitor C_d . The primary windings of the transformers are connected to each other in series. Each transformer has a winding ratio of 1:2. The primary voltage is 50 V and the secondary 100V, because the line-to-line voltage of the source is 200 V (= 50 V x 4). The reason for adopting the quad-series voltage source PWM converters as the power circuit is to suppress the harmonics caused by switching operation without increasing the switching frequency, paying attention to practical applications. The voltage rating of the power transistors used here is 450 V and the current rating 25 A [37].

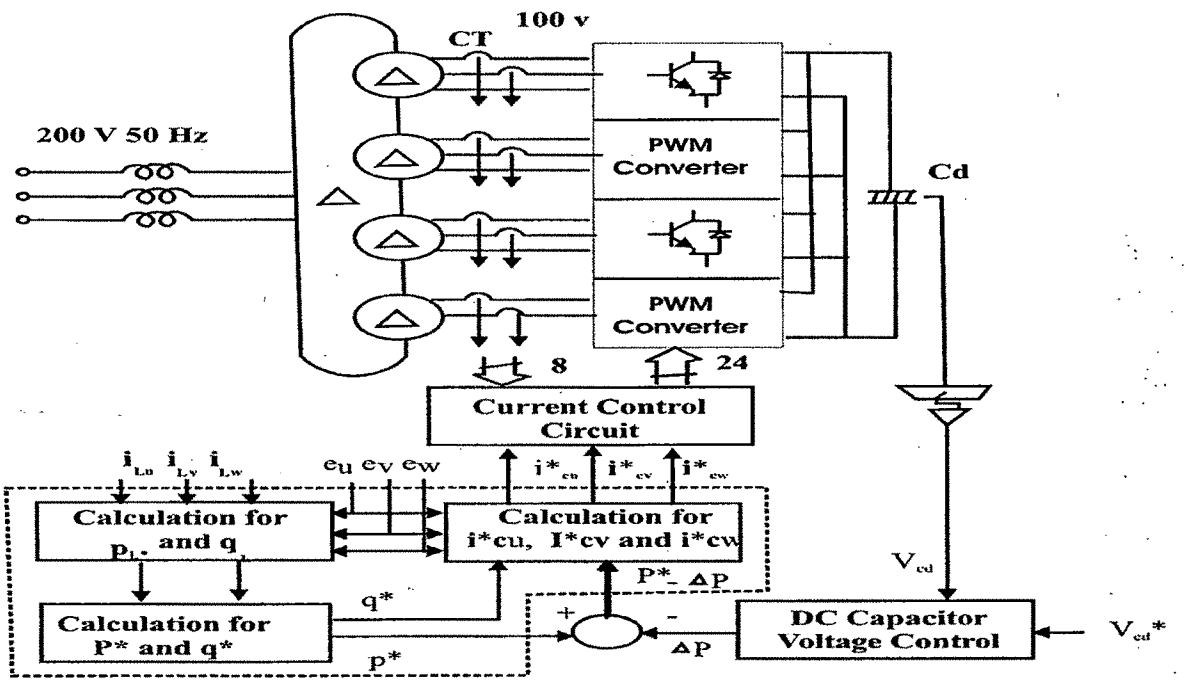


Fig 4.6 APF: System Configuration

As shown in Fig. 4.6 the control circuit consists of the calculation for the harmonic current within the dashed line, the dc capacitor voltage control, and the current control for the quad-series voltage source **PWM** converters. The calculation circuit for the harmonic current is divided into three calculation circuits. In the calculation circuit for p_L and $\mathbf{q}_L$, the three-phase voltages and the three-phase load currents are transformed into the **p-** q orthogonal coordinates. Fig. 4.7 shows the eight discrete voltage vectors $V(k)$ and a voltage vector e_o

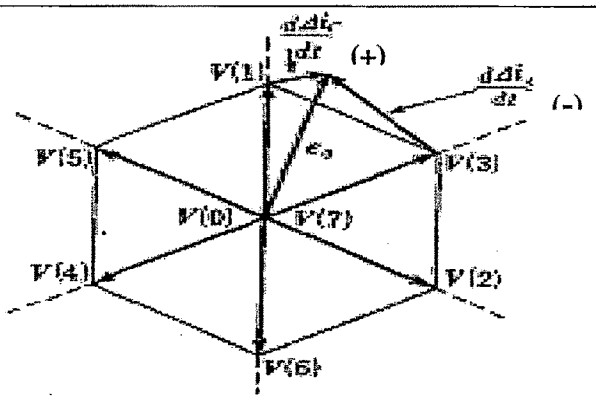


Fig 4.7 Voltage Vector Diagram

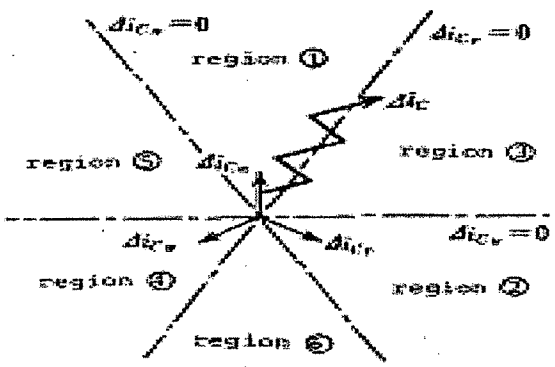


Fig 4.8 Current Vector Diagram

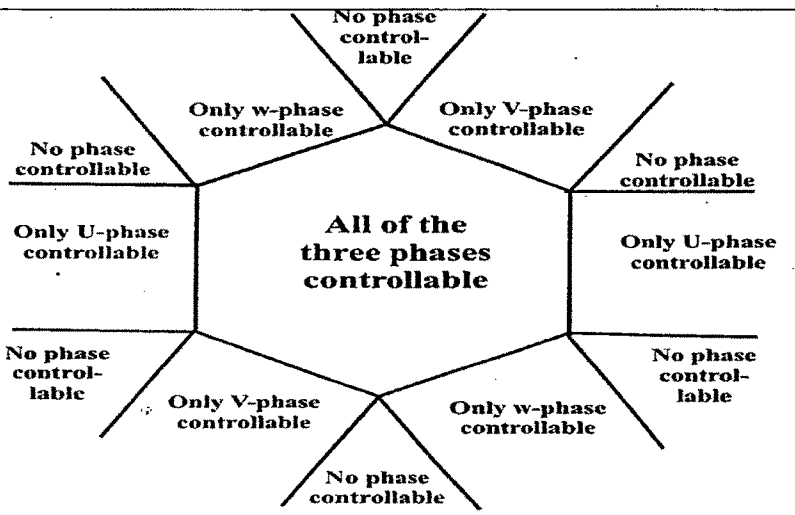


Fig.4.9. Summary of Analysis: Current controllable region

Fig. 4.8 shows the trajectory of Ai,. The active power filter selects such a voltage vector $V(k)$ among the eight that Ai, becomes a minimal vector on the basis of the polarity of the error current in each phase which is detected every a sampling interval of time [30]. Fig. 4.9 shows the summary of the analysis. An interval of time when e_o exists outside the hexagon corresponds to a commutation.

4.2.2 Design of Active Power Filter

Since harmonic compensation is the goal of an active power filter using quad-series voltage source **PWM** converter, it is important to achieve an optimal design of various parameters which influence the compensation performance, as well as to discuss the calculation circuit for i_{cu}^*, i_{cv}^*, i_{cw}^*, . In this section, a vector differential equation was derived, which relates the current controllability to various design parameters for an arbitrary compensating current system.

The optimal design of the active power filter depends on the order, amplitude and phase of the harmonic current for which it would compensate. Let the compensation objective be the harmonic current generated by the three-phase thyristor bridge converter of rating 20 kVA. In designing the active power filter, the following requirements are assumed:

I. The maximum voltage of the dc capacitor is 250 V, which is limited by the voltage rating of the power transistors used here.
II. The maximum value of the average switching frequency is 3.5 kHz, from the viewpoint of losses,
III. The commutation inductance of the thyristor bridge converter, **L** is 1.3 mH.

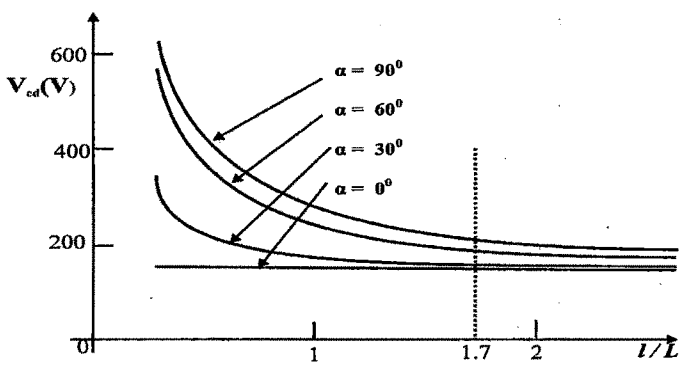


Fig 4.10 Theoretical Optimal Voltage of DC Capacitor

Fig. 4.10 shows the theoretical optimal voltage of the dc capacitor versus I/L in the case that the control angle α varies from 0^0 to 90^0. The definition of the optimal voltage is such a minimum voltage that ***eo*** always exists inside the hexagon formed by V ***(k).***

4.3 PASSIVE EMI Filter

This section deals with integrating a small-sized passive electromagnetic interference (EMI) filter with a voltage-source pulse-width modulated (PWM) inverter. The purpose of the

filter is to eliminate both high-frequency common-mode and normal-mode voltages from the three-phase output voltages of the inverter. A laboratory system consisting of a 5-kVA inverter, a 3.7-kW induction motor, and a specially-designed passive EMI filter was constructed [38] to verify the viability and effectiveness of the filter. As a result, both line-to-line and line-to-neutral output voltages look purely sinusoidal as if the inverter were an ideal three-phase variable-voltage, variable-frequency power supply when viewed from the motor terminals. This result in a complete solution to serious EMI issues related to high-frequency common-mode and normal-mode voltages produced by the PWM inverter.

Remarkable progress of power semiconductor devises has enabled an increase in the carrier frequency of a voltage-source pulse-width modulated (PWM) inverter using insulated gate bipolar transistors (IGBTs) rated at 600 V or 1,200 V to 10 kHz.. This significantly contributes to improved controllability of voltage, current, and torque. It also helps in reduction of acoustic noise. However, high-speed switching of IGBTs increases high-frequency leakage currents, bearing currents, and shaft voltage. Researchers and engineers in the area of power electronics and ac motor drives recognize it as electromagnetic interference (EMI) issues [44].

Presently, passive filters are employed at the output of voltage-source PWM inverters to deal with EMI related issues. Various types of filter configuration, based on inductors and capacitors, or diodes, have been proposed in [40-49]. Although a "clamping filter" in [27] is effective in suppressing the high voltage gradient at its motor terminals when a cable feeder between an inverter and motor is very long, it has little capability of mitigating the so called "shaft voltage." So far, no literature has been published on either a design procedure of a passive EMI filter consisting of both common-mode and normal-mode filters, or its installation effect on three-phase line-to-neutral and line-to-line voltages. Other solutions based on combination of passive components and active devices such as complimentary transistors have been described in [50-51]. Ogasawara, *et al.* has proposed a circuit consisting mainly of complimentary transistors and a common-mode transformer for achieving active cancellation of common-mode voltage [50]. This solution effectively eliminates the line-to-neutral common-mode voltage and shaft voltage. Takahashi, *et al.*, developed an active EMI filter that bypasses the zero-sequence current from the ground wire to reduce the ground leakage current [24] The active circuits of [50-51] have limitations because complimentary transistors rated at 600 V or higher are presently not available in the market.

[38] Focuses on integration of a small-sized specially designed passive EMI filter with a voltage-source PWM inverter operated at a carrier or switching frequency as high as 15 kHz. The motivation of this research is based on the well-known fact that the higher the carrier or switching frequency, the smaller and the more effective the EMI filter. The integration of the EMI filter makes both line-to-neutral and line-to-line voltages sinusoidal as if the inverters were an ideal variable-voltage, variable- frequency power supply when viewed from the motor terminals. Hence, it is possible to solve all of the EMI issues caused by high-frequency common-mode and normal-mode voltages. Experimental results obtained from a 5-kVA laboratory system confirm the viability and effectiveness of the specially-designed passive EMI filter.

4.4 Design Optimization of a resonant turn-off Snubber

An active resonant turn-off snubber suited for high-power IGBT converters is presented. The main feature of the snubber is that the maximum current rating of the auxiliary switching devices is small compared with that of the main switches. The basic operation of the snubber is described. This is followed by a detailed analysis of the losses in the circuit, which gives rise to an optimum snubber design procedure. An experimental version of the snubber is evaluated on an IGBT phase arm, and detailed measurements of the efficiency of the converter are taken [52] . The experimental results are in close agreement with the theoretical predictions.

Snubber circuits and soft-switching techniques are applied to power electronic switches to reduce switching losses and limit EMI. Through reduction of switching losses, higher switching frequencies can be obtained that result in higher bandwidth, improved dynamics and smaller filter components. A number of soft-switching topologies can be applied to IGBT-based converters. However, most of these topologies introduce special control requirements or high peak voltage or current ratings on the main switches.

One of the key considerations when designing the turn-off snubber is to obtain the optimum balance between the reduction in turn-off losses in the main IGBTs and the losses in the snubber circuit itself. In this Section, the different loss mechanisms are studied, including the losses in the resonant inductor, auxiliary switch and other snubber components. A number of studies on the switching behavior of IGBTs under soft-switched conditions can be found in the relevant literature [53-55]. [52] introduces an active resonant turn-off snubber for which the peak current rating of the auxiliary switches is significantly smaller than that of the main switches. Even though the snubber does not provide the full benefit of a combined turn-on and turn-off snubber, the benefits of the snubber are significant compared with the cost of the snubber components.

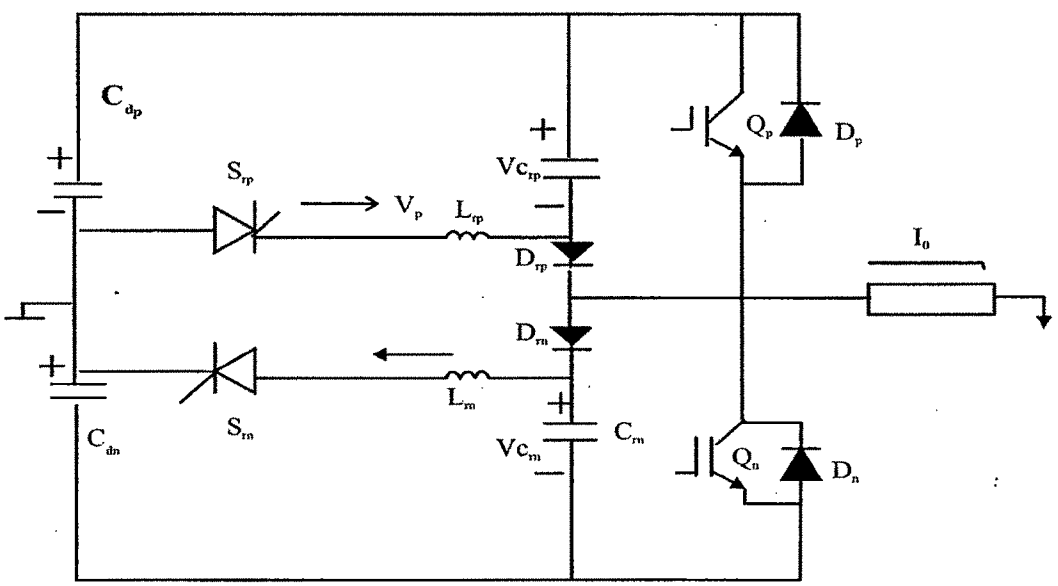


Fig 4.11 Resonant turn-off Snubber Topology

Fig. 4.11 shows the resonant turn-off snubber topology. IGBTs Q_p, and Q_n, along with freewheeling diodes Δp, and Δn, form a standard IGBT phase-arm. Capacitors *Cdp* and *Cdn* form the DC-link capacitor bank, with the centre point taken as the ground reference. The resonant snubber consists of capacitors C_{rP} and C_{rn}, diodes D_{rp}, and D_{rn}, inductors L_{rp}, and L_{rn}, and auxiliary switches S_{rp} and S_{rn}. Components C_{rp}, D_{rp}, L_{rp} and S_{rp} form the turn-off snubber for Q_p and S_{rp} is only triggered during periods of negative load currents

A number of papers on the optimum design of passive and active snubbers can be found in the literature [56-58].In contrast with the approach followed here, most of these papers do not consider the effect of the parasitic components in detail.

Some decisions have to be made about the operation of the converter and the ratings of some of the snubber components before the optimum design procedure is undertaken. These are the converter switching frequency f_s, maximum duty cycle d_{max}, blanking time t_b have to be selected based on the maximum time available for the capacitor discharge cycle t1(max). The approach followed in [52] is to find those values of C_r and L_r that are optimum in the sense that they result in the fewest total converter losses. The strategy is to calculate the total turn-off losses over one fundamental cycle of the output current for a range of different values of C_r and L_r. Those values of L_r and C_r that result in the fewest losses over one cycle of the output current are selected as the optimum values. The first step is to choose the range of values of C_r and L_r over which the optimisation process will be performed Secondly, for each value of C_r and L_r, the main IGBT turn-off losses and the losses in the auxiliary circuit are calculated over one cycle of the fundamental output current waveform, based on the loss equations [52]. If the voltage rise time of the snubber capacitor t_{vr}, exceeds the blanking the t_b, operation of the discharge circuit is ceased, the data sheet values of turn-off losses in the main IGBT may be used.

4.5 Controlling Reactive Power Compensation in APF

Shunt active power filters (APFs) can be used to compensate both harmonics and reactive powers from nonlinear loads. However, due to the limitation of the APF output current, the harmonics cannot be compensated successfully if the required compensating current is higher than a certain level. To overcome this problem, the section depicts an adaptive algorithm for controlling reactive power generated by the APF [59]. This control algorithm will permit the APF to fully compensate both harmonic and reactive currents if the total compensation demand is within the APF capacity. When a high level of compensation current is required, the reactive power generation will be reduced to save the APF capacity for the harmonic compensation task. The implementation of the adaptive algorithm with different types of APF controller is also discussed. Performances of APFs with and without the adaptive algorithm are simulated.

The problem of power quality is gaining more concern due to the widespread use of power-electronic based loads. It is because these nonlinear loads may seriously pollute power lines with their high level of harmonic currents and poor power factor. Shunt active power filters (APFs) have been considered as an effective solution for this problem as they can compensate simultaneously these harmonics and reactive power.

On the other hand, the APF is practically realized as a current regulator using voltage-source converter [60] or current-source converter [61-64] whose maximum output current is limited at a certain level. When being used for compensating both harmonics and reactive power from nonlinear loads, the APF output current can be distorted if the required compensation current is higher than the converter limit. Consequently, the harmonics in the power lines cannot be compensated successfully.

This problem can be overcome if the APF is used to treat the harmonics only. In this case, however, the APF capacity is not of full use. An adaptive controller for reactive power compensation can offer a better solution for this issue. With this control algorithm, both reactive- and harmonic- currents are fully compensated if the total compensation demand is within the APF capacity. When the required compensation current is higher than the output limit of the APF, the reactive power generation will be reduced to a suitable level to save the APF capacity for compensating harmonics. With this adaptive control principle, the APF output current can be prevented from distortion due to over limit of the APF converter, whilst the system power factor is kept at a highest available level.

The implementation of the adaptive algorithm with two conventional types of APF controller is discussed [59] . Using a DSP-based controller, the proposed algorithm can be simply implemented by modifying the control software for conventional APF controllers and no extra hardware is required. Performances of the APF systems with- and without the adaptive algorithm are simulated and compared [59]

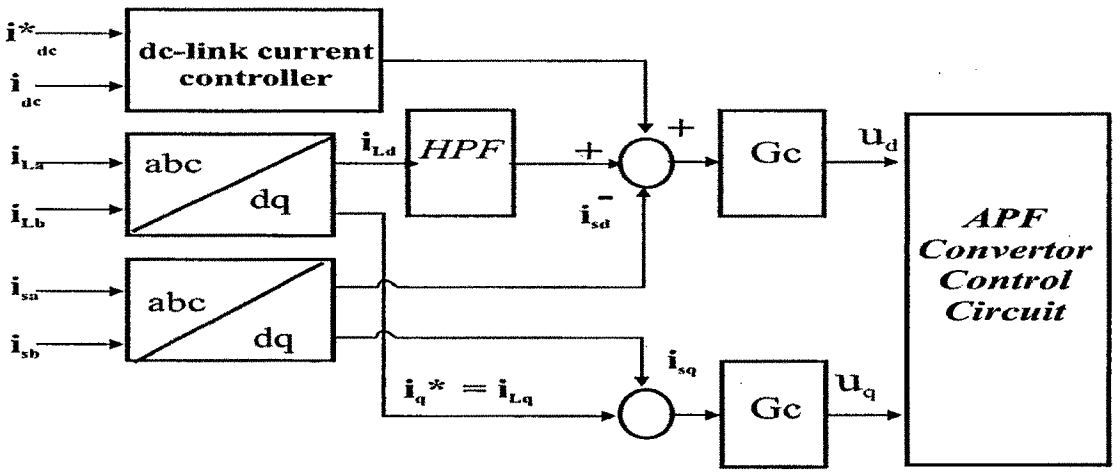
4.5.1 PRINCIPLE OF THE ADAPTIVE ALGORITHM

On the basis of circuit topology, APFs can be broadly classified into voltage-source APF (VS-APF) and current source APF (CS-APF). The APF investigated in this section is of CS type. However, in the literature review, the controller structure for both APF types can be considered similar. Further, it will be seen later that the control algorithm is designed as an additional block to the conventional APF controller and it does not affect to the design as well as the dynamic of the existing control loop. Therefore, the proposed algorithm could also be applied for APFs of voltage-source type.

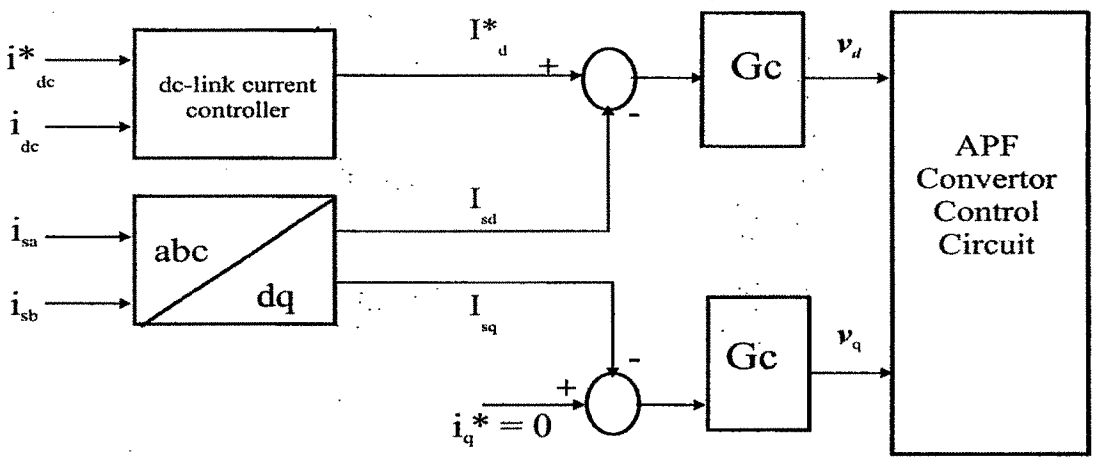
The commonly used structure of APF controller [60-64] consists of two cascade control loops: (i) the outer loop to regulate the dc-link voltage (for VS-APF) or dc-link current (for CS-APF), (ii) the inner loop to control the generation of compensation current.

The controller can be built in a stationary frame or in a rotating d-q frame synchronized with supply voltage vector. In this paper, the latter frame is used as it can maintain good performance for the APF output when the supply voltage is unbalanced [65].

On the basis of feedback signal type to detect harmonics, the APF controller configurations can be different. In general, the feedback signal can be: (i) load current [60-62]; (ii) line current [63-64]. APF controllers in according to these feedback types are termed as the controller type 1 and type 2, respectively.



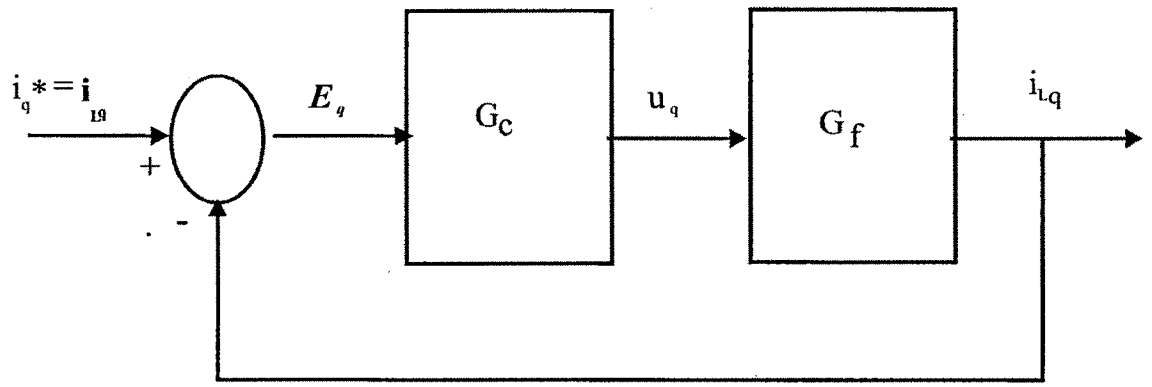
(a): APF controller type 1(using load current feedback)



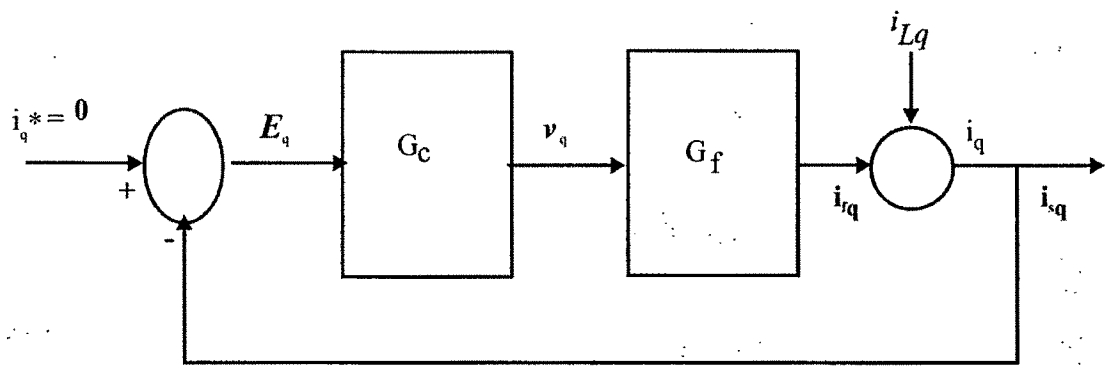
(b): APF Controller type 2 (using source current feedback)

Fig 4.12 Conventional VS-APF

Fig.4.12 show the structure of two controller types for a CSAPF. In both types of controllers, it should be noted that the d-axis loop controls the APF currents used to compensate the losses of the APF converter and the d-component of harmonics. The q-axis loop is to control the APF current which compensates the reactive power and the q-component of harmonics from the loads. Therefore, the control of APF reactive current generation can be achieved by acting on the qaxis loop only.



(a): APF controller type 1



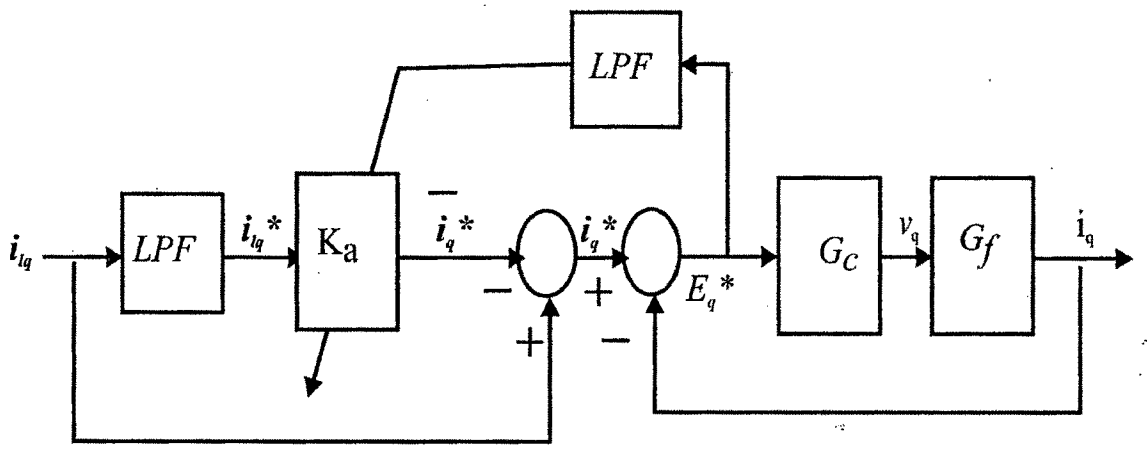
(b): APF controller type 2

Fig 4.13 Equivalent Block Diagram of q-axis loop Conventional VS-APF

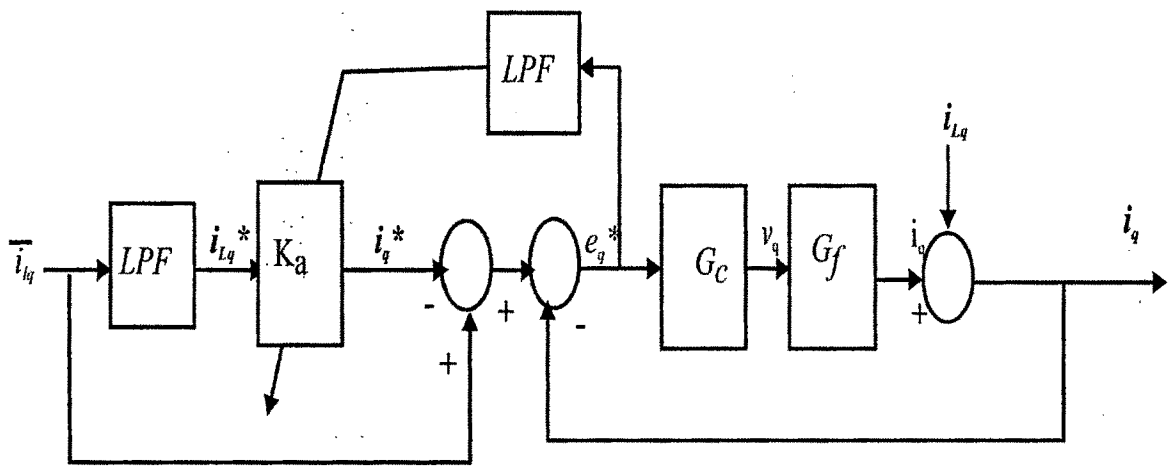
Fig.4.13 shows the equivalent block diagram of the q-axis loop of two conventional APF controllers. In this figure, *ifq* is the qcomponent of APF output current. For fully compensating both harmonic- and reactive currents from the load, the q-command signal i*q is set to be *iLq* (the q-component of load current) in the controller type 1 (Fig. 4.14a), or to be zero in the controller type 2 (Fig. 4.14b). Further, the converter transfer function G_f is of the same form for both types APF controllers whilst the q-loop compensator G_c could be selected differently in two types of controllers. The derivation of G_f as well as the selection of G_c for these conventional types of CS-APF controllers is thoroughly discussed in [62] and [63].

It should be noted that if the APF cannot compensate successfully both reactive power and harmonics due to its output current limit, the line current will be distorted. In this case, a dc-level exists in the q-error signal eq of both controller types. It varies accordingly with the distortion level in the line current. The principle of the proposed adaptive algorithm is to adjust the dc-level i_q^* in the q-command signal so that the reactive power generated by the APF will be adjusted to a suitable level to keep the distortion of line current within a certain range.

Fig.4.14 shows the block diagram of the proposed adaptive algorithm implemented with APF controller type 1 and type 2



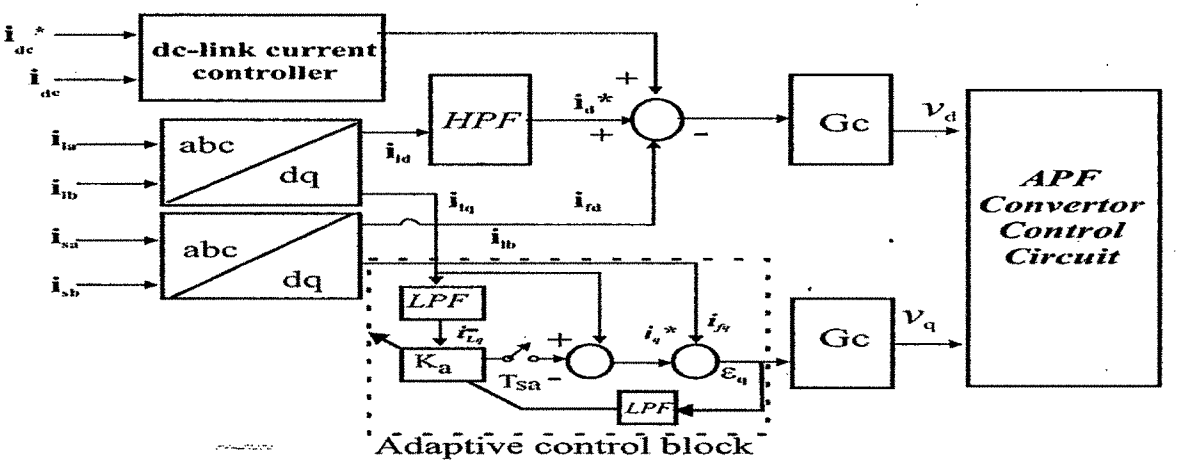
(a): APF controller type 1



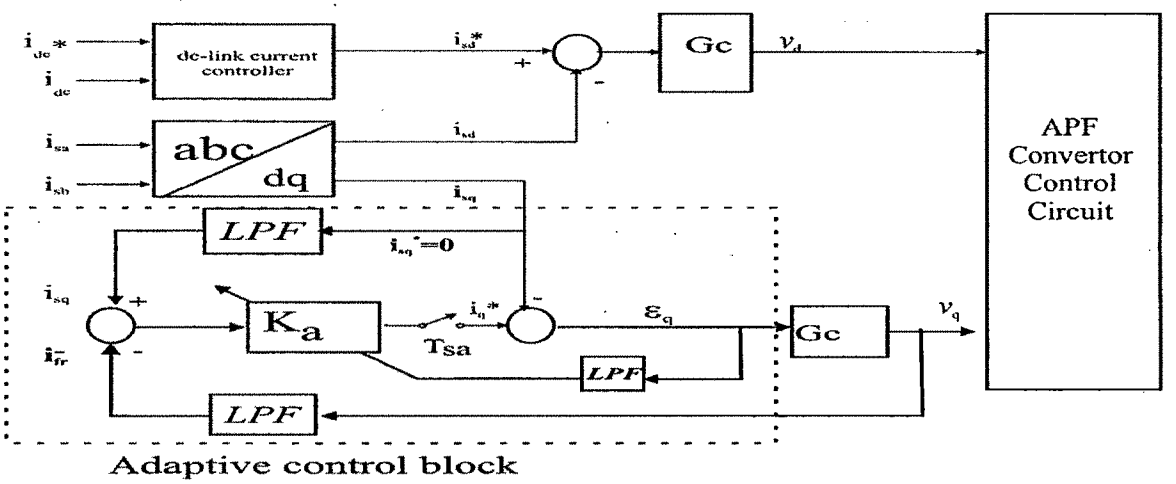
(b): APF controller type 2

Fig 4.14: Block Diagram of Adaptive Algorithm Implemented on VS-APF

Fig 4.15 depicts implementation schematics. With this algorithm, the reactive power generated by the APF is controlled by adjusting the reactive component of load current iLq with the adaptive gain Ka. Ka =1, means the reactive power from the load is not compensated at all, while Ka =0, means this reactive power is fully compensated. Thus, Ka must be limit in the range:1 $0 < K < 1$. The adaptive gain Ka is adjusted in every sampling interval Tsa.



(a): Adaptive Algorithm Implementation: APF controller type 1



(b). Adaptive Algorithm Implementation: APF Controller type 2

Fig 4.15: Schematic Diagram of Adaptive Algorithm Implementation

4.6 Advanced Control Strategies

The section describes the advanced control strategies for control of shunt APF.

4.6.1 Sliding Fast Fourier Transformation (SFFT)

By construction, an active filter is similar to a PWM unity power factor rectifier, but different to it by the fact that the inverter for APF applications present a forth IGBT leg or a centre tap on the main filtering capacitor battery which is connected to the neutral [66]. Shunt Active Filter [67-68] calculates in real time the harmonics in the load current which are applied as references to the inverter in order to cancel them and to guarantee a sinusoidal form for the supply current as shown in the Fig 4.16. There are different solutions for controlling the shunt APF [69-73] . The direct method is to analyze FFT the load current, by a sliding technique.

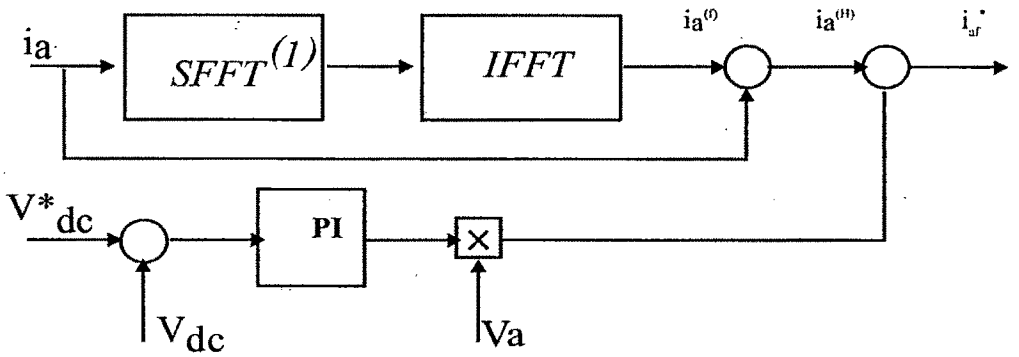


Fig.4.16 Calculation of the APF current reference

The first harmonic of the current is reconstructed (IFFT) and by subtracting it from the load current the harmonic of the load current is obtained. Beside these harmonic currents the inverter has also to produce a voltage across the filter capacitor in the buster mode. Although theoretically the APF dose not consume active power, in practice, due to internal inverter losses a certain input power is necessary. Consequently beside the harmonic current reference it is necessary to be added a current in phase with the particular voltage and of a magnitude proportional with the output of the voltage regulator.

SFFT solution requires a high amount of mathematical calculation. For this reasons the commercial available APFs use two DSPs, one dedicated to SFFT and a second one for the current control. [73].

4.6.2 p-q-n method

The technique called p-q theory was developed by Akagi et al. [74] starting by the classical change of coordinates from a b c to α, ß, 0 for the three phase voltages and currents. For sinusoidal voltage references only first harmonic currents are producing non zero average active and reactive power. Consequently, by some simple calculations one can determine the fundamental of the load currents and respectively their harmonics [76-77].

4.6.3 d-q Control:

Disadvantage of p-q theory is the fact that the references are a combination of 5th, 7th, 11th, 13th and so on odd harmonics and the regulators are PI type, unsuitable for this type of input. [73] Presented a solution based on a new d-q transformation in a new frame system in which both the references and the corresponding feedback to have an important d.c. content.

To verify the simulated results, a 5 KHz IGBT APF controlled by a Motorola 56F803 developing board (40 MIPS DSP controller has an 8 input analog 12 bits ADC converter with an acquisition time per channel 1.2 μs and 6 PWM output port channels) The tests were made using on a diode rectifier / capacitance-resistance load. The results were presented integer 10 in which all the electrical variables are in Q15 format and the time in number of samples. All these values were recorded by the microcontroller in the process in the RAM memory and they were downloaded after the experiment through the serial port. All the electrical variables were unfiltered in order to study also the influence of noise and spikes on the regulator response.