Appendix C: List of Papers

Presented/Published in Proceedings of Conferences/Seminars

1. **Khodidas Ghinaiya and Hina Chandwani**

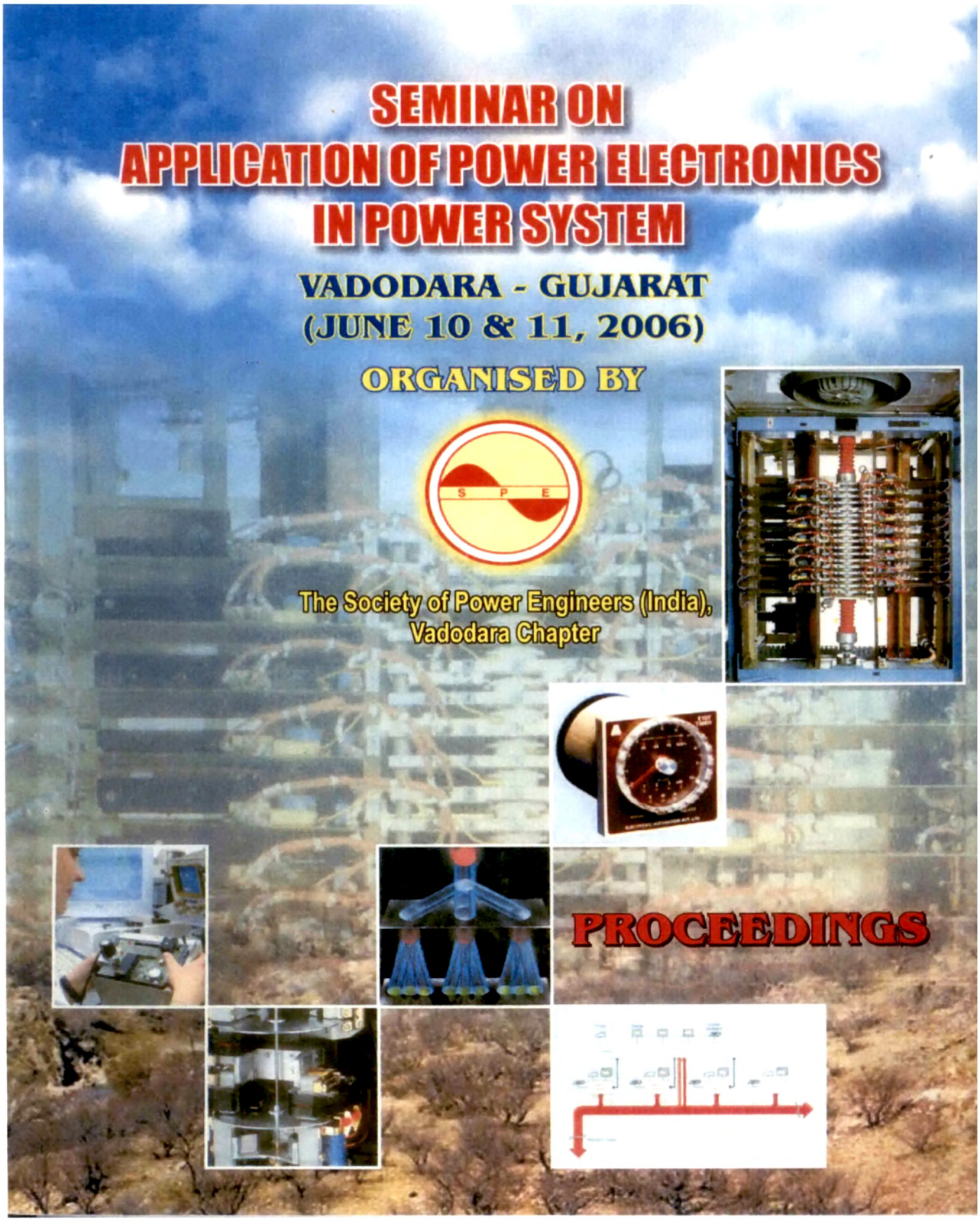
   "Single Phase PWM rectifier for Power factor correction "Proceedings of seminaron

   - Application of Power Electronics in Power system" Organized by The Society of Power Engineers (I) Vadodara Chapter at E R D A , Makarpura, Vadodara (June 10 & 11,2006) pp 68-74

2. **M M Ranade, N A Patel, V R kanetkar , H B Chandwani**

   "Higher reliability & Energy saving by addressing requirements of IGBT gate driver and coordination with power converter protection."

   - Proceedings of seminaron Appliaction of Power Electronics in Power system" Organized by The Society of Power Engineers (I) Vadodara Chapter at E R D A , Makarpura, Vadodara (June 10 & 11,2006) pp116-126 3


SEMINAR ON
APPLICATION OF POWER ELECTRONICS
IN POWER SYSTEM
VADODARA - GUJARAT
(JUNE 10 & 11, 2006)
ORGANISED BY
S P E
The Society of Power Engineers (India),
Vadodara Chapter
PROCEEDINGS

Appendix C: List of Papers

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1. *To conduct seminars, workshops & short term courses*
2. *To give platform to manufacturers for technical presentation of their products.*
3. *To arrange study tours.*
4. *To provide guidance to Engineering students.*
5. *To distribute the priced publication of CBIP. NEW Delhi*
6. *To Promote research work and rewarding the same*
7. *To maintain bio-data of Expert members.*
8. *To render helping hand to utilities in crisis / Disaster / (Earth quake, flood, cyclone etc.)*
9. *To progagate Energy conservation techniques.*
10. *Publication of news magazines.*
11. *To offer guidance to individual in day to day Engineering problems.*
12. *Library*

SINGLE PHASE PWM RECTIFIER FOR POWER FACTOR CORRECTION

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Abstract

The Potential of PWM self commutated voltage source converters in the area of AC to DC power conversion has been well established. These converters offer unity power factor operation while delivering near sinusoidal current and reduced input/output filter size. Two mostly used current controlled strategies employed to control the power flow in a PWM rectifier are indirect current control (ICC) and hysteresis current control (HCC). HCC technique is studied here for its simplicity and also due to its suitability in low to medium power applications. This paper presents hysteresis current control (HCC) in detail. The study and performance evaluation are made using MATLAB–SIMULINK (Sim Power System).

Introduction

Line commutated thyristor converters have been widely used for the AC/DC for a number of years though they have serious disadvantages like
(i) Non-sinusoidal currents, rich in lower order harmonics, drawn from the supply lines,
(ii) Poor operational power factor, especially, at large firing angles, and
(iii) Low frequency harmonics or ripple in the output dc voltage.

The PWM converter designs with forced commutated thyristor converters could overcome these disadvantages. However, owing to the bulkiness, losses in the commutation circuitry and complexity of control the forced commutated thyristor converters could not be used effectively. With the introduction of self commutated devices like power transistors, MOSFET's and GTO's, the PWM converter designs got simplified considerably. As such, there is a distinct possibility that the PWM self commutated converters will replace the classical line commutated converters in the near future.

The PWM self commutated converters have two categories, viz., voltage source converters (VSCs) and current source converters (CSCs). Both have the primary advantages of delivering near sinusoidal input currents at unity power factor and 0-360 °
power angle range.

In this report discussion is restricted to VSCs, the recent past has shown considerable amount of work being published. The switching devices, such as power transistors or MOSFETs, used by the VSCs have low current ratings but higher switching frequency ratings as compared to GTOs. Thus they can serve low to medium power applications while the GTOs are more suitable in high power applications.

Basic configuration.

The basic configuration used by single phase bi-directional VSC's are shown in fig.1.1 along with operating mode in fig 1.2. The switching devices S_1 to S_4 in fig.1.1 generate a voltage Van between the terminals 'a' and 'n'. Typical Van voltage patterns are shown in fig 1.3 for converter. Van is three level waveform for full bridge i.e [0 $+V_{DC}$, 0 $-V_{DC}$].

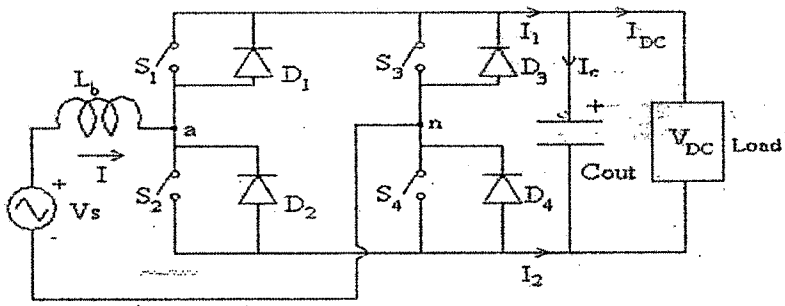
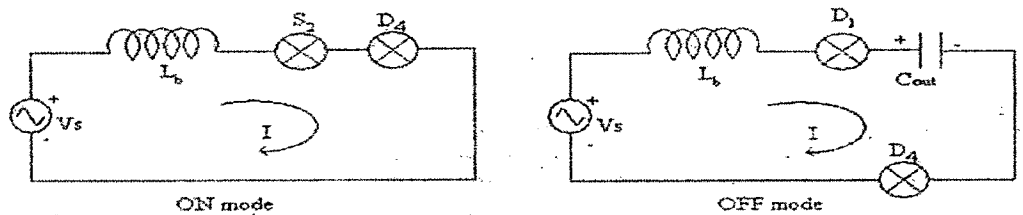


Fig 1.1 Basic configuration



(POWERING)

Fig 1.2 Operating mode.

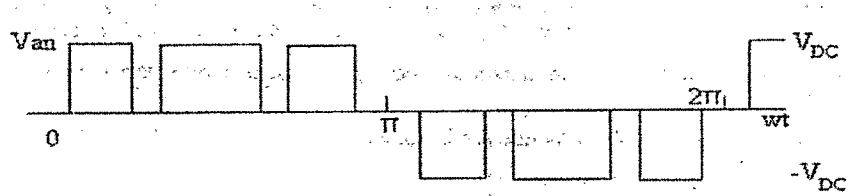


Fig 1.3

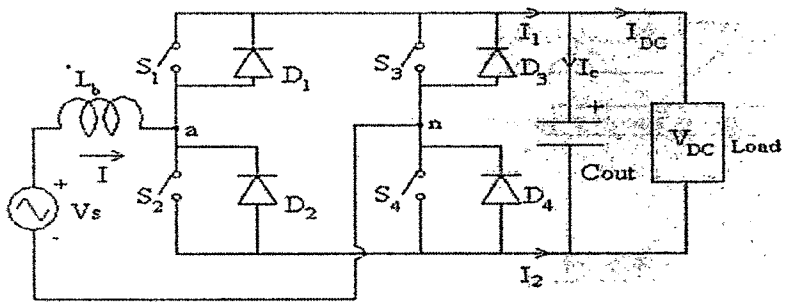


Fig 1.1 Basic configuration

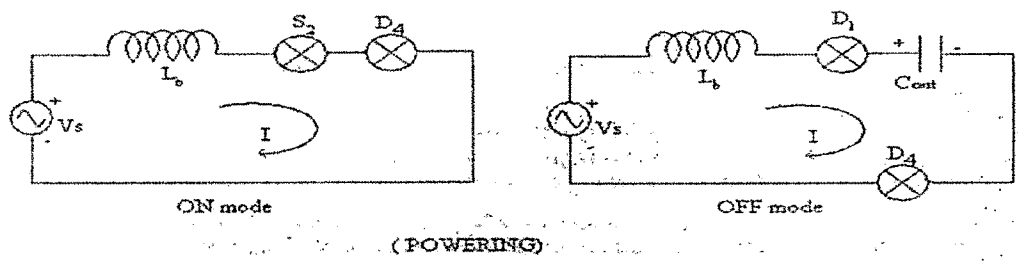


Fig 1.2 Operating mode.

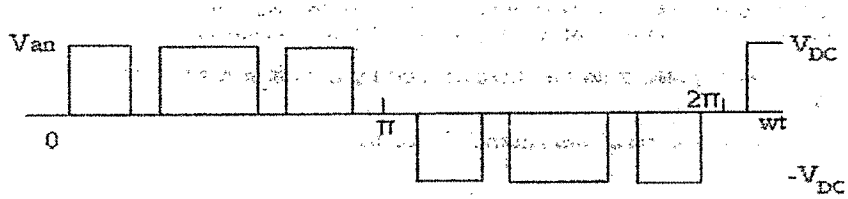


Fig 1.3

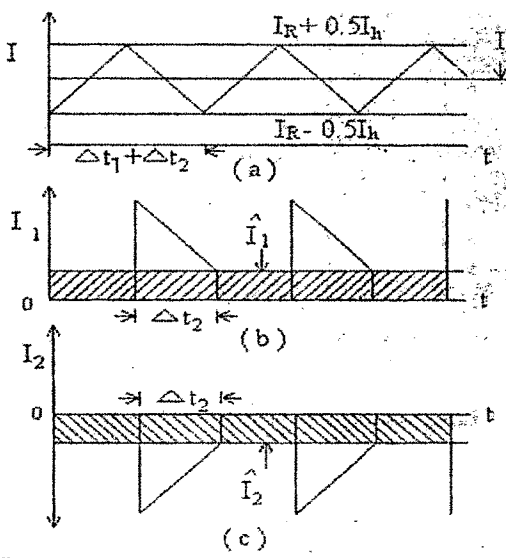


Fig 1.4
(a) Typical Input Current waveform in one switching cycle.
(b) Instantaneous current, and local average at upper dc link.
(c) Instantaneous current, and local average at lower dc link.

In order to understand the design aspect of VSCs, it is necessary to evaluate DC link current in converters. These are evaluate based on "Local average" criterion suggested in [1].

Analysis method of local average for Full-bridge

DC link currents

Consider fig. 1.2 corresponding to the on and off mode operation (powering) of S_2, a typical switching waveform of the input current 'I' is shown in fig 1.4. The current is considered to be controlled in a current window ΔI_h using HCC technique. The reference current is $I_R = I_m \sin(wt + \phi)$. The current rises in the on time Δt_1 to reach the upper limit of the window, while falls in the off time Δt_2 to reach the lower limit of the window. It is assumed that $\Delta t_1+\Delta t_2$ is so brief that I_R is substantially constant.

It is proposed here that each pulse train be characterized by a local average, the time span of the average being $\Delta t_1+\Delta t_2$.

From fig 1.4a the local average of the on time current $\hat{I}_{on}$ defined as,

$$\hat{I}_{on} = \hat{I}_1 = \frac{\int_0^{\Delta t_2} I dt}{\Delta t_1 + \Delta t_2} \approx \frac{I_R \cdot \Delta t_2}{\Delta t_1 + \Delta t_2}$$

while the instantaneous value of I_1 is

$I_1 = 0$ in the time span Δt_1

$I_1 = I$ in the time span Δt_2

Likewise, a local average for $\hat{I}_2$ ($\hat{I}$ off) and it is evaluated as,

$$\hat{I}_{off} = \hat{I}_2 = \frac{-I_R \cdot \Delta t_2}{\Delta t_1 + \Delta t_2}$$

The "Local averages" are illustrated in Figs. 1.4b and 1.4c for full bridge configuration.

Switching times

During the positive cycle of Input supply (V_S), in fig 1.2 when switch S_2 is on,

$$\Delta t_1 = \frac{L_b \cdot \Delta I_h}{V_S}$$

When S_2 is OFF,

$$\Delta t_2 = \frac{L_b \cdot \Delta I_h}{V_{DC} - V_S}$$

Thus,

$$\hat{I}_1 = -\hat{I}_2 = \frac{I_R \cdot V_S}{V_{DC}}$$

When switching rates are very fast, one can make $\Delta I_h \rightarrow 0$, $(\Delta t_1 + \Delta t_2) \rightarrow 0$, and $I \rightarrow I_R$. In this ideal situation, one can treat the local averages $\hat{I}_1$ and $\hat{I}_2$ as the continuous time function.

Substituting,

$V_S = V_m \sin(wt)$

And $I_S = I_m \sin(wt+\phi)$

$$\hat{I}_1 = -\hat{I}_2 = \frac{V_m \cdot I_m \cdot (\cos\phi - \cos(2wt+\phi))}{2 \cdot V_{DC}}$$

Where ,
V_m = Peak of the input voltage 'V_S'
I_m = peak of the reference current I_R
ø = operating power factor angle selected
V_{DC} = output DC voltage

For the unity power factor operation i.e. for ø =0,

$$\hat{I}_1 = -\hat{I}_2 = \frac{V_m \cdot I_m \cdot (1 - \cos(2wt))}{2 \cdot V_{DC}}$$

For the full bridge VSC for unity power factor,

$$\text{Instantaneous input ac power} = V_S \cdot I_S = \frac{V_m \cdot I_m (1 - \cos(2wt))}{2 \cdot V_{DC}}$$

and

$$\text{Instantaneous output dc power} = V_{DC} \cdot \hat{I}_1 = \frac{V_m \cdot I_m (1 - \cos(2wt))}{2 \cdot V_{DC}}$$

Last two equation shows that the instantaneous ac and dc powers are equal.
Further,

Average input ac power = $\frac{V_m \cdot I_m}{2}$, and

Average output dc power = $V_{DC} \cdot I_{DC}$

Comparing last two equations,

$$I_{DC} = \frac{V_m \cdot I_m}{2 \cdot V_{DC}}$$

So for the full bridge VSC

$$\hat{I}_1 = -\hat{I}_2 = I_{DC} - \frac{V_m \cdot I_m \cdot \cos(2wt)}{2 \cdot V_{DC}}$$

The above equation shows that the DC link currents of the full bridge VSC have a second harmonic component riding on the average output direct current I_{DC}.

Control strategy.

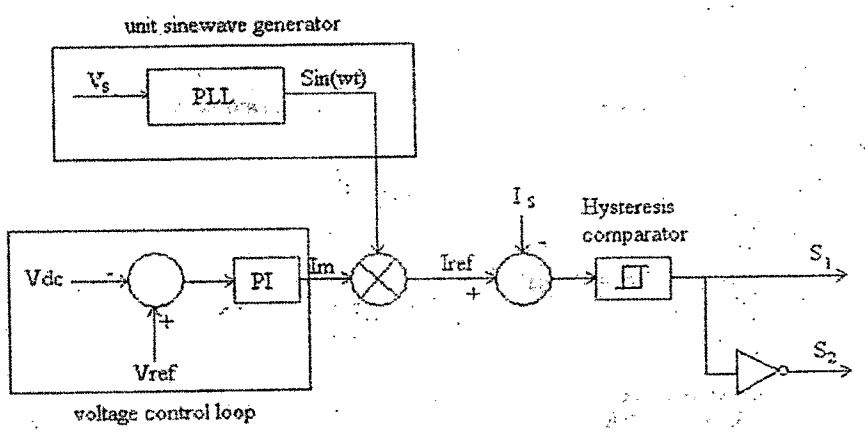


Fig 1.5 Block diagram of control strategy

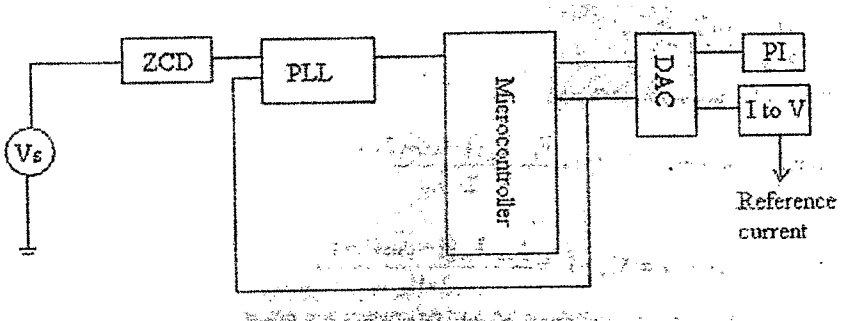


Fig 1.6 Control Block diagram of reference current generator

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As shown in fig 1.6 apart from the micro-controller all other part are implemented with analog and digital circuit. Micro-controller used here is of 8-bit and it serves two function i) it stores pattern of sine wave in it's program memory which is used to generate unit sine wave and ii) it provides initial startup control of converter along with different protection such as over voltage, over current etc.

Detail of prototype.

Devices used in the prototype are given below.

L = 2mH, 60Amp.

Cout = 3300μF/450VDC , two such capacitor are in parallel

IGBT used is BSM 150 GB 120D – 1200V/210A (Tc=25°C).

THYRISTOR used is IXYS MCC 56-16 io1B Itrms = 100A and Itavm = 63A.

Input Filter used to remove high frequency ripple in supply current ,

Ls = 500μH / 150A

and Cs = 15μF/370V @ 50/60Hz.

Converter performance is checked for resistive as well as Inverter Load.

Result of resistive load is given below.

→ Current sensor after LC filter.

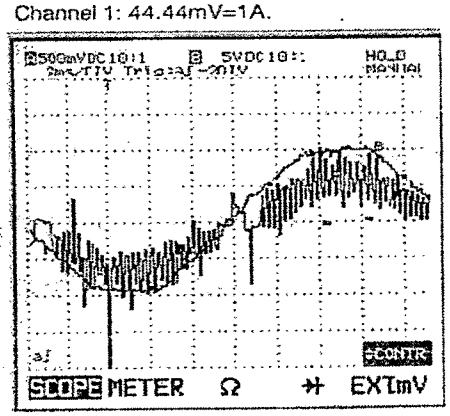
It is Hal-effect sensor with ratio of 90A/4V.

I.e. 1A represented by 44.44mV

Wave form of the result

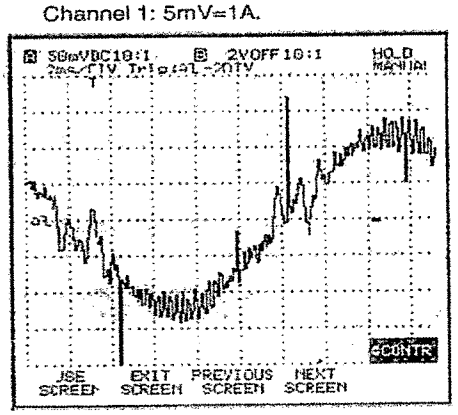
For 2.5kW resistive load

Channel 1: 44.44mV=1A.



a)

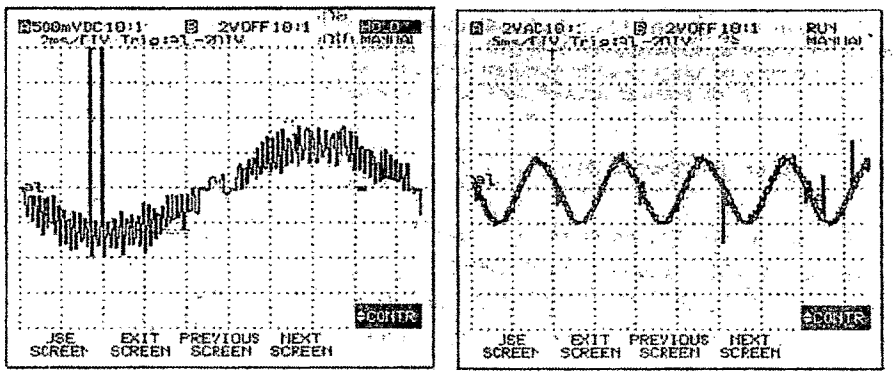
Channel 1: 5mV=1A.



b)

a) Input current and voltage on control side
b) Input current waveform

Channel 1: 44.44mV=1A.



a) b)

a) Input current full cycle in controlled condition.
b) DC link voltage ripple.

Conclusion.

This paper deals with use of present day self – commutated devices (particularly IGBT) for power converter applications. The converter topology and its control strategy is executed for Power Factor Correction for UPS application. The control system is realized with analog and digital approach. While the analog section is used for PI loop implementation and gating signal generation, 8-bit Microcontroller is used to store the sine wave pattern and to provide different protection.
Prototype developed gives a good result with constant DC link voltage and near unity power factor with near sinusoidal line current.

References.

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[2] J.W.Dixon and B.T.Ooi, " Indirect current control of a unity power factor sinusoidal current boost type three phase rectifier, " IEEE Trans. on Industrial Electronics, IE-35, no. 4, pp 508-515, Nov. 1988

[3] Mohan / Undeland / Robbin, " Power electronics, converters, applications and design", Third Edition, John Wiley & Sons, Inc.

[4] R. Itoh and K. Ishizaka , " Single phase sinusoidal converter using MOSFETs" IEE Proceedings, Vol. 136, pt. B, no.5, pp 237-242, Sept. 1989.

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HIGHER RELIABILITY & ENERGY SAVING BY ADDRESSING REQUIREMENTS OF IGBT GATE DRIVER AND COORDINATION WITH POWER CONVERTER PROTECTION

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Abstract

With increased use of four quadrant converters in various applications, the use of Insulated Gate Bi-polar Transistor (IGBT) has also increased rapidly. IGBT has become more popular because ease of turn-on and turn-off, low gate power, higher switching frequencies (15 kHz), good voltage capabilities (3300V), and current ratings (1800A). Though IGBT has better control characteristics compared to Thyristor or Gate Turn-off Thyristor (GTO), essentially it has poor I^2t rating. Thus the IGBT needs a very fast acting gate driver to sense voltage across its collector and emitter and turn-off the device if it is rising fast due to a short circuit condition / current flowing through it. If the gate driver cannot act within 8 to 12 microseconds, the IGBT is likely to get damaged.

The gate driver for IGBT hence is an important element in the design of power converters using IGBTs, operation and protection. The paper describes gate driver for 200A, 1400V Fuji make IGBT, responses of the driver for normal and short circuit conditions, the protection circuit implementation, and presents the experimental results for the responses. Similar results for 225 A, 1700V ABB make IGBT also are presented. The test conditions are maintained close to what the converters utilizing these IGBTs are likely to experience, as it is the only way to ensure that the gate driver and the protections will work correctly in reality when the converter operates in actual conditions.

The paper is intended to provide an insight in understanding the gate driver, its functions, correlation of the short circuit conditions with operation of the gate driver, and finally making the driver operate with necessary and realistic conditions, it can also be said that the properly designed gate drive electronics can optimally reduce the switching losses of IGBT and hence can contribute to energy saving .

I. Introduction

Solid-state ac to dc power conversion of electric power is widely used in adjustable speed drives, switch mode power supplies, uninterrupted power supplies, HVDC transmission, and traction.

The power converters make use of power stack assemblies of uncontrolled / controlled semiconductor devices. The controlled power devices could be Thyristor, Gate Turn-off Thyristor (GTO), power MOSFET, or Insulated Gate Bi-polar Transistor (IGBT), when we consider present scenario of commercial available devices. While thyristor is a force-commutated device, the other three are self-commutated devices. The gate drivers for these power devices form the integral and necessary part of entire converter design.

It is necessary to see that the gate drivers are properly designed to take care of normal as well as abnormal conditions, like short circuit conditions when large current is likely to flow through the device. Since the I^2t rating, especially for power MOSFET and IGBT are quite low as compared to thyristor or GTO, high-speed semi-conductor fuses cannot protect these devices. Thus gate driver has to turn-off the device within microseconds (8 to 12μs) and hence the design of the gate driver forms a very important aspect of the power converters using these devices. Having made a design for the gate driver, it is also essential to test it with the actual converter creating the necessary short circuit and observing the response of the gate driver. If the actual converter is not available, it is necessary to create short circuit conditions close to what converter might be facing in reality and then test the gate driver in such conditions [1].

used in power converters with 240V single-phase and 415V three-phase applications for reactive power compensation. While the single phase converter operates with 600V DC bus voltage and 1.5kHz switching frequency, the three phase converter operates with 850V DC bus voltage and 3kHz switching frequency. Gate driver design, actual short circuit phenomenon, and working of the protection are explained in detail and experimental results are presented with necessary explanation for proper performance of the driver and the IGBT.

II. Gate drive requirements for IGBT

Isolation

In general gate driver for all IGBTs in a converter must be isolated from earth, control electronics and from each other. Minimum recommended isolation is 2.5kV for one minute for 415V systems.

Gate resistance Rge

The lower the gate resistance the lower will be the turn-on and turn-off times. This will mean faster switching on and off of the switch and lower switching losses. But faster the turn off the higher will be turn off over voltage generated due to associated leakage and wiring inductances. Further, if the gate resistance is low, there will be a momentary high current pulse drawn by the IGBT gate.

It is hence essential to have two separate resistors, one for forward driving of the gate and one for reverse biasing it. The forward resistor needs to be low for the fast turn on. The reverse resistor should be of higher value than the forward resistor so as to reduce the unwarranted voltage overshoots.

Implication of gate emitter voltage and requirement of bipolar voltage

A positive gate voltage above the threshold value is required to turn on the device. The lower the gate- emitter voltage (Vge), the higher is the Vce (sat) (collector-emitter voltage) and the on state power dissipation. For lower Vge, the short circuit withstand probability is higher. A negative Vge is required to reduce the probability of unwanted turn-on of the device. This will also reduce the turn-off switching time, which will mean fast switching action and less switching power dissipation.

Over current protection

An IGBT can get subjected to over current situations. These conditions could be as below.

- IGBT may have to carry excessive current than rated because of the sudden increase in load current
- Simultaneous turn on of the two series devices in one arm of the converter resulting in short circuit of the dc bus and allowing the dc bus capacitors to discharge through them
- Insulation breakdown due to single or double earth fault

To terminate the over current rapidly, the turn-off must be very fast with due consideration for the over voltage issue. A separate sensing for earth fault is required to save the device.

Drive power calculations

Drive power is calculated as follows.

Drive power = $(1/T) \int [v^*i\ dt]$
To be integrated from 0 to T
Voltage ' v ' is different for turn on and turn off .
Drive power = $Fs[Vge^*Qch + (-Vge)^*Qch]$

Vge = The turn on gate emitter voltage
-Vge= The turn off gate emitter voltage
Fs = Switching frequency

Qch can be obtained for the given Vge i.e. for the given turn on gate-emitter voltage from the manufacturers data curves.

Blanking time

In case of converters, where two IGBTs are in series for one leg of the converter, it is necessary to provide some blanking time between the turn-off of one device and turn-on of other device to avoid a direct short circuit across the DC bus.

Circuit layout considerations

The length of the wires used while manufacturing of IGBT stack assembly (device modules, snubber circuits, dc capacitors, heatsink, blower in case of force cooling, temperature sensor, bus bars and insulation) dictates total dc loop leakage inductance. It is necessary that this inductance is minimum. Higher inductance increase overshoot in voltage across the device when it turns off.

III. Gate drive details for Fuji IGBT

The 200A, 1400V Fuji IGBT requires the gate driving voltage +15V/ -5V. Fuji IGBT module contains 2 IGBTs in one package. The block diagram in fig. 1 gives overall features of the gate drive card for the IGBT module. The gate drive card posses two channels for the two IGBTs. The control electronics supplying the pulses to the IGBT module uses following power supplies for the two gate drive channels.

- +12V
- -12V
- Signal ground (SG)
- 0 (zero ground)

Signal ground and zero ground are shorted externally and hence can be assumed same for all practical purposes.

IGBT is driven by an hybrid driver IC which produces the rated Vge at its outputs. Various different hybrid driver ICs are available, like EXB840, EXB841, EXB850, and EXB851 from the manufacturer. The selection of the hybrid IC is based upon the rated voltage, rated current, and the operating frequency of the IGBT to be driven. The hybrid driver IC selected for the Fuji device is EXB841.

Fig 2 shows the block diagram of a single channel of the gate drive (GD) card. Hybrid IC, EXB 841, uses an isolated supply of 20V. It converts the dc supply voltage at a required Vge level at its output (+15V for turn on and –5V for turn off). Each channel also consist of opto-coupler with high isolation voltage 2500V for one minute to isolate power side from electronic control circuit.

During normal operation, the PWM pulses are given at the control inputs of the respective channels. These are transferred to the hybrid IC through comparator stages, with each comparator stage contributing almost 0.5μs of delay. Hybrid IC itself contributes 0.5μs delay for pulse transmission. Thus, the overall delay between PWM pulse at the control input and the pulse appearing at the gate emitter terminals of the IGBT is approximately 3-4μs. Since this is for all the IGBT's of the three-phase converter, a certain degree of synchronization gets maintained amongst all the IGBT's. Figure 3 gives the pulse waveform.

Normally, blanking time of 10 to 12μs is sufficient to avoid direct short of IGBT's in same leg and is achieved by using an RC network, which delays the pulse for the incoming IGBT. Refer fig. 4 for this delay understanding.

A micro-controller controls the overall operating sequence and PWM pulse pattern for the IGBT's. The gate drive incorporates the function of protection against over current by sensing the over current in IGBT through the hybrid driver IC.

The over current condition can occur for very short. Thus it needs to be latched for some time for the micro-controller to sense it and execute a proper shut down procedure for the given converter. The latch circuit latches this signal (that symbolizes over current condition sensed) for few milliseconds giving sufficient time for the micro-controller to accept information and execute the shut down procedure, and then it is de-latched by a de-latching circuit.

A comparator stage has been configured in each channel which compares the voltage coming from the control input, the voltage produced by the Hybrid IC and opto-isolator when short circuit is sensed and voltage pulse from Latch-de-latch circuit and gives a 'HOLD' command for the gate drives. The

latter two pulses are zero during normal operation. Hence PWM pulses get transferred to the gate emitter as Vge .

IV. Operation of the gate driver during over current

Hybrid driver IC in gate drive incorporates over-current sensing and protection circuit. An over-current is detected according to the relationship between the drive signal and the collector voltage. Refer Fig. 5(a) and (b). Fig 5(a) shows a logical AND gating of the voltage sensed across collector-emitter and pulse delivered. When pulse is delivered and Vce voltage is high, trip command is generated, indicating the short circuit condition.

The instant when the pulse is delivered, Vce voltage falls to zero. A sudden high current begins to flow through the device when short circuit occurs and the voltage Vce starts increasing as shown in Fig. 5(b). When this rising current reaches a value which corresponds to Vce is 7-8V, the AND gate logic of the hybrid IC operates and the trip command is generated at its pin no. 6. This is shown in Fig 6.

Pin 5 of the hybrid IC turns on the opto-isolator stage which provides a soft cut off signal to the comparator stage in gate drive card which stops the PWM pulses and hence the Vge signal to IGBT.

As shown in the block diagram fig. 2, the over current protection circuit gives a command to trip generation circuit which further sends a 'trip from gate drive' signal to a Latch-de-latch circuit.

The Latch-de-latch circuit latches the 'trip from gate drive' signal up to few milliseconds (approximately 16ms), thus giving a hardware inhibit for the IGBT pulses. This is sufficient time for the micro-controller to execute a proper shut down procedure and to stop the gate pulses to both the IGBTs of a leg.

V. Analysis for the total turn-off delay

The total propagation delay from the time the PWM pulse appears at the control input to the time when the gate pulse Vge gets withdrawn due to the short circuit sensing is attributed to propagation delays at various stages.

As shown in the fig. 7 the total delay is
$= \Delta t1 + \Delta t2 + \Delta t3 + \Delta t4 + \Delta t5 + \Delta t6$

where

$\Delta t1$= 1.5μs (from PWM at the control input connector CN2/10 (3 comparators) till the PWM pulse reaches at the base of the final driving stage transistor Q)
$\Delta t2$ = 0.5μs (forward delay of the hybrid IC)
$\Delta t3$ = 0.5μs (at the beginning of this instant current starts rising. This is the delay for Vce reaching zero and then rising to the sensing level)
$\Delta t4$ = 3μs (over current sensing and command delivery to the opto- isolator by the hybrid IC)
$\Delta t5$ = 2μs (delay in one Op amp buffer (0.5μs) and in 3 Op amp comparator stages of the Latch-de-latch circuit that gives the HOLD command)
$\Delta t6$= 5μs (delay for actual turn off (3μs +2μs))

Total delay = 12.5μs (should be considered as a guiding figure)

VI. Importance of short circuit testing

The IGBT converter is a 4 quadrant converter working with boost charged dc bus. The dc bus voltage has to be more than peak of the incoming supply voltage. In this case the dc bus operates at 850V. In the practical applications due to mal-operation of the control electronics or EMI effect, even if a sufficient blanking time is provided, the IGBTs may face unwarranted triggering resulting in large uncontrolled currents due to the stack capacitor discharging through them. Thus, the short circuit sensing logic and the trip logic have to operate within the short duration of few microseconds.

The IGBT device basically has to perform two operations satisfactorily. First, it has to switch at a operating frequency of the converter in which it is used at rated voltage and allowing the rated current to flow. The second function is its behavior under over current condition, when it has to turn off within short duration. In order to ensure proper working of the IGBT under these two conditions, the normal switching test for the device under given power conditions and short circuit test at given dc voltage (applied through charged capacitor bank) are essential to be performed on the converter itself. The normal frequency operation test helps in ascertaining the losses and temperature rise of the converter. The short circuit test helps in checking performance of the entire protection system employed. However, considering practical limitations, these tests can be performed separately as indicated here. Further, the normal frequency operation test is carried out at lower frequency of 250Hz, (just to check the PWM pulse transmission is okay), while the short circuit tests are carried out at full dc bus voltage and also to check IGBT performance under repetitive short circuit pulse application from practical point of view.

VII. Short circuit testing and experimental results

In the intended converter, the IGBT is operated at 600 / 850V dc and 1.5 / 3kHz operating frequency, based on single-phase or three-phase operation. As explained in section VI (Importance of short circuit test), the short circuit testing of this device at 850V dc as well as with switching of 3 kHz at 850V dc becomes essential.

The test set up consist of a single pulse generation circuit which generates a single pulse to be given at the control input of the gate drive card to turn the IGBT on for the pulse width duration. The power circuit has got a capacitor bank, which is charged by the input supply, and when the IGBT is turned on the entire energy stored in the capacitor bank is discharged through the IGBT. Refer fig.s 8 and 9 which give details of the power circuit / test set up used for the testing. One is for testing the IGBT up to 560V DC and the other one is for testing the IGBT up to 850V DC.

Initially it is tested for normal switching function. It is switched by giving a square wave of 250Hz at its control input with device current of 6-8A. The waveforms captured are of Vge and Vce, as given in fig. 10.

From the delay calculations in the section V, it is evident that the gate driver is designed to cut off the IGBT in 12 μs) for over current / short circuit condition. To ensure this proper operation of the gate drive card, the IGBT is short-circuited for various different time intervals around 12 μs mark. The intervals selected are as below.

- 5 μs (interval less than the calculated 12 μs duration of cut off)
- 13μs (interval nearest to 12μs mark
- 25μs (interval greater than 12μs)
- 40μs (interval far above the 12μs mark)

The short circuit testing is done step wise starting from 50V DC. Increasing the voltage, the short circuit testing is done at 100V and then at 200V DC for all those pulse widths given above. Once the confirmatory level of the gate drive is attained, the dc voltage is further increased at 400V, then at 560V and finally short circuit test is done at 850V dc for all the above pulse widths. The waveforms are given in fig. 9 for the voltages Vce, Vge, input pulse and device current.

The final test is a repetitive test at 850V, wherein the short circuit pulse of 25μs is given at every 1min. interval, to check how many such shots the IGBT is able to with stand.

The test results for the 200A, 1400V, Fuji make IGBT (2MBI200PB-140) are given in fig. 10and fig.11

Similar test results for the 225A, 1700V ABB make IGBT (5SNS 0225U170100) are given in fig. 12.

VIII. Some important aspects for design

It is essential to note certain points as summarized below.

- The gate driver must operate with less than 12 μs to stop the conduction of the IGBT completely.
- A criss-cross protection for the IGBTs in same leg should be given right at the point where the gate driver trip is available for any of the IGBTs. This ensures immediate turn-ff of both the IGBTs in the same leg.

- A Latched protection then can be given to ensure all the IGBTs turn-off following gate driver trip command for any of the IGBTs in the converter stack. The Latch-delatch time could be kept more than 5ms so that the main electronic regulator has enough time to react and apply the final stop conduction command.
- The turn-on and turn-off resistors define the respective time. However, the turn-off resistor needs to be higher than the turn-on resistor and its actual value will get defined by acceptable over shoot of the voltage seen by the device during the short circuit tests.
- The short circuit test needs to be conducted at rated dc bus voltage as seen by the converter in normal operation.

IX. Conclusion

The paper analyses the gate driver requirements for 200A, 1400V IGBT, details out the design requirements essential for the fast protection of the IGBT when it faces short circuit conditions at actual operating dc bus voltages of 600 / 850V DC, and explains as to how these requirements can be built in along with coordinated protections for a typical power converter. Short circuit test results are given for the 200A, 1400V and 225A, 1700V IGBT are in line with the desired performance of the gate drivers.

The paper also summarizes the complete protection requirements when the IGBT is a part of the power converter and hence will serve as a guide line for IGBT converter design engineers.

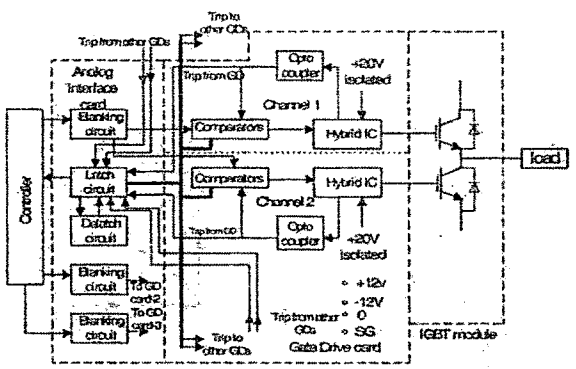
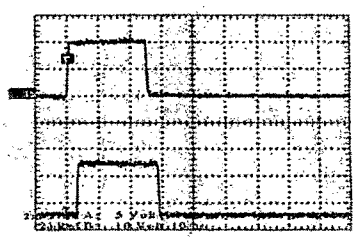
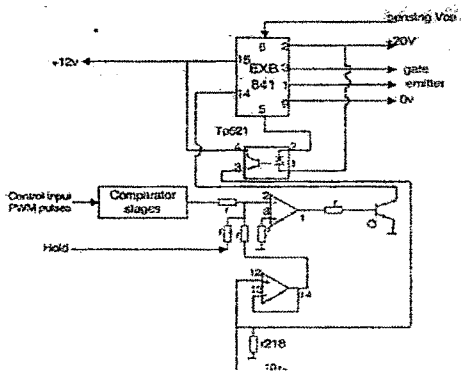


Fig. 1: Block diagram of the gate drive Card with 2-Channels



Ch1:-input pulse Ch2:-Vge

Fig. 3: Shows the delay between the input pulse and the Gate-Emitter Voltage



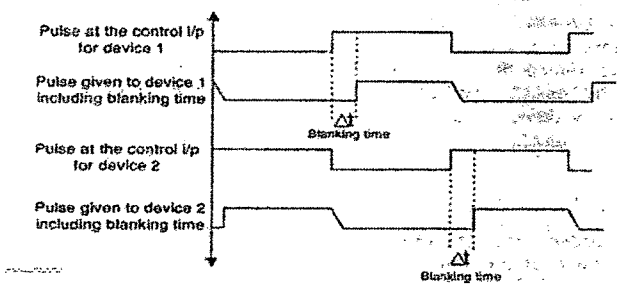
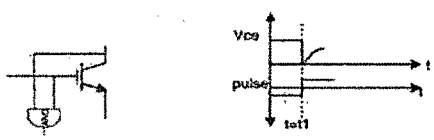


Fig 4: Blanking time

Fig 2: Block diagram of a single channel of gate drive card for Fuji IGBT



(a) (b)

Fig. 5 : (a) Logical AND relationship between the drive signal and collector voltage (b) Vce waveform when the short circuit pulse is applied at t = t1

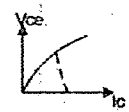


Fig 6: Relationship between Collector Current and Vce

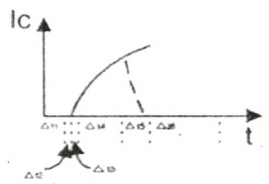


Fig 7 : The Total Delay breakdown

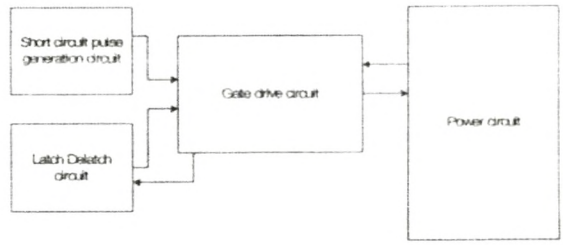
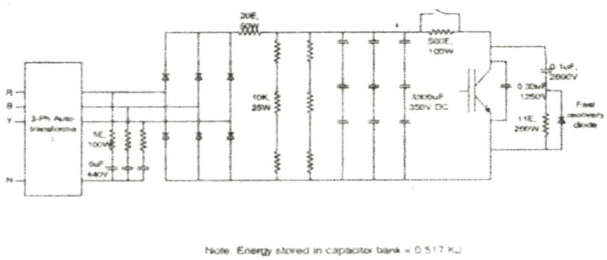
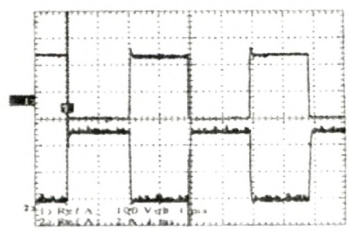


Fig. 8: Test Set-up block diagram



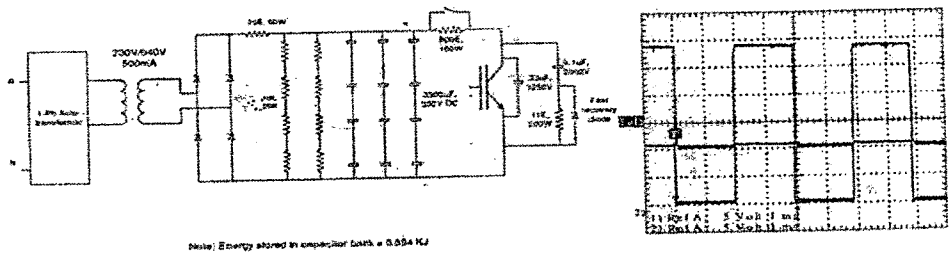
Note: Energy stored in capacitor bank = 0.517 KJ

(a) **Power circuit upto 560V**



Ch1:- Vce Ch2:- Device current

(a)



(b) Power circuit upto 850V

Fig.9 : Power circuit for testing

Ch1:- Vge Ch2:-input pulse

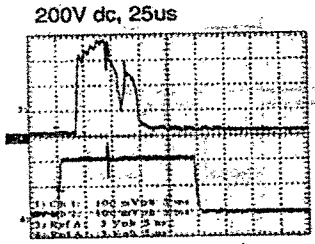
(b)

The load resistor connected in series is of 75 Ohm . The device current is 5A . Pulse train at the control input is of 250 Hz with 50% duty cycle. This makes charging time constant greater than 2 ms so the dc bus voltage drops to 250V.

Fig. 10 : Switching test of Fuji IGBT at 250Hz and 375V

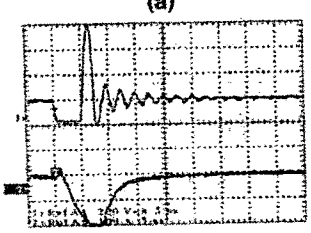
Short circuit test (Fuji IGBT)

200V dc, 25us



Ch1 : Vge Ch2: Input pulse

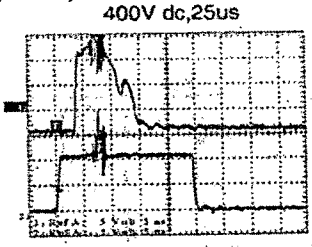
(a)



Ch1: Vce Ch2 Device current (inverted)

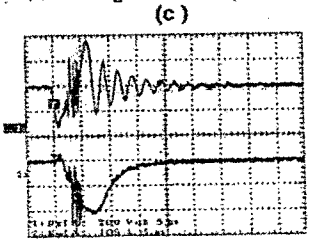
(b)

400V dc,25us



Ch1 : Vge Ch2: Input pulse

(c)



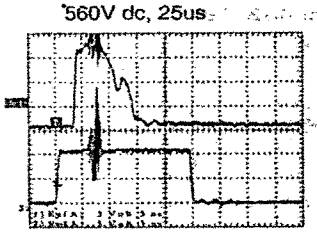
Ch1: Vce Ch2 Device current (inverted)

(d)

(a) and (b) : Device turns off in 12 microseconds. Vce overshoot 600V.
(c) and (d) : Device turns off in 12 microseconds. Vce overshoot 400V.

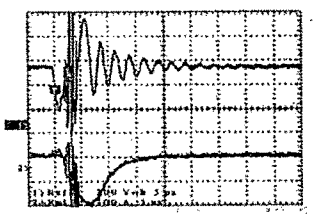
Appendix C: List of Papers

560V dc, 25us



Ch1 : Vge Ch2: Input pulse

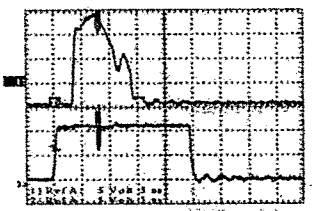
(e)



Ch1: Vce Ch2 Device current (inverted)

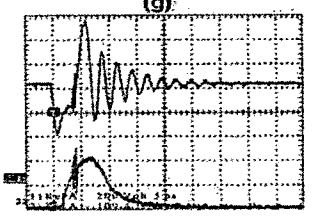
(f)

850V dc, 25us



Ch1 : Vge Ch2: Input pulse

(g)



Ch1: Vce Ch2: Device current (inverted)

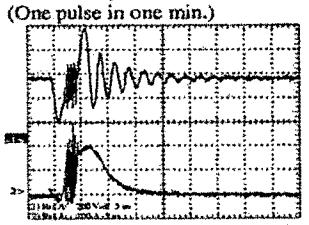
(h)

(e) and (f) : Device turns off in 12 microseconds. Vce overshoot 420V.
(g) and (h) : Device turns off in 12 microseconds. Vce overshoot 530

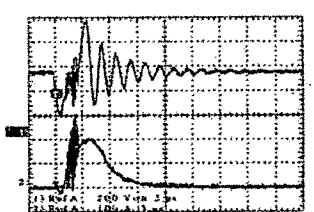
Fig. 11 : Short circuit and destructive test results for Fuji IGBT

Destructive test at 560V with 25us pulse and 50 such shots

(One pulse in one min.)

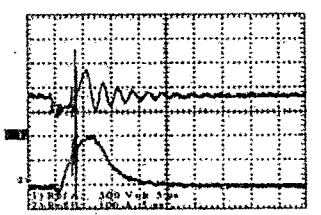


Vce and Ic waveform of 1st short ckt test **(i)**

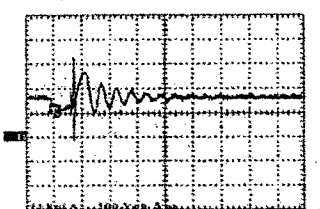


Vce and Ic waveform of 50th short ckt test **(j)**

Destructive test at 850V with 25us pulse and 50 such shots



Vce and Ic waveform of 1st short ckt test **(k)**

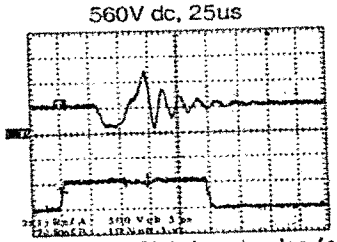


Vce waveform of 50th short ckt test **(l)**

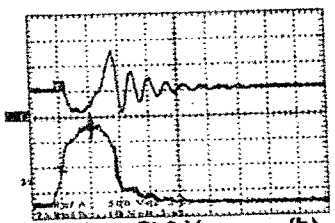
Note : All waveforms of No. 1 to 50 were same as above for 560V and 850V

Fig. 12 : Short circuit and destructive test results for ABB IGBT

560V dc, 25us

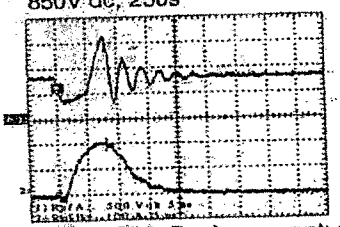


Ch1 : Vge Ch2: Input pulse **(a)**

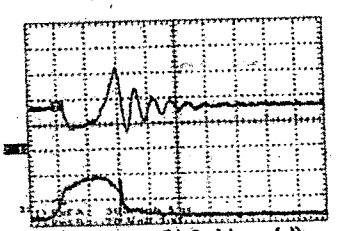


Ch1: Vce Ch2 Vge **(b)**

850V dc, 25us



Ch1 : Vce Ch2: Device current **(c)**



Ch1: Vce Ch2: Vge **(d)**

(a) and (b) : Device turns off in 12 microseconds.

(c) and (d) : Device turns off in 12 microseconds.