

Appendix D: Experimental Waveforms (Analog Controller)

D-1 Transformed Waveforms (Two Phase: 2ϕ)

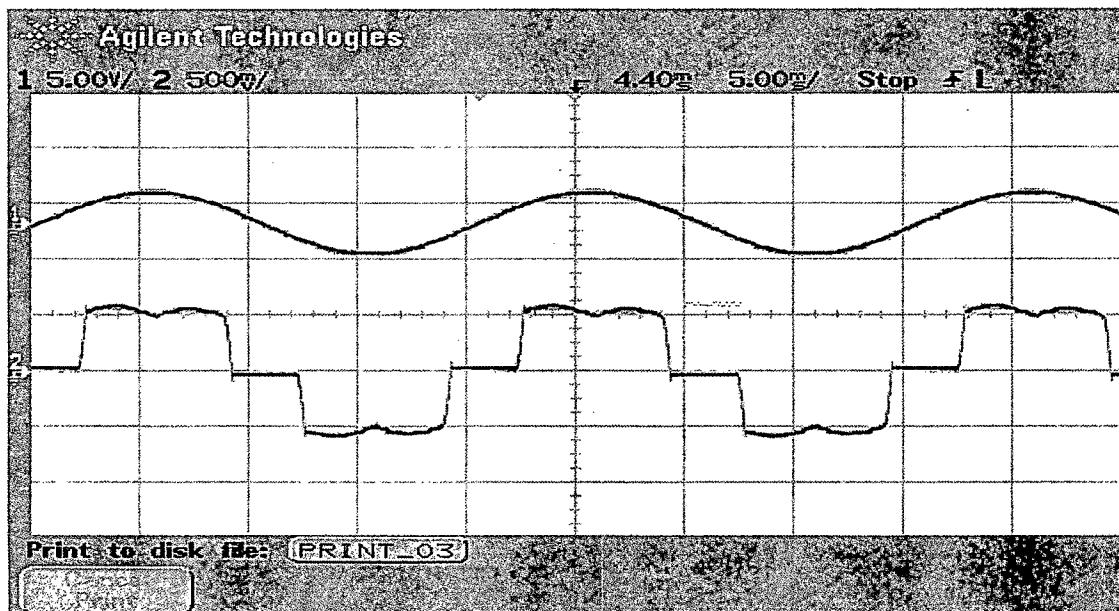


Fig D-1.1: v_α and i_α

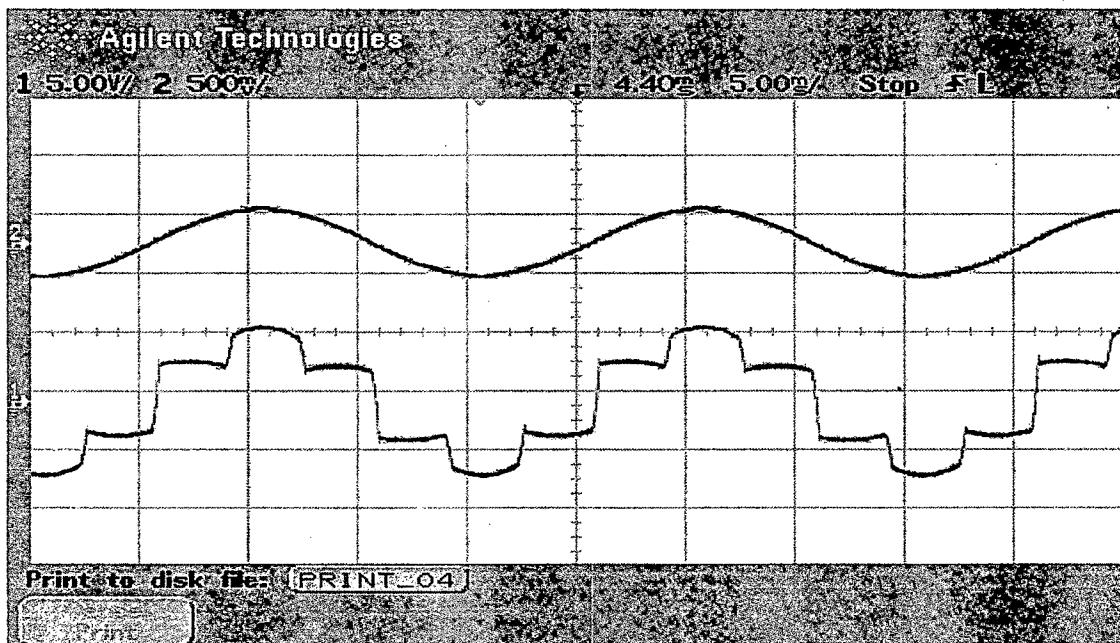


Fig D-1.2: v_β and i_β

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D_2 Power components

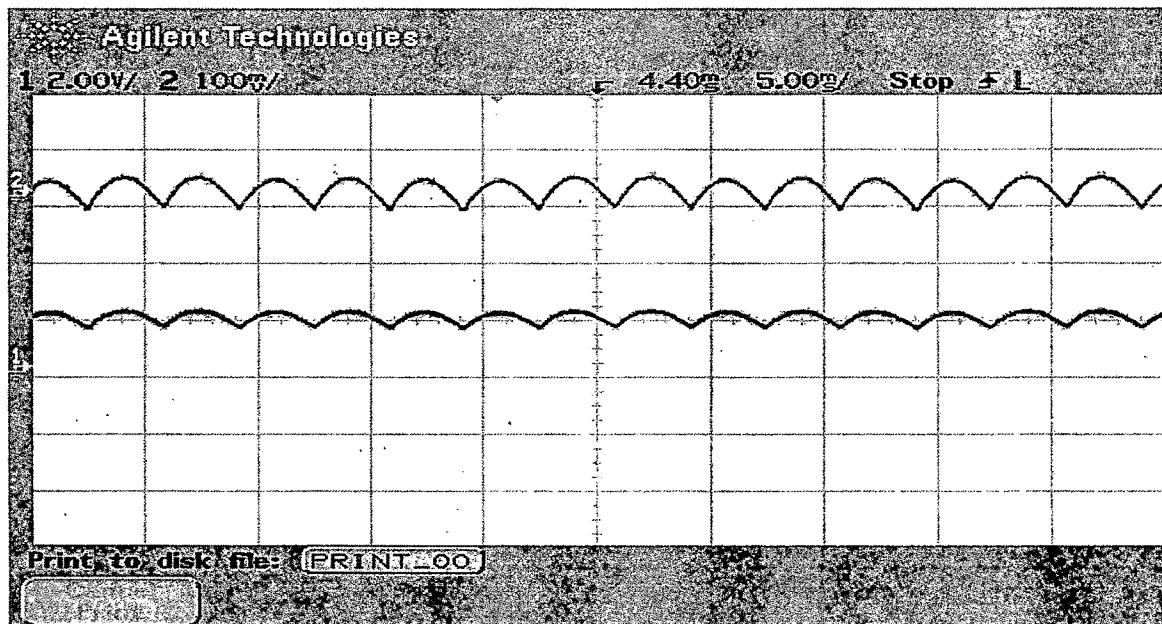


Fig D-2.1 p_{ac} AND p (Active Power)

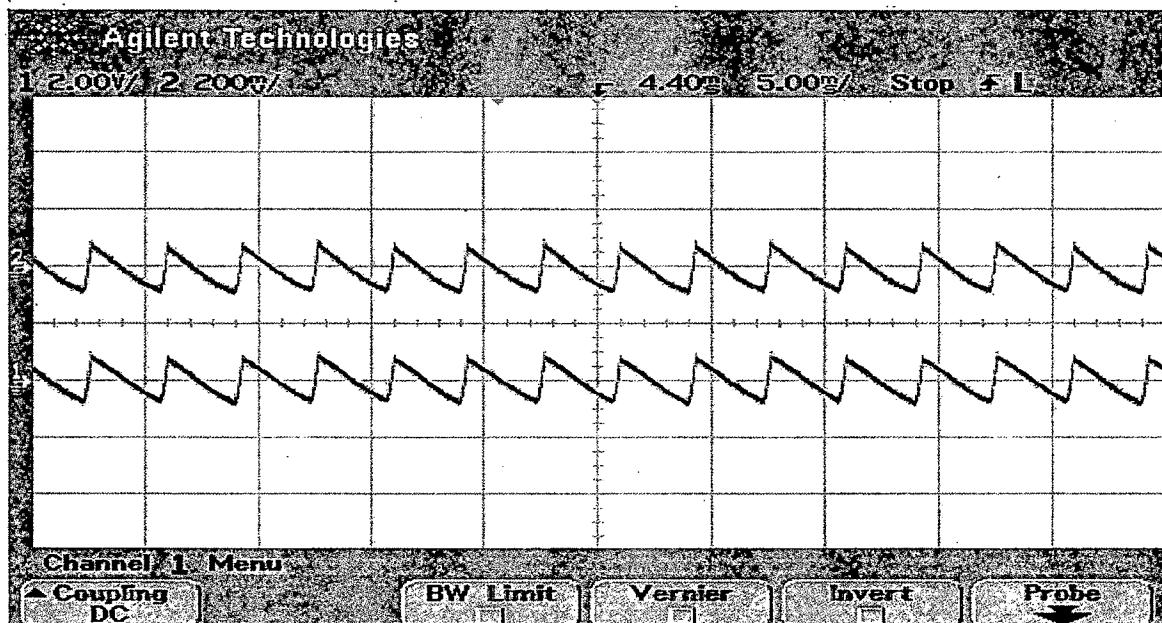


Fig D-2.2: q_{ac} AND q (REACTIVE POWER)

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D-3 Compensating Reference Currents (2 ϕ)

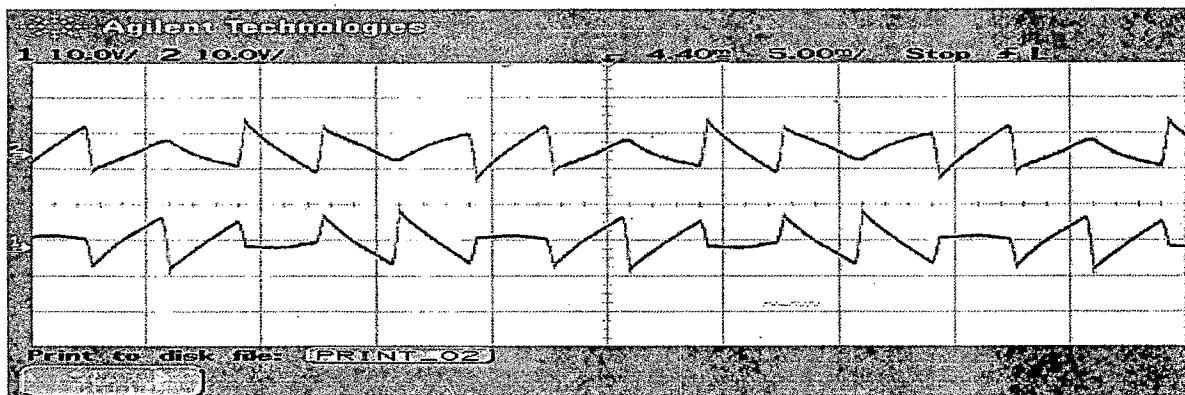


Fig D-3.1 i_{ca} and i_{cb} (α and β Phase)

D-4 Compensating Reference Currents (3 ϕ)

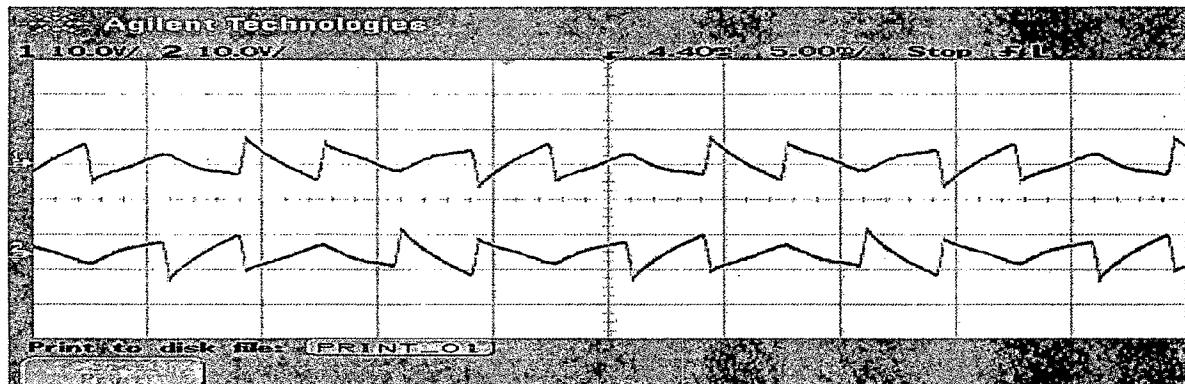


Fig D-4.1 i_{ca} , and i_{cb} (Phase-A and Phase-B)

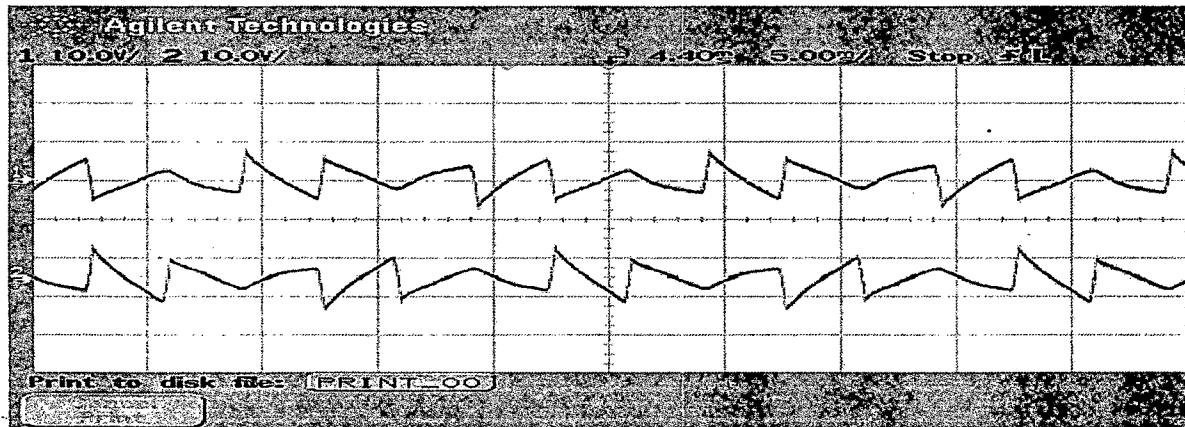


Fig D-4.2: i_{ca} , and i_{cc} (Phase-A and Phase-c)

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D-5 Source Voltage and Load Currents (3 ϕ)

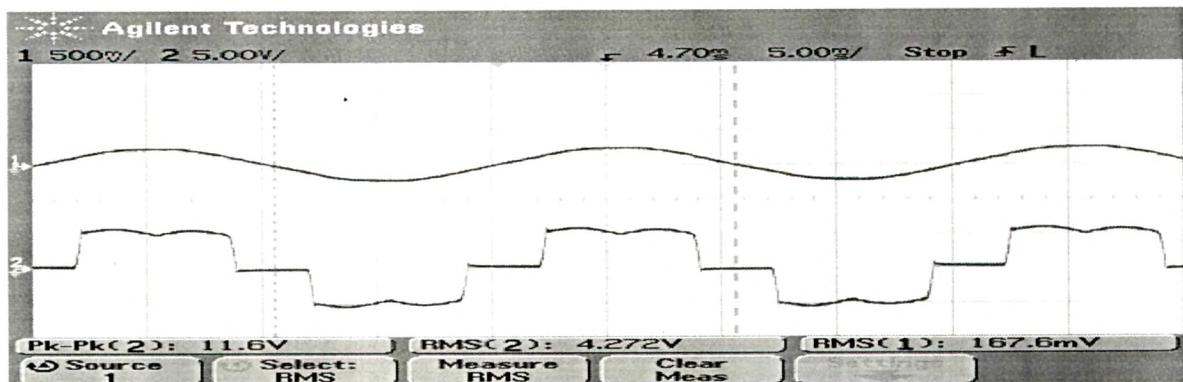


Fig D-5.1: Phase A

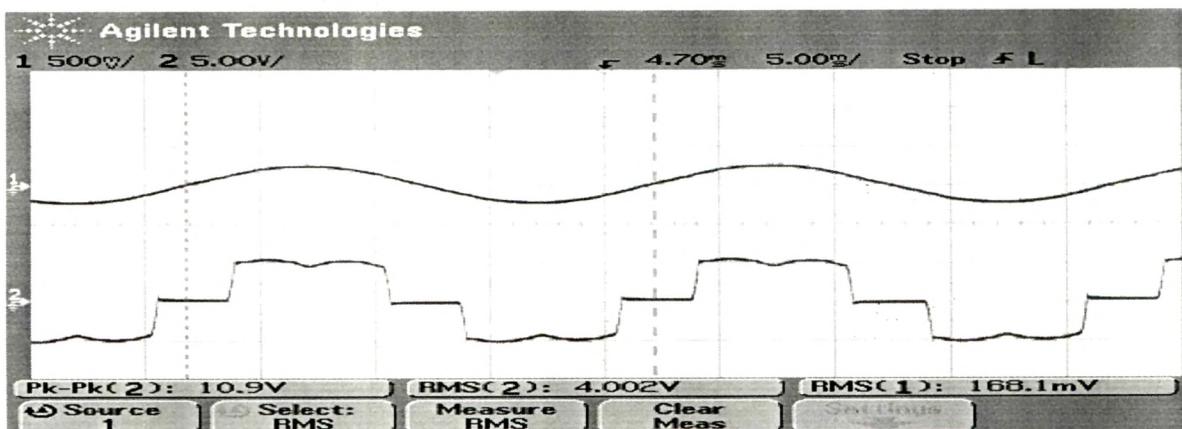


Fig D-5.2: Phase B

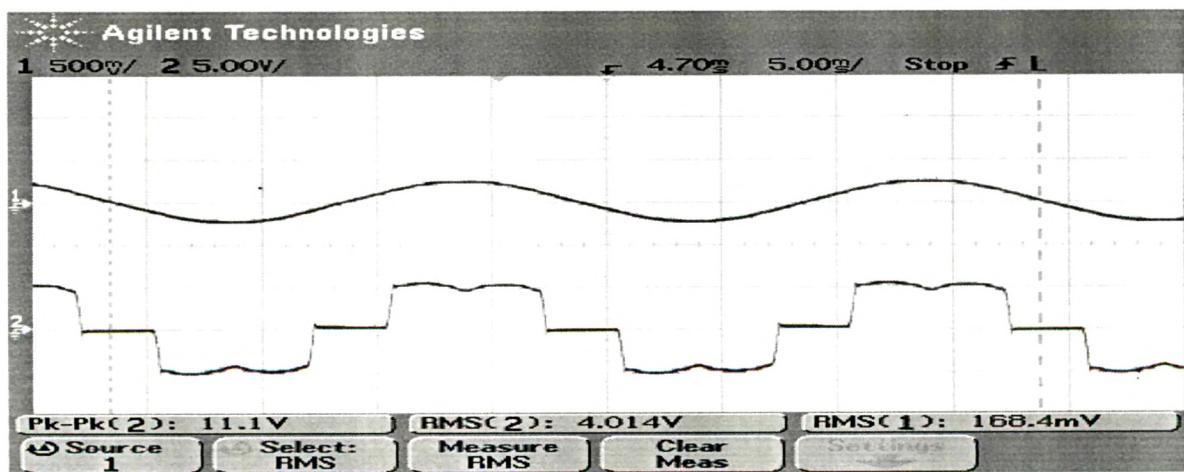


Fig D-5.3: Phase C

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D-6 Source Voltage and Compensating Currents (3 φ)

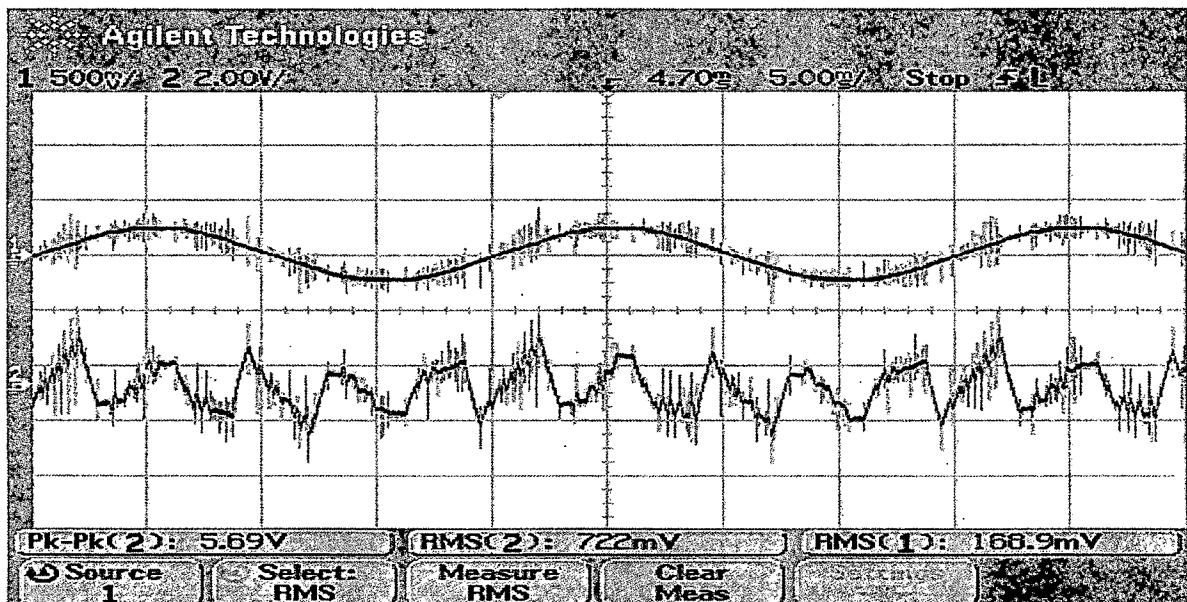


Fig D-6.1: PHASE-A

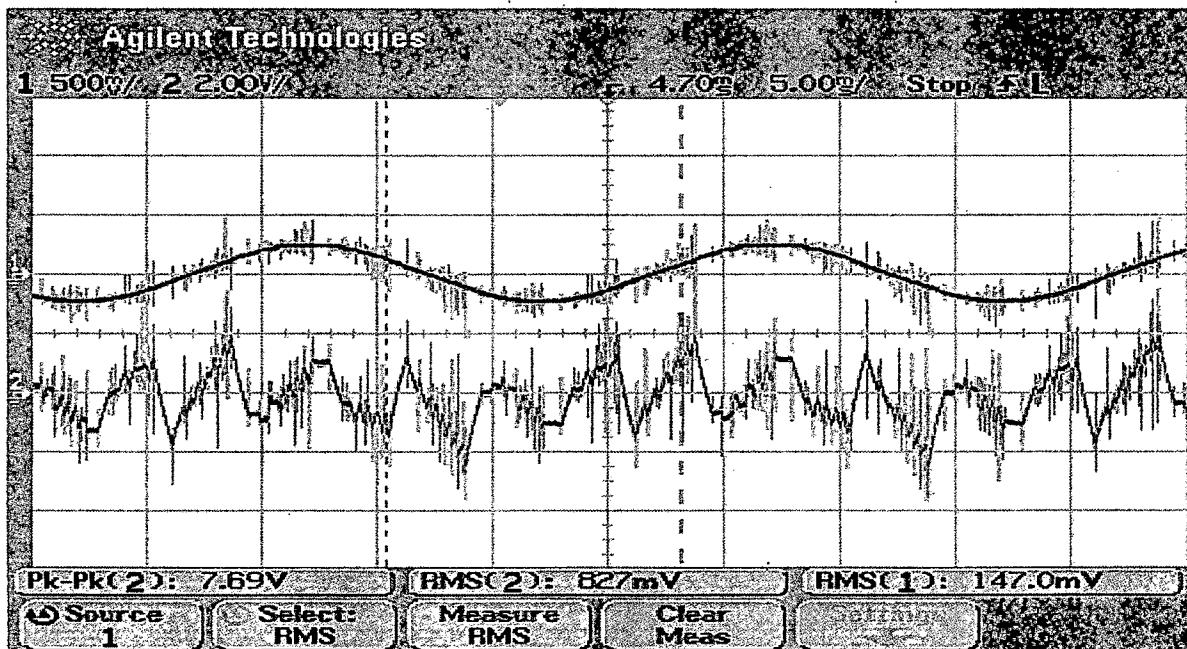


Fig D-6.2: PHASE B

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D-7 Source Current and Source Voltage (3 φ)

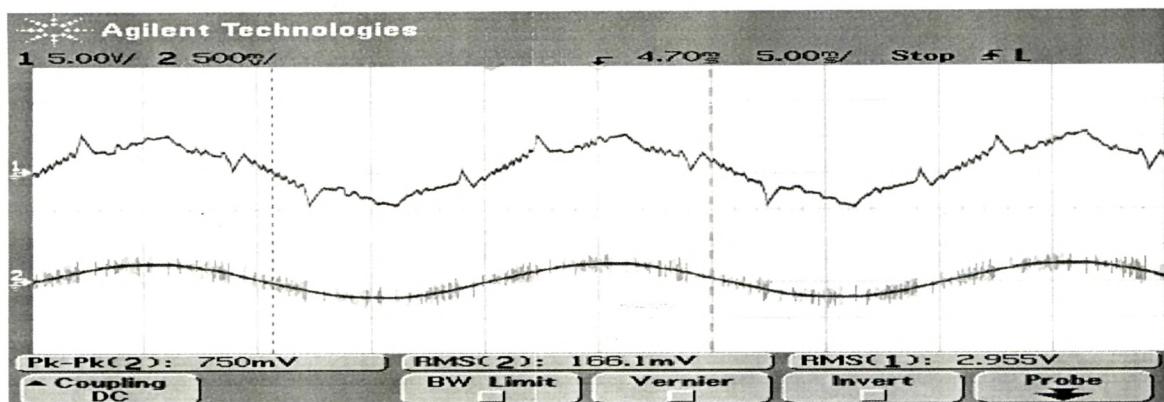


Fig D-7.1: PHASE-A

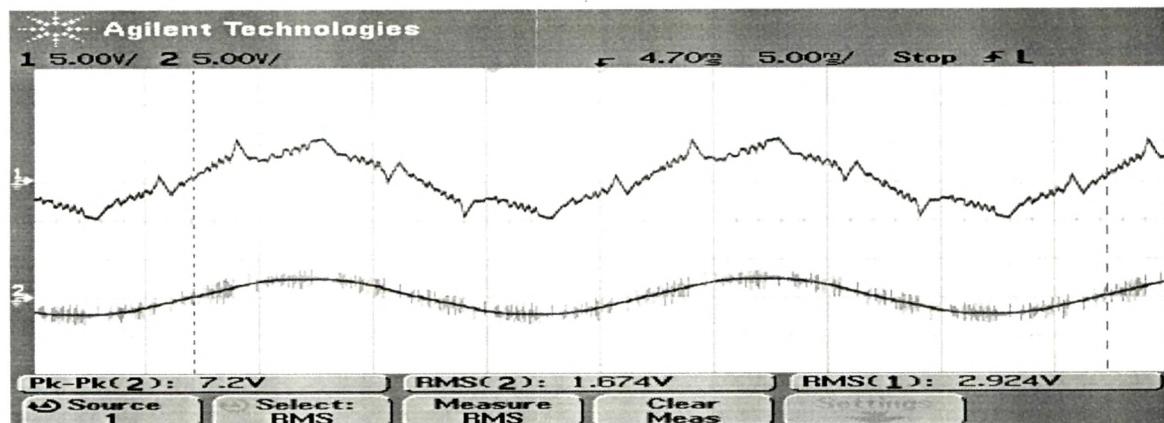


Fig D-7.2: PHASE-B

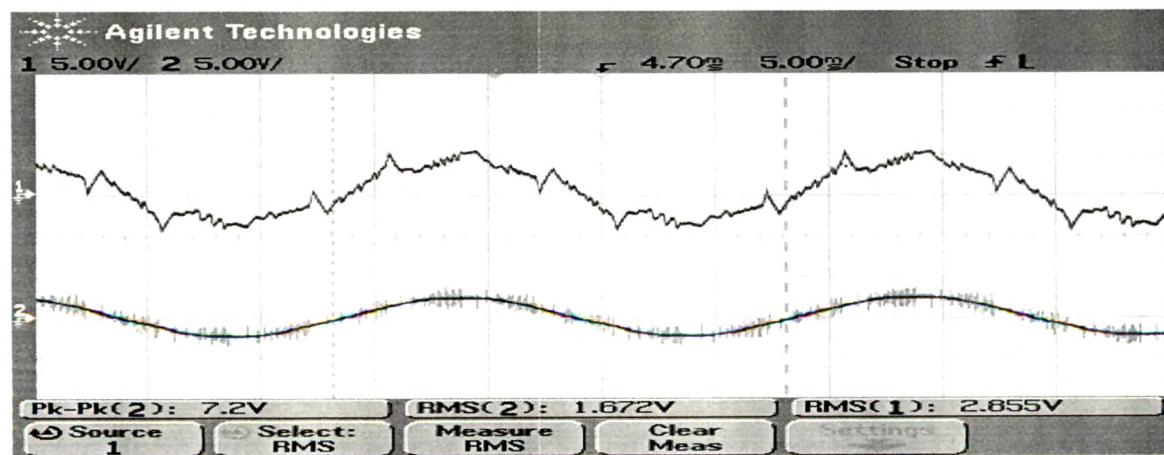


Fig D-7.3: PHASE-C

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D-8 v_{ce} and Compensating Current

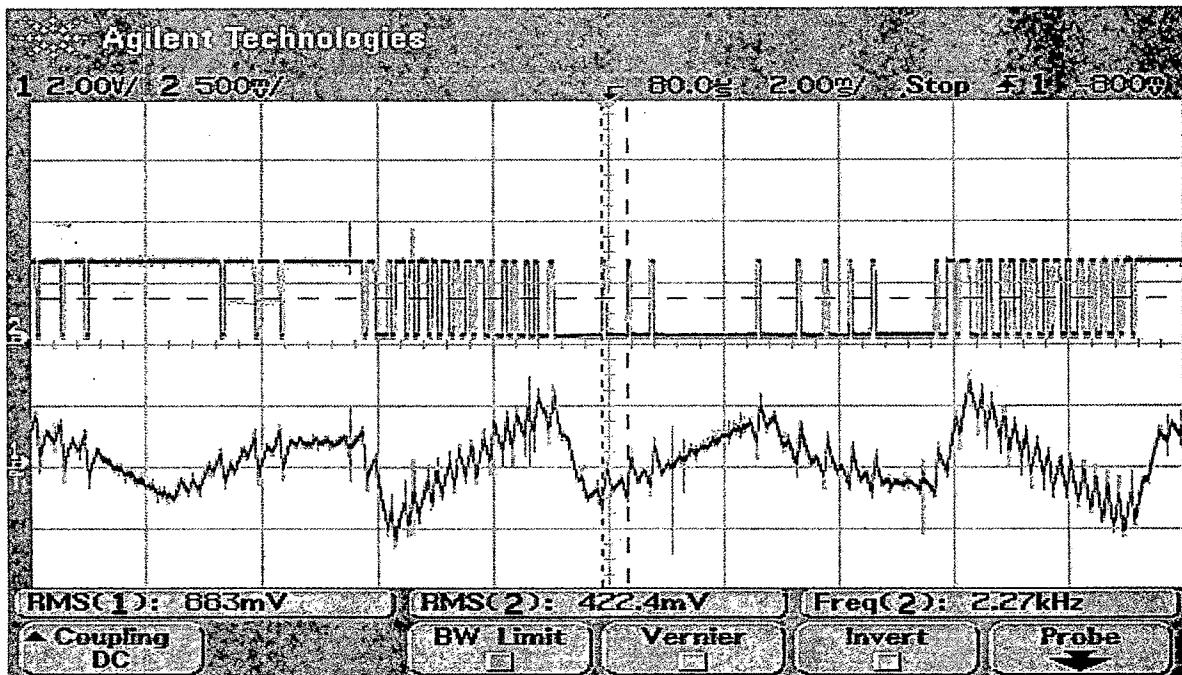


Fig D-8.1: UPPER IGBT PHASE- A

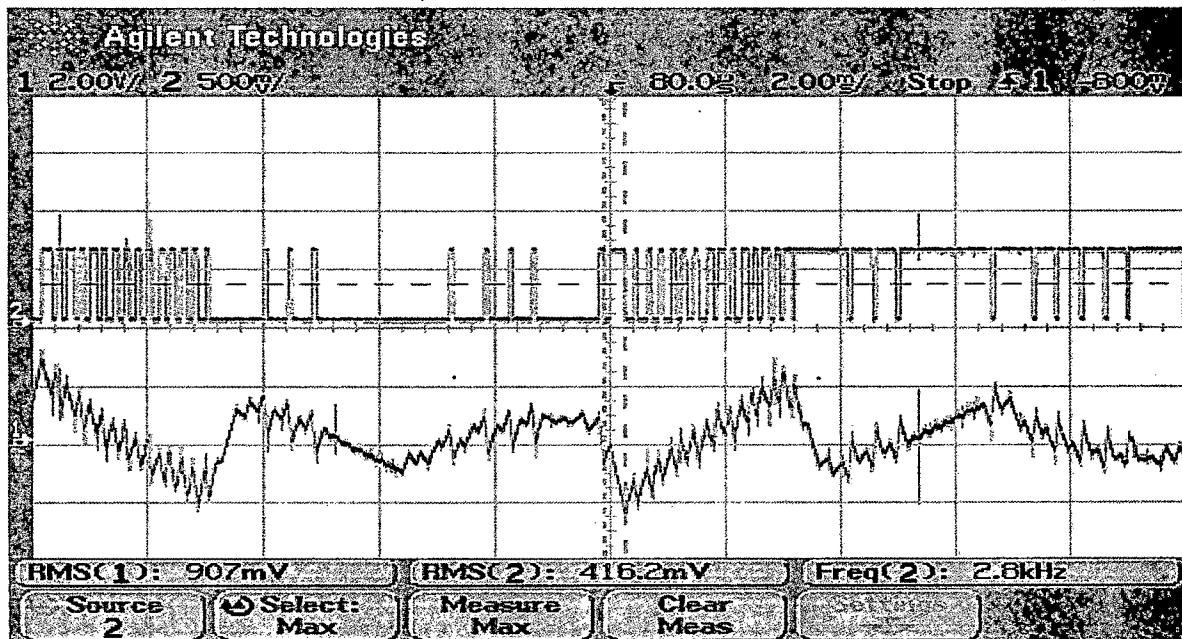


Fig D-8.2: V_{ce} and COMPENSATING CURRENT

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D-9 Gate Pulse and Compensating Current

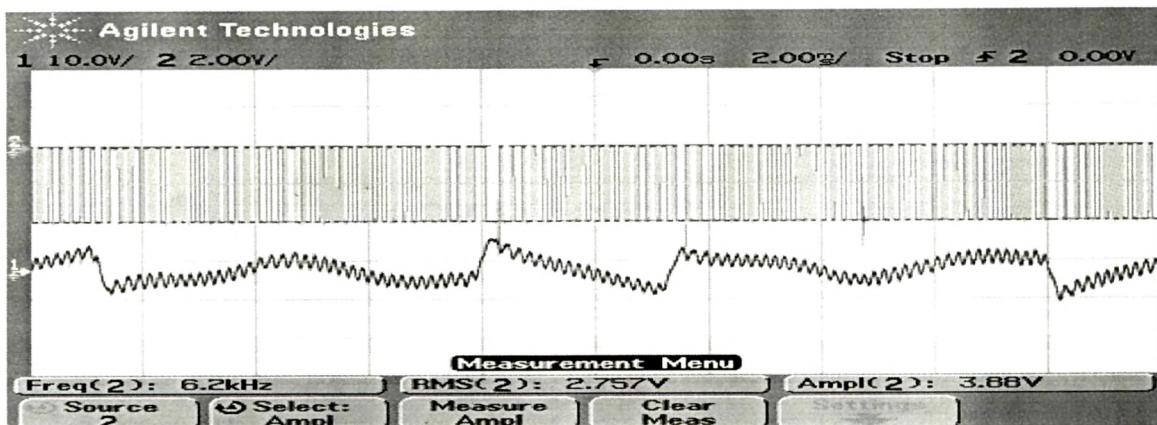


Fig D-9.1: UPPER IGBT A-PHASE

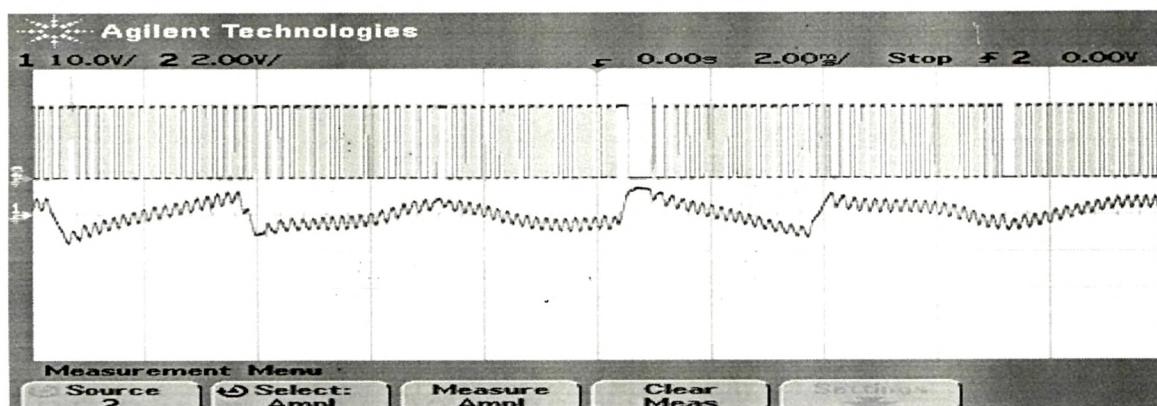


Fig D-9.2 LOWER IGBT A-PHASE

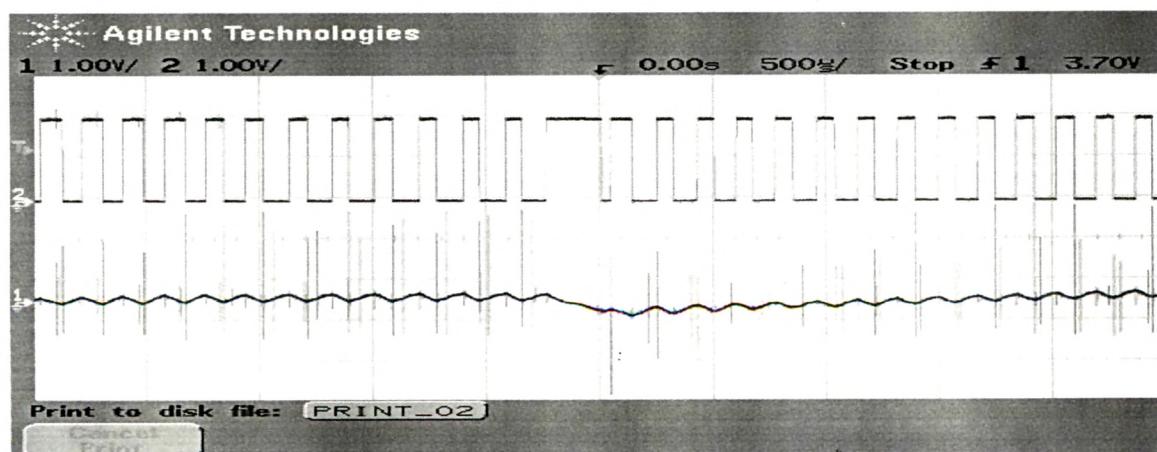


Fig D-9.3: UPPER IGBT: Phase-A (Zoomed)