APPENDIX-D SUMMARY OF RESULTS

D1: Response of the control input

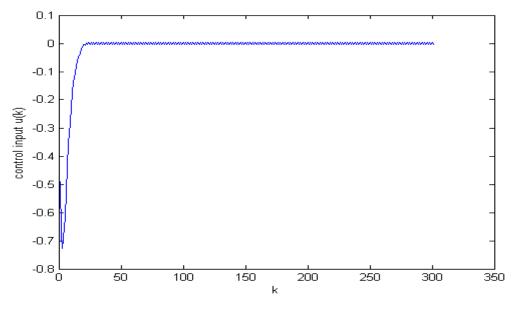


Figure 2. 17 Control Input u

D2 : : Response of the sliding surface

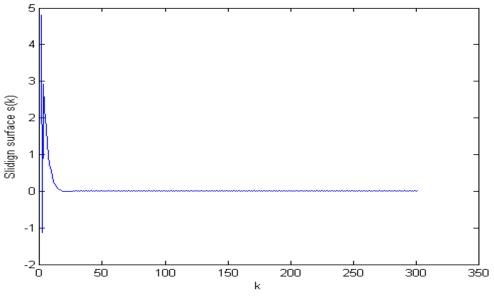
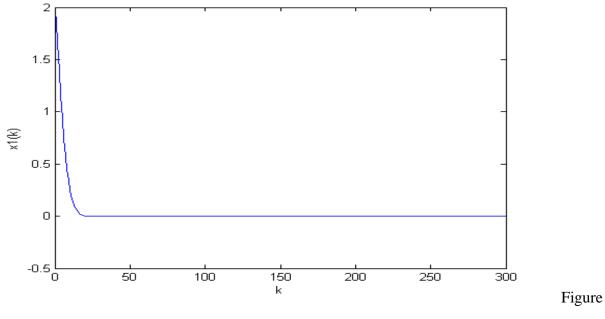


Figure 2.18 Sliding Surface S

D3: Response of the Position state



2.19 *Position state* x_1

D4: Response of the Angular velocity state

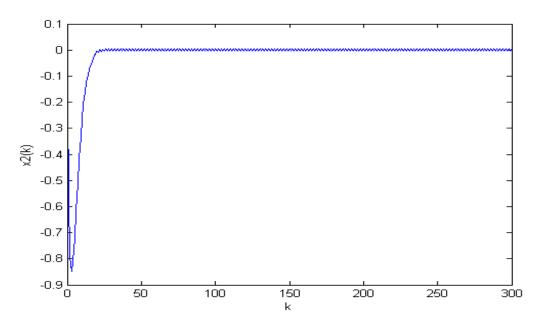
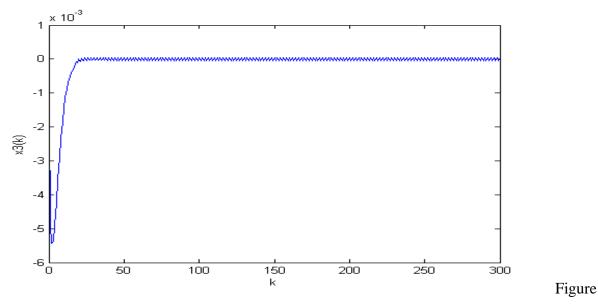
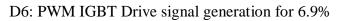


Figure 2.20 Angular velocity state x₂

D5: Response of Armature current state x3



2.21 Armature current state x3



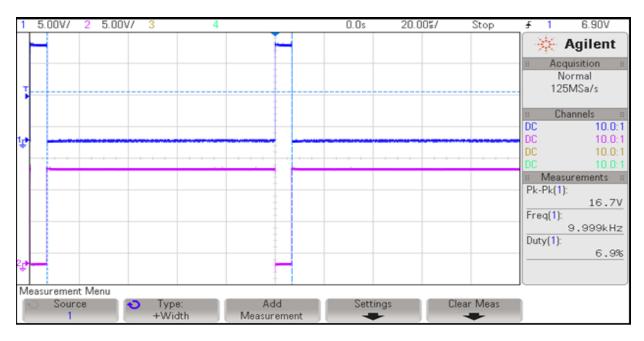


Figure A. 28 PWM for 6.9% duty cycle

D7: PWM IGBT Drive signal generation for 25.2%

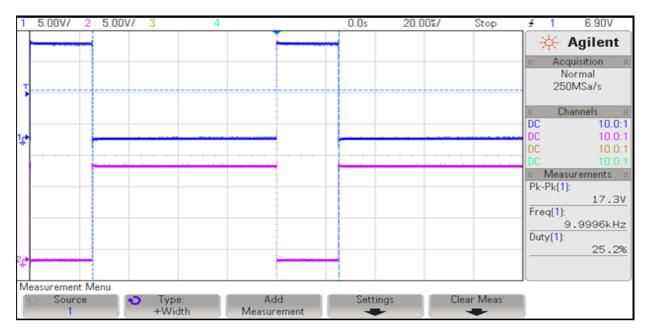


Figure A.29 PWM for 25.2% duty cycle

D8: PWM IGBT Drive signal generation for 6.9%

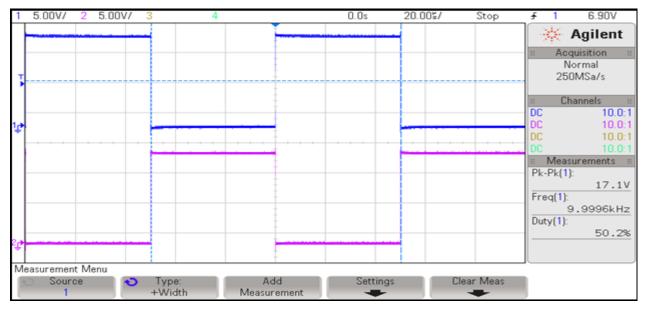


Figure A.30 PWM for 50.2% duty cycle

D9: PWM IGBT Drive signal generation for 75.2%

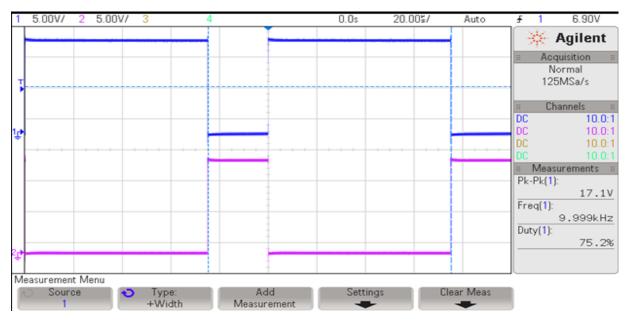


Figure A.31 PWM for 75.2% duty cycle

D10: PWM IGBT Drive signal generation for 93.6%

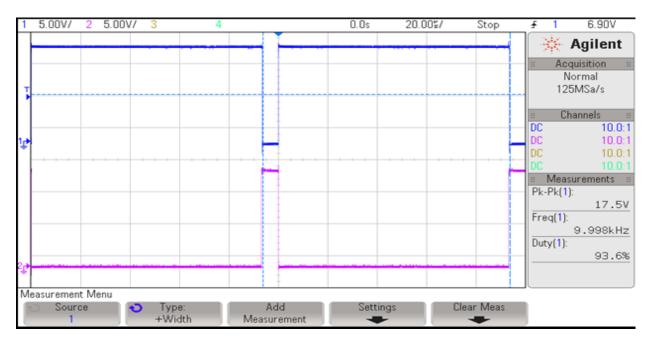


Figure A.32 PWM for 93.6% duty cycle

D11: IGBT Gate pulse generation from DSP

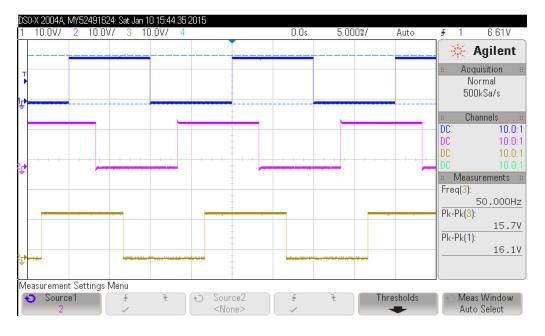


Figure 5.2 Gate pulses from DSP

D12: Normal and Inverted Gate pulses

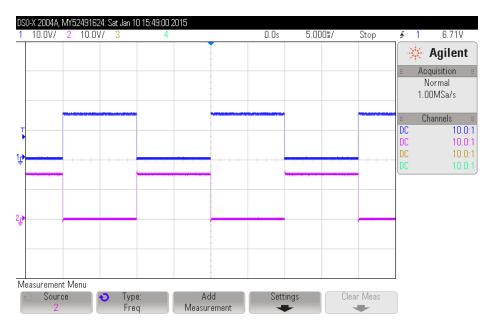
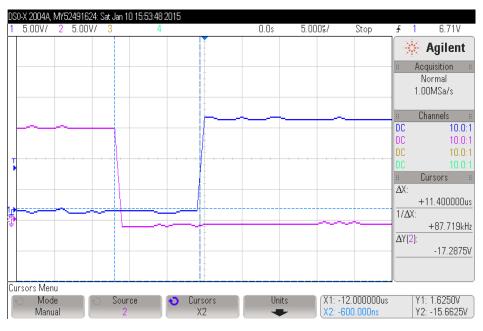
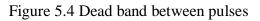


Figure 5.3 Inverted Gate pulse from DSP



D13: Dead Band between Pulses



D14: Line-Line Output voltage

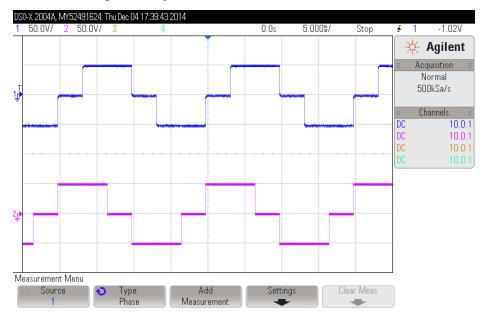


Figure 5.5 Output Voltage between R-Y and Y-B phases

D15: Pulse generation using DSP

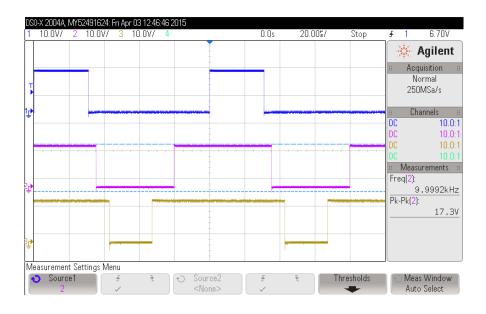


Figure 5. 9 Drive signals for three phase voltage source inverter

D16 : Another view of Pulse Generation using DSP

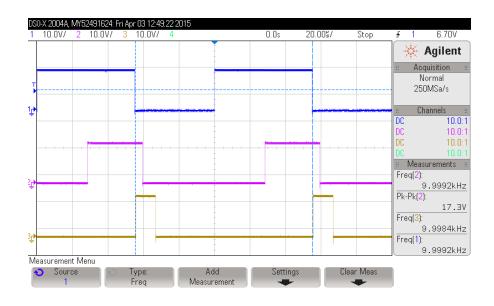


Figure 5.10 High Frequency drive signal



D17:Dead Band between Pulses

Figure 5. 11 Dead band between normal & inverted drive signal

D18: Result of Output voltage

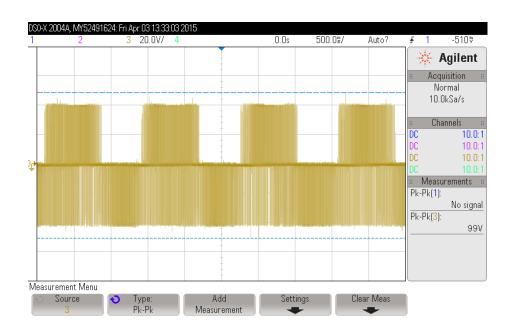


Figure 5. 12 Output voltage of inverter

D19: Insight view of Output voltage

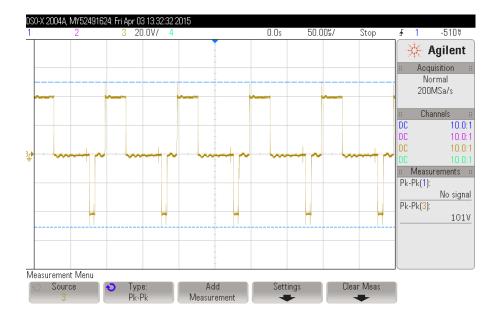


Figure 5.13 Insight view