DESIGN AND IMPLEMENTATION OF DSP BASED CONTROL OF HYBRID CASCADED MULTILEVEL INVERTER USING VARIOUS NOVEL PULSE WIDTH MODULATION TECHNIQUES

A

Thesis submitted for the award of the Degree

of

DOCTOR OF PHILOSOPHY

In

Electrical Engineering

By

Mrs. Meeta K. Matnani

ELECTRICAL ENGINEERING DEPARTMENT

FACULTY OF TECHNOLOGY AND ENGINEERING

THE MAHARAJA SAYAJIRAO UNIVERSITY OF BARODA,

VADODARA-390001

GUJARAT, INDIA

FEBRUARY 2014

DEDICATED

TO

MY FAMILY

AND

TEACHERS

Anyone who stops learning is old, whether at twenty or eighty. Anyone who keeps learning stays young. The greatest thing in life is to keep your mind young.

Henry Ford

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Certificate

This is to certify that the thesis entitled ***'Design and Implementation of DSP Based Control of Hybrid Cascaded Multilevel Inverter Using Various Novel Pulse Width Modulation Techniques'*** submitted by ***Mrs. Meeta K Matnani*** in fulfillment of the degree of ***DOCTOR OF PHILOSOPHY*** in ***Electrical Engineering Department***, Faculty of Technology & Engineering, The Maharaja Sayajirao University of Baroda, Vadodara is a bonafide record of investigations carried out by her in the Department of Electrical Engineering, Faculty of Technology & Engineering, The Maharaja Sayajirao University of Baroda, Vadodara under my guidance and supervision. In my opinion the standards fulfilling the requirements of the Ph.D. Degree as prescribed in the regulations of the University has been attained.

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Declaration

I, **Mrs. Meeta K. Matnani** hereby declare that the work reported in this thesis entitled **'Design And Implementation of DSP Based Control of Hybrid Cascaded Multilevel Inverter Using Various Novel Pulse Width Modulation Techniques'** submitted for the award of the degree of **DOCTOR OF PHILOSOPHY** in Electrical Engineering Department, Faculty of Technology & Engineering, The Maharaja Sayajirao University of Baroda, Vadodara is original and has been carried out in the Department of Electrical Engineering, Faculty of Technology & Engineering, The Maharaja Sayajirao University of Baroda, Vadodara. I further declare that this thesis is not substantially the same as one, which has already been submitted in part or in full for the award of any degree or academic qualification of this University or any other Institution or examining body in India or abroad.

February 2014 **Mrs. Meeta K Matnani**

Acknowledgements

I express my thanks to **Almighty** for providing me inspiration, strength, energy and patience to start and accomplish my work with the support of all concerned a few of them I am trying to acknowledge.

It is great pleasure and privilege to have an opportunity to work on the project entitled "Design and Implementation of DSP Based Control of Hybrid Cascaded Multilevel Inverter using Various Novel Pulse Width Modulation Techniques". I would like to express my sincere gratitude to my guide **Dr. Hina B. Chandwani,** for her inspiring guidance and invaluable suggestions that has been the driving force in the success of my project work and who has been main source of inspiration throughout the course of work.

I am also grateful to **Mr. B. B. Modasia, Proprietor, Control System Engg., GIDC Makarpura, Vadodara** for his technical suggestions, guidance and providing laboratory facilities for implementation of hardware. I am also thankful to his technical assistant **Mr. D. M. Kapre** for helping me in hardware implementation.

I thank **Prof. S. K. Shah**, Ex-Head and **Prof. S. K. Joshi**, Head, Electrical Engineering Department, Faculty of Technology & Engineering, The Maharaja Sayajirao University of Baroda, Vadodara for their valuable time, guidance, support and suggestions. I am really thankful to them as they allowed me to work in the department as Ph. D. student.

I would like to thank all teaching and non-teaching staff of Electrical Engineering Department, Faculty of Technology and Engineering, The Maharaja Sayajirao University of Baroda, Vadodara for providing me co-operative environment.

I am thankful to **Mr. Nitin Paranjape (Managing Director), Edutech Systems, Vadodara** for his technical support and providing laboratory facilities for implementation and testing of software of the project.

I am thankful to **Department of Science and Technology(DST), New Delhi, India** for sponsoring the research project under **Women Scientist Scheme(WOS-A) Disha Programme.**

I express my thanks to all my colleagues for their help and throughout support. Last but not least, I express my thanks to **my family** for all support, inspiration and love provided to me with all inconveniencies caused because of my engagement in this work.

Mrs. Meeta K.Matnani

Abstract

Multilevel inverter and hybrid multilevel inverter play important role in medium and high voltage industries. In this project these multilevel inverters are compared and work is done for hybrid multilevel inverter. Different topologies are available for multilevel inverters. Some of them are simulated and their working is understood.

Over modulation, linear range of modulation, switching states, switching frequency and capacitor charge maintenance are contributing factors in limiting the capability and performance of the multilevel inverter. Anyhow higher order harmonics can be controlled by changing the switching frequency. Hybrid multilevel inverter systems are designed to work in environments with as many modulation techniques as possible in varying power conditions. Multilevel inverter and hybrid multilevel inverter have emerged as one of the most promising approaches for high voltage inverter with lowest total harmonic distortion, lower voltage stress on switches and increased approximation towards sinusoidal wave. Hybrid multilevel inverter also provides very high efficiency over normal inverter.

The aim of the project is simulation, design and implementation of hybrid multilevel inverter. Simulations are carried out for cascaded multilevel inverter and different hybrid multilevel inverter for comparison.

In this project hybrid multilevel inverter is controlled by multi carrier pulse width modulation techniques like PDPWM, PODPWM, APODPWM and THIPDPWM obtained using DSP. All these modulation techniques are adapted for selected HMLI which in general are implemented for either cascaded multilevel inverter, symmetrical or asymmetric hybrid multilevel inverter or other multilevel inverter. In that way all these modulation techniques are novel for this work. The combination of MATLAB/SIMULINK, CCS, emulator and DSP is used for controlling of system. The software based control developed for optimization of hybrid Multilevel Inverter system give provisions for configuration changes or further development.

If this system is to be made portable then batteries can be used. Here testing is done on batteries as well as regulated power supply. Regulated power supply is developed for high voltage and current rating.

The work presents the use of different modulation techniques, simulation, analysis and implementation of the control of hybrid multilevel inverter. Regulated power supply for DC 40V/80V is developed with 5A current rating. Simulations are for

single phase cascaded multilevel inverters (five level, seven level and nine level) and THD is compared.

Simulations are also done for different hybrid multilevel inverters like asymmetric hybrid multilevel inverter, symmetrical hybrid multilevel inverter and half bridge module based hybrid multilevel inverter with single phase and three phase configurations. Simulations are done with and without modulation. For simulated circuits with modulation THD is varying from 0.6% to 1.8% for different topologies with different modulation techniques for single phase and three phase.

Similarly, simulations are done for selected hybrid multilevel inverter with different modulation techniques for single phase and three phase and comparison is done on basis of THD. For single phase THD varies from 1.15% to 1.52% and for three phase THD varies from 0.84% to 1.41%.

The selected hybrid multilevel inverter is designed for single phase and three phase. In the project multicarrier modulation techniques like PD, POD, APOD and THIPDPWM are implemented with constant modulation index which can be changed to achieve different results.

THD obtained as low as 1.2% from hardware and 0.19% from simulations. This system can work for 1.5 kW power output.

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ACRONYMS

AHMLI	Asymmetric Hybrid Multilevel Inverter
AHPWM	Alternative Hybrid Pulse Width Modulation
APODPWM	Alternative Phase Opposition Disposition Pulse Width Modulation
ADC	Analog to Digital Converter
CAN	Controller Area Network
CCS	Code Composer Studio
CHB	Cascaded H Bridge
CM	Common Mode
CMLI	Cascaded Multilevel Inverter
COPWM	Carrier Overlapping Pulse Width Modulation
DCMLI	Diode Clamped Multilevel Inverter
DSC	Digital Signal Controller
DSO	Digital Storage Oscilloscope
DSP	Digital Signal Processor
EPB	Educational Practice Board
EV	Electric Vehicle
FACTS	Flexible Ac Transmission System
FCMLI	Flying Capacitor Multilevel Inverter
FFT	Fast Fourier Transform
GPIO	General Purpose Input Output
GTO	Gate turn off Thyristor
HCMLI	Hybrid Cascaded Multilevel Inverter
HEV	Hybrid Electric Vehicle
HLCCAPOPWM	Higher And Lower Carrier Cells And Alternative Phase Opposition Pulse Width Modulation
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate Commutated Thyristors
ISPWM	Inverted Sine Carrier Pulse Width Modulation
I/O	Input Output
JTAG	Joint Test Action Group
LED	Light Emitting Diode

MC-PWM	Multi Carrier Pulse Width Modulation
MC-SFO PWM	Multi Carrier Switching Frequency Optimal Pulse Width Modulation
MC-SH PWM	Multi Carrier Sub- Harmonic Pulse Width Modulation
MLI	Multilevel Inverter
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MUX	Multiplexer
MV	Medium Voltage
NPC	Neutral Point Clamped
PDPWM	Phase Disposition Pulse Width Modulation
PODPWM	Phase Opposition Disposition Pulse Width Modulation
PSC-SFO PWM	Phase Shifted Carrier Switching Frequency Optimal Pulse Width Modulation
PSPWM	Phase Shifted Pulse Width Modulation
PS-SUB-PWM	Phase-Shifted Suboptimal Carrier Pulse Width Modulation
PWM	Pulse Width Modulation
SDCS	Separate DC Sources
SHE-PWM	Selective Harmonic Elimination Pulse Width Modulation
SHPWM	Sub Harmonic Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion
THIPDPWM	Third Harmonic Injection Phase Disposition Pulse Width Modulation
UART	Universal Asynchronous Receiver/Transmitter
VFISPWM	Variable Frequency Inverted Sine Carrier Pulse Width Modulation
VFPWM	Variable Frequency Pulse Width Modulation
VSI	Voltage Source Inverter
μF	microfarad
kΩ	Kilo ohm
ma	Amplitude Modulation Index
mf	Frequency Modulation Index

CHAPTER 1

INTRODUCTION

Multilevel inverters (MLI) have very important development for medium voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. Multilevel inverters refer to the inverters with output which have more than two voltage levels possible with respect to pole. The feature of having an output voltage level that is higher than those of the power semiconductor switching devices' ratings puts the MLIs in high power inverters class. The application of MLIs has been extended to the medium power range due the advantages of reduced distortion, dv/dt stress and common mode voltage [1]–[3].

1.1 OVERVIEW

The cascaded H-bridge inverter (CHB) is a MLI topology with a modular structure. The main drawback of a CHB inverter is the need for a large number of isolated dc supplies [4]-[6]. To ease this problem hybrid multilevel inverters created by cascading smaller dissimilar inverter circuits are suggested [7].

Hybrid inverters have different approaches to achieve the goal of multilevel output such as: Employing different power switches like GTO and IGBT in cascade thus operating at low and high frequency[8] or modifying the series connection of cascade connected MLI[9] or obtaining multilevel output with combination of inverter and converter[10],[11] or replacing the dc supply of the lower voltage stages with capacitors and controlling the inverter to receive zero average power from the capacitor-fed stages [12], [13] or replacing the highest voltage cascaded stages with a singly-supplied inverter such as a basic 2-level, six-switch inverter [14] or a multilevel neutral point clamped stage [15] or supplying various hybrid inverter stages using the same dc source and isolating the outputs using a multi primaries transformer [16], [17] but this option is not suitable when a wide frequency range including very low frequency is needed and also by applying half bridge inverter cascaded with H bridge inverter[18] with single DC source or separate DC sources.

Multicarrier pulse width modulation (PWM) inverters have been developed to overcome shortcomings in solid-state switching device ratings, so that large motors can be controlled by high-power adjustable-frequency drives. Multilevel inverters can operate at both fundamental switching frequency and high frequency switching.

The different PWM schemes of multilevel inverters are classified into two types the multi carrier Sub- Harmonic pulse width modulation (MC-SH PWM) and the multi carrier switching frequency optimal pulse width modulation (MC-SFO PWM), Sub Harmonic PWM (SHPWM), Phase Shift PWM (PSPWM), Variable Frequency PWM

(VFPWM) and Carrier Overlapping PWM (COPWM) techniques employed for various modulation indices using spectrum of the output voltage. Other performance measures from above modulation techniques such as crest factor, form factor etc. and the use of inverter state redundancies to perform additional application specific control tasks.

For all above modulation techniques, the switching devices of the main power stage switch once per cycle for different modulation indices. This is suitable for the high power semiconductor devices. Stress on the devices is reduced and total harmonic distortion (THD) is also reduced.

The multicarrier PWM method uses several triangular carrier signals, keeping only one modulating sinusoidal signal. For an n level inverter n-1 carriers are employed [19] – [20]. The carriers have the same frequency and same peak to peak amplitude but are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency 50 Hz. At every instant each carrier is compared with the modulating signal. Each comparison gives high level or low level output if the modulating signal is greater or smaller than the triangular carrier respectively. The results are added to give the voltage level, which is required at the output terminal of the inverter.

Different multicarrier PWM methods include Phase Disposition (PD) Method [21], Alternative Phase Opposition Disposition (APOD) Method, Phase Opposition Disposition (POD) Method, Phase Shifted (PS) Method [22] and Hybrid Modulation Technique [23]-[26]. Different modulation techniques for hybrid multilevel inverter are studied in simulations and results are compared.

Other modulation techniques are also studied such as Multicarrier Sub Harmonic Pulse Width Modulation (MC-SH PWM)[27], Multi Carrier Switching Frequency Optimal PWM (MC-SFO PWM)[28], Phase Shifted Carrier Switching Frequency Optimal Pulse Width Modulation (PSC-SFO PWM)[29] and HLCCAPOPWM control technique [30].

The research will have an impact such that THD, stress on the devices are reduced. This project aims at developing a multilevel inverter using various pulse width modulation. It will be possible to implement the developed pulse width modulation techniques for linear range of modulation.

There are several types of multilevel inverters but the one considered in this work is the hybrid cascade multilevel inverter (HCMLI). HCMLI has many distinct features particularly in terms of its structure which is simple and modular.

Most multilevel inverters have an arrangement of switches and capacitor voltage sources. By a proper control of the switching devices, these can generate stepped output voltages with low harmonic distortions. These multilevel inverters are widely used in manufacturing factories and acquired public recognition as one of the new power inverter fields because they can overcome the disadvantages of traditional pulse width-modulation (PWM) inverters. The selected hybrid cascaded multilevel inverter includes a standard 3-leg inverter (one leg for each phase) and H-bridge in series with each inverter leg. It can use only a single DC power source to supply a standard 3-leg inverter along with three full H-bridges supplied by capacitors. But in this work separate four DC sources are used instead of capacitors because capacitors were not easily available. In case capacitor were used, balancing of capacitor is main task. Multilevel carrier based PWM method is used to produce a five level phase voltage. Control for this hybrid MLI is obtained using DSP 28335. Control signals are generated using MATLAB/SIMULINK (2013) in discrete model, code is generated using CCS 3.3/ CCS 5.1, which is loaded in EPB28335 using Emulator xds510USB.

The features and discussions of research carried out in the thesis includes:

- Survey of different modulation techniques, power circuits and limitations of existing topologies of Hybrid multilevel inverter (HMLI) with control circuitry.
- Comparison of different modulation techniques applied to different hybrid multilevel inverter topologies on the basis of THD using MATLAB simulation
- MATLAB simulations for selected HMLI (single phase and three phase) with different modulation techniques.
- Effect of amplitude modulation index (referred as modulation index in this work) and frequency modulation index on Total harmonic distortion (THD) for HMLI using MATLAB simulations.
- Design and development of power circuit for HMLI.
- Realization of hardware circuit using MOSFET/IGBT.
- Control signal realization using EPB28335 with CCS3.3 and emulator xds510usb
- Designing and implementation of interfacing card.
- Implementation of selected HMLI for low and high power output (single phase and three phase) with different modulation techniques using EPB28335.
- Testing of hardware circuit and comparison with simulated results.

1.2 ROADMAP

The thesis is organized as follows:

Chapter 1 This chapter provides an overview and the context for the remainder of the thesis. It also introduces the present trends in Multilevel inverter. It presents the significance and scope of work to be carried out in the thesis.

Chapter 2 This chapter gives comparative study of multilevel inverters and evolution of hybrid multilevel inverter. Hybrid multilevel inverters are classified on basis of power devices used, power supplies used and configuration of power devices. Other classification is based on modulation technique applied

Chapter 3 This chapter introduces different modulation techniques that can be applied to multilevel inverter. More focus is on multicarrier based modulation techniques. Discussion is related with modulation index which is based on modulation index and frequency modulation index.

Chapter 4 In this chapter MATLAB simulations carried out for different cascaded multilevel inverters and hybrid multilevel inverters are discussed to finalize the topology of this project. Important factors to be considered are total harmonic distortion, number of power supplies and number of power devices. Also output levels are decided initially.

Chapter 5 In this chapter MATLAB simulations are carried out for single phase and three phase with different modulation techniques and results are discussed for selected topology.

Chapter 6 In this chapter controlling of power switches is discussed. The processor used for controlling switching pattern of power circuit is TMS28335 with code composer studio and emulator. Control signals are obtained using MATLAB SIMULINK with Code Composer Studio and Emulator. All these interfaces are discussed in detail. This chapter describes steps involved in generation and application of control signals to power circuit.

Chapter 7 Design of the power circuit of hybrid multilevel inverter for five level output is described in this chapter. Design is for single phase and three phase circuits. Circuit is designed for low as well as high power rating. This chapter also describes regulated power supply design.

Chapter 8 In this chapter results obtained from hardware are given and compared with simulation results.

Chapter 9 Conclusion and further possible expansion with respect to output power and load applied are discussed in this chapter. Also applications could be open loop or closed loop as per requirement.

Chapter 10 Thesis ends with Bibliography which includes the list of references used in each chapter.

CHAPTER 2

MULTILEVEL INVERTER to HYBRID MULTILEVEL INVERTER

This chapter gives comparative study of multilevel inverters and evolution of hybrid multilevel inverter.

The idea of multilevel inverters has been introduced since 1975 [1]. The term multilevel began with three level inverter [2]. Thereafter several multilevel inverter topologies have been developed [3–9]. But the basic concept of a multilevel inverter is to obtain high power by using a series of power semiconductor switches. Thus a staircase voltage waveform can be achieved from several low voltage DC sources. Capacitors, batteries and renewable energy voltage sources can be used as the multiple DC voltage sources. The switching of the power switches combine these multiple DC sources in order to achieve high voltage at the output however the rated voltage of the power semiconductor switches depends only upon the rating of the DC voltage sources to which they are connected.

A multilevel inverter achieves high power ratings and also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system for a high power application [10-12]. Thus a multilevel power inverter structure can be utilized as an alternative in high power and medium voltage situations. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM).

2.1 MULTILEVEL INVERTER CONFIGURATION

Many multilevel inverter topologies have been proposed during the last three decades. Modern research has engaged novel inverter topologies and unique modulation schemes. Three different major multilevel inverter structures have been reported in the literature: cascaded H-bridges inverter with separate DC sources, diode clamped (neutral clamped) and flying capacitors (capacitor clamped).

The first topology introduced was the series H-bridge design [1]. This was followed by the diode-clamped multilevel inverter [2,14,15] which utilizes a bank of series capacitors to split the DC bus voltage. After few years the flying-capacitor (or capacitor clamped) [16] topology was introduced in which instead of series connected capacitors floating capacitors are used to clamp the voltage levels. Another multilevel design, slightly different from the previous ones, involves parallel connection of inverter outputs through inter-phase reactors [17]. In this design the switches must block the entire reverse voltage, but share the load current. Various combinatorial designs have

also emerged [18] and been implemented by cascading the fundamental topologies [19-23] such designs come under hybrid topologies category. These designs can create higher power quality for a given number of semiconductor devices than the fundamental topologies due to a multiplying effect of the number of levels.

Moreover, number of modulation techniques and control techniques have been developed for multilevel inverters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), space vector modulation (SVM), multicarrier modulation and others.

In the beginning multilevel inverters were introduced to drive high voltage as in High Voltage Direct Current (HVDC) applications to make the front-end connection between DC and AC lines. In this way the limits on the maximum voltage tolerable by the semiconductor switches were overtaken and the inverters were able to drive directly the line voltage without a transformer.

Nowadays it is possible to find multilevel applications even in low voltage field like motor drive because of the high quality of the AC output. In particular back-to-back multilevel systems can drive motors with very good performance concerning the line voltage and current distortions and also reduces the losses. Recent advances in power electronics have made the multilevel concept practical [2, 14-30]. In fact the concept is so advantageous that several major drive manufacturers have obtained patents on multilevel power inverter and associated switching techniques [4, 31-36].

In addition, many multilevel inverter applications focus on industrial medium-voltage motor drives [7, 37] utility interface for renewable energy systems [38] flexible ac transmission system (FACTS) [39] and traction drive systems.

2.1.1 WORKING PRINCIPLE OF MULTILEVEL INVERTER

General concept of multilevel inverter can be explained in this section which is very popular. In this explanation operation of semiconductors are shown by an ideal switch with several states. The switching pattern of switches and commutation of them allow the addition of the capacitor voltages as temporary DC voltage sources whereas the switches should withstand the voltages of capacitors. Thus Fig. 2.1 shows one phase leg of multilevel inverter with different number of levels [10].

Fig. 2.1(a) is a two-level inverter since the output voltage V_a has only two possible values while Fig. 2.1(b) is a three-level inverter since its output can have three different values. If m is the number of possible output voltage levels it is called m-level inverter shown in Fig. 2.1(c). By increasing the number of levels the output voltage

waveforms will have more steps and thus have a reduced harmonic distortion. However a high number of levels will increase the complexity and introduce voltage imbalance problems.

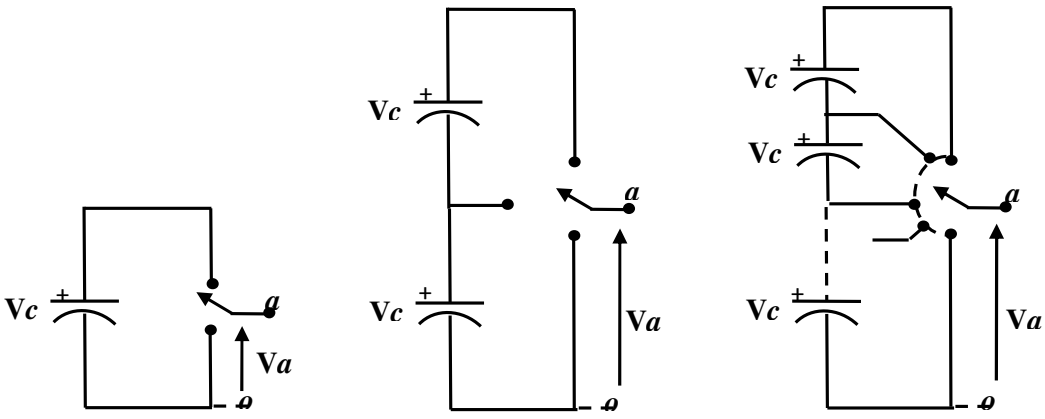


Fig. 2.1 Single leg of multilevel inverter (a) Two level (b) Three level (c) m level

2.2 DIODE CLAMPED MULTILEVEL INVERTER

Fig. 2.2 describes working of a three-level diode-clamped inverter. In this circuit two series-connected bulk capacitors C_1 and C_2 divide the DC-bus voltage. If the middle point of the two capacitors is defined as the neutral point n then the output voltage v_{an} has three states: $V_{dc}/2$, 0 and - $V_{dc}/2$. When switches S_1 and S_2 are turned on then output voltage v_{an} is $V_{dc}/2$ while for – $V_{dc}/2$ output switches S_1'and S_2' are turned on and for the 0 level S_2 and S_1' are switched on.

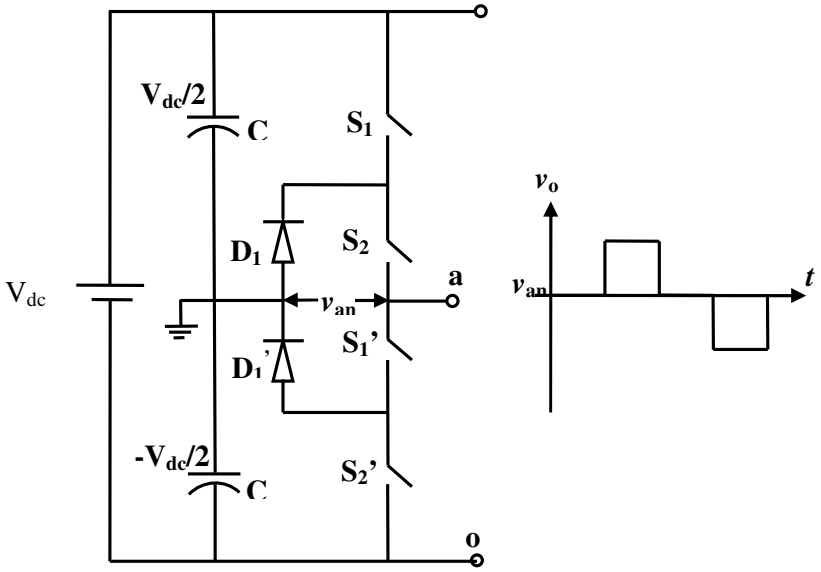


Fig. 2.2 Three level diode clamped inverter

The key components that distinguish this circuit from a conventional two-level inverter are diodes D_1 and D_1'. These two diodes clamp the switch voltage to half the level of the DC-bus voltage. When both switches S_1 and S_2 turn on the voltage across '*a*' and 'o' is V_{dc} i.e. $V_{ao}=V_{dc}$. In this case D_1' balances the voltage sharing between S_1'and S_2' with S_1' blocking the voltage across C_1 and S_2' blocking the voltage across C_2. Note that output voltage v_{an} is ac and V_{ao} is DC. The difference between v_{an} and V_{ao} is the voltage across C_2 which is $V_{dc}/2$. If the output is between '*a*' and 'o', then the circuit becomes a DC/DC inverter which has three output voltage levels: V_{dc}, $V_{dc}/2$ and 0.

Fig. 2.3 shows a five-level diode-clamped inverter in which the DC bus consists of four capacitors C_1, C_2, C_3 and C_4. For DC-bus voltage V the voltage across each capacitor is $V_{dc}/4$ and each device voltage stress will be limited to one capacitor voltage level i.e. $V_{dc}/4$ through clamping diodes.

To explain how the staircase voltage is obtained the neutral point '*n*' is considered as the output phase voltage reference point. There are five switch combinations to obtain five level voltages across '*a*' and '*n*'.

For voltage level $v_{an}=V_{dc}/2$ turn on all upper switches S_1–S_4. For voltage level $v_{an}=0$, turn on two upper switches S_3 and S_4 and two lower switches S_1' and S_2'. For voltage level $v_{an}=-V_{dc}/4$ turn on one upper switch s4 and three lower switches S_1'–S_3'. Similarly it can be explained for other voltage levels. Four complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the four complementary pairs are (S_1, S_1'), (S_2, S_2'), (S_3,S_3'), and (S_4,S_4').

Although each active switching device is only required to block a voltage level of V_{dc}/ (m-1), the clamping diodes must have different voltage ratings for reverse voltage blocking. Using D_1' of Fig. 2.3 as an example when lower devices S_2'-S_4'are turned on, D_1' needs to block three capacitor voltages or $3V_{dc}/4$. Similarly D_2 and D_2' need to block $2V_{dc}/4$, and D_3 needs to block $3V_{dc}/4$. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m-1)x(m-2). This number represents a quadratic increase in m. When m is sufficiently high the number of diodes required will make the system impractical to implement. If the inverter runs under PWM the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications [10].

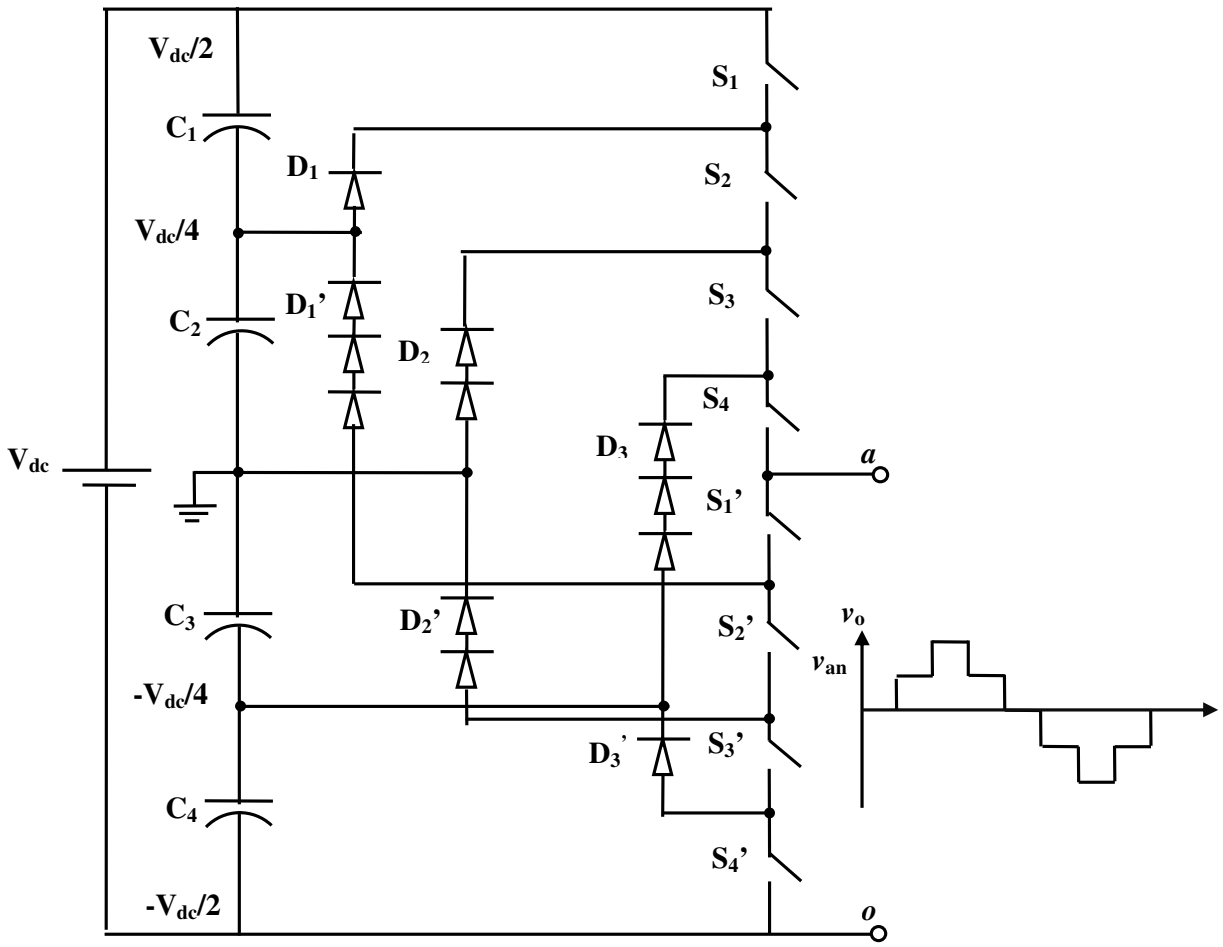


Fig. 2.3 Five level diode clamped inverter

Table 2.1 Switching combination for five level DCMLI

SWITCHING STATES								Output Voltage
S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	
ON	ON	ON	ON	OFF	OFF	OFF	OFF	$V_{dc}/2$
OFF	ON	ON	ON	ON	OFF	OFF	OFF	$V_{dc}/4$
OFF	OFF	ON	ON	ON	ON	OFF	OFF	0
OFF	OFF	ON	ON	ON	ON	ON	OFF	$-V_{dc}/4$
OFF	OFF	OFF	OFF	ON	ON	ON	ON	$-V_{dc}/2$

2.3 FLYING CAPACITOR MULTILEVEL INVERTER

Fig.2.4 illustrates the fundamental building block of single phase-leg capacitor-clamped inverter. The circuit has been called the flying capacitor inverter [11], [16], [40] with independent capacitors clamping the device voltage to one capacitor voltage level. The inverter in Fig. 2.4 provides a three-level output across *a* and *n*, i.e. v_{an} =$V_{dc}/2$, 0 or –$V_{dc}/2$. For voltage level $V_{dc}/2$ switches S_1 and S_2 need to be turned on for –$V_{dc}/2$ switches S_1'and S_2' need to be turned on and for the 0 level either pair (S_1,S_1') or

(S_2,S_2') needs to be turned on. Clamping capacitor C_1 is charged when S_1 and S_2' are turned on and is discharged when S_2 and S_1' are turned on. The charge of C_1 can be balanced by proper selection of the 0-level switch combination.

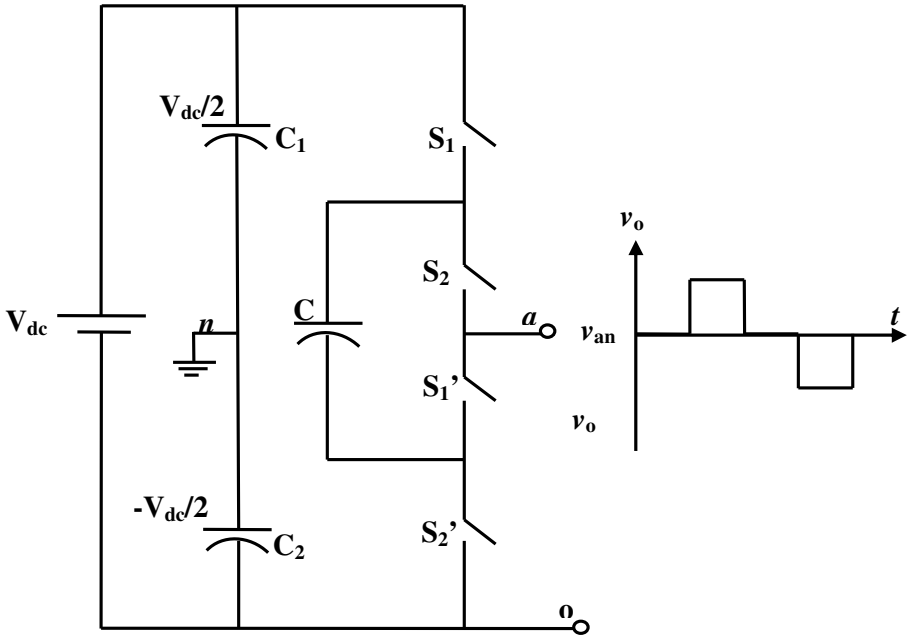


Fig. 2.4 Three level flying capacitor multilevel inverter

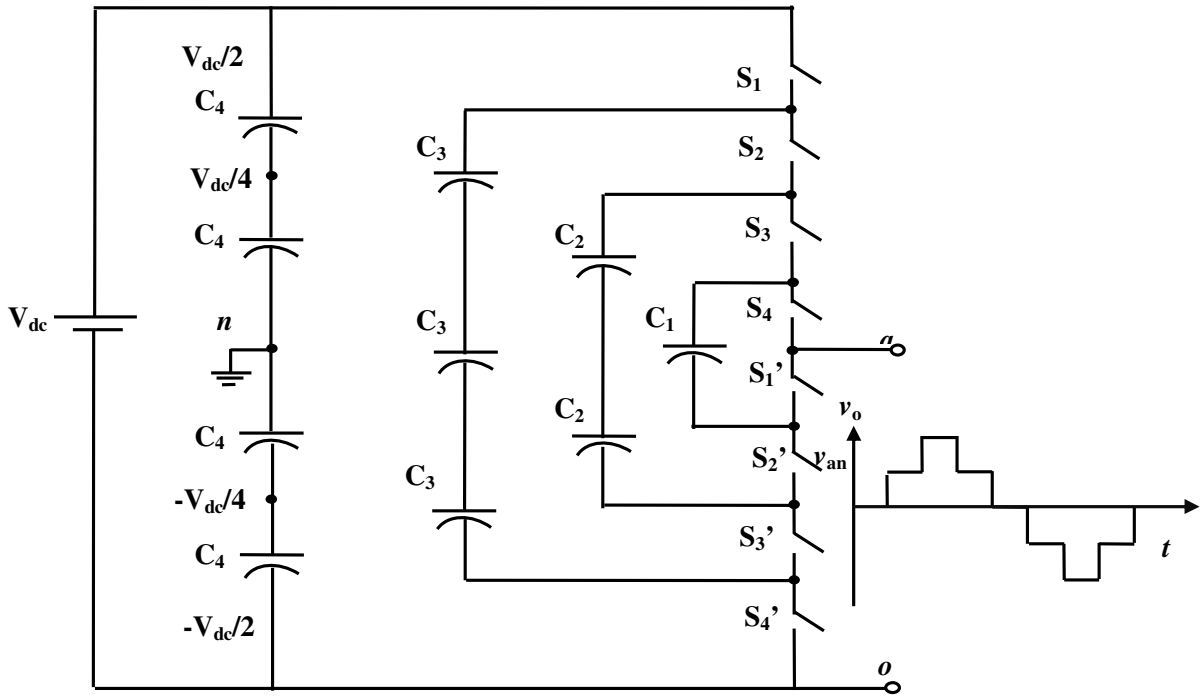


Fig. 2.5 Five level flying capacitor multilevel inverter

The voltage synthesis in a five-level capacitor-clamped inverter has more flexibility than a diode-clamped inverter. Using Fig. 2.5 as an example the voltage of the five-level phase-leg '*a*' output with respect to the neutral point '*n*', v_{an} can be obtained by following switching combinations.

Table 2.2 Switching combination for five level FCMLI

SWITCHING STATES								Output Voltage
S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'	
ON	ON	ON	ON	OFF	OFF	OFF	OFF	$V_{dc}/2$
ON	ON	ON	OFF	ON	OFF	OFF	OFF	$V_{dc}/4$
OFF	ON	ON	ON	OFF	OFF	OFF	ON	$V_{dc}/4$
ON	OFF	ON	ON	OFF	OFF	ON	OFF	$V_{dc}/4$
ON	ON	OFF	OFF	ON	ON	OFF	OFF	0
OFF	OFF	ON	ON	OFF	OFF	ON	ON	0
ON	OFF	ON	OFF	ON	OFF	ON	OFF	0
ON	OFF	OFF	ON	OFF	ON	ON	OFF	0
OFF	ON	OFF	ON	OFF	ON	OFF	ON	0
OFF	ON	ON	OFF	ON	OFF	OFF	ON	0
ON	ON	OFF	OFF	OFF	ON	ON	OFF	$-V_{dc}/4$
OFF	OFF	OFF	ON	OFF	ON	ON	ON	$-V_{dc}/4$
OFF	OFF	ON	OFF	ON	OFF	ON	ON	$-V_{dc}/4$
OFF	OFF	OFF	OFF	ON	ON	ON	ON	$-V_{dc}/2$

For voltage level $v_{an} = V_{dc}/2$, turn on all upper switches S_1– S_4. For voltage level $v_{an} = 0$, there are six combinations as shown in Table 2.2. For voltage level $v_{an} = -V_{dc}/4$ there are three combinations: S_1,S_1',S_2',S_3'($v_{an} = V_{dc}/2$ of upper C_4's $-3V_{dc}/4$ of C_3's), S_4,S_2',S_3',S_4'($v_{an} = V_{dc}/4$ of C_1 – $V_{dc}/2$ of C_4's) and S_3,S_1',S_3', S_4'($v_{an} = V_{dc}/2$ of C_2's – $V_{dc}/4$ of C_1 – $V_{dc}/2$ of lower C_4's). Other output voltage combinations are given in Table 2.2.

In the preceding description the capacitors with positive signs are in discharging mode while those with negative sign are in charging mode. By proper selection of capacitor combinations it is possible to balance the capacitor charge. Similar to diode clamping the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an m-level inverter will require a total of (m-1)x(m-2)/2 clamping capacitors per phase leg in addition to (m-1) main DC-bus capacitors.

2.4 CASCADED MULTILEVEL INVERTERS

Inverter topology based on the series connection of single-phase inverters with separate DC sources [41] is explained here. As stated above, the general function of the multilevel inverter is to synthesize a desired voltage from several separate DC sources

(SDCSs) such as solar cells, fuel cells, ultra capacitors, etc. Fig. 2.6 shows the power circuit for one phase leg of a five-level inverter with two cells in each phase (one cell refers to single phase H Bridge).

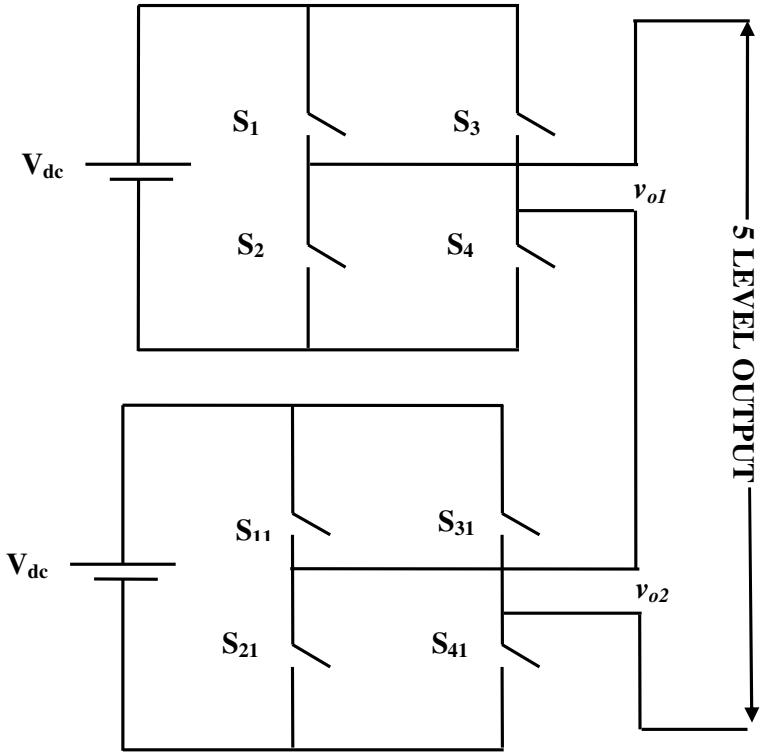


Fig. 2.6 Five level cascaded multilevel inverter

Table 2.3 Switching combination for five level CMLI

Switching State						Output Voltage v_{an}
S_{11}	S_{31}	S_{12}	S_{32}	V_{H1}	V_{H2}	
1	0	1	0	V_{dc}	V_{dc}	$2V_{dc}$
1	0	1	1	V_{dc}	0	V_{dc}
1	0	0	0	V_{dc}	0	V_{dc}
1	1	1	0	0	V_{dc}	V_{dc}
0	0	1	0	0	V_{dc}	V_{dc}
0	0	0	0	0	0	0
0	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	1	1	0	0	0
1	0	0	1	V_{dc}	$-V_{dc}$	0
0	1	1	0	$-V_{dc}$	V_{dc}	0
0	1	1	1	$-V_{dc}$	0	$-V_{dc}$
0	1	1	0	$-V_{dc}$	0	$-V_{dc}$
1	1	1	1	0	$-V_{dc}$	$-V_{dc}$
0	0	0	1	0	$-V_{dc}$	$-V_{dc}$
0	1	0	1	$-V_{dc}$	$-V_{dc}$	$-2V_{dc}$

The resulting phase voltage is obtained by the addition of the voltages generated by the different cells.Each single-phase full-bridge inverter generates three voltages at the output: V_{dc}, 0 and $-V_{dc}$ this is accomplished by different combinations of the four switches in each cell as explained in Table 2.3. The ac output of each full-bridge inverter is connected in series such that the synthesized voltage waveform is the sum of all of the individual inverter outputs. The number of output phase (line-neutral) voltage levels in a cascade multilevel inverter is given by 2N+1, where N is the number of DC sources. The CHB inverter explained above can be extended to any number of voltage levels.

2.5 FEATURES OF MULTILEVEL INVERTER

Thus features of a multilevel inverter can be summarized as follows:

Output Waveform Quality: Multilevel inverters can generate the output voltages with very low distortion and reduced *dv*/*dt* stresses can be achieved therefore electromagnetic compatibility (EMC) problems can be minimized. Hence output waveform quality is improved.

Common-Mode (CM) Voltage: Multilevel inverters produce smaller CM voltage therefore the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore CM voltage can be eliminated by using advanced modulation strategies such as that proposed in [13]. Thus common mode voltage is reduced.

Input Current Distortion: Multilevel inverters can draw input current with low distortion.

Switching Frequency: Multilevel inverters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

High Voltage Capacity: Multilevel inverter structure can be utilized in high and medium voltage applications.

Low THD and *dv*/*dt*: The output waveform voltages is composed of voltage levels greater than three which leads to lower THD and dv/dt in comparison to the two-level inverter operating at the same voltage rating and device switching frequency.

Multilevel inverters do have some disadvantages. One particular disadvantage is the greater number of power semiconductor switches needed. Although lower voltage rated switches can be utilized in a multilevel inverter each switch requires a related gate drive circuit. This may cause the overall system to be more expensive and complex. Also the capacitor banks or insulated sources needed to achieve the voltage steps on the DC

busses.

2.6 HYBRID MULTILEVEL INVERTER

Hybrid multilevel inverter gives multi level operation by using hybrid source, hybrid configuration or hybrid device in such a way to produce output with reduced number of DC sources, high speed capability, low output switching frequency, low switching loss, high conversion efficiency, flexibility to enhance and various topologies for different applications.

Broadly HMLI can be classified as per power circuit configuration and modulation technique used.

2.7 CLASSIFICATION OF HYBRID MULTILEVEL INVERTER

Hybrid multilevel inverters are classified on basis of types of power devices used, number of power supplies used, magnitude of the power supplies used and how power devices are connected in circuit. Thus broad classification of hybrid multilevel inverter is as follows:

- ***Asymmetric Hybrid Multilevel Inverter***
- ***Hybrid Multilevel Inverter Based on Half-Bridge Modules***
- ***New Symmetrical Hybrid Multilevel Inverters***
- ***Hybrid Clamped Five-Level Inverter Topology***
- ***Distinct Series Connected cells Hybrid Multilevel Inverter***
- ***Hybrid Medium-Voltage Inverter based on a NPC Inverter***
- ***New Hybrid Asymmetrical Multilevel H-bridge Inverter***
- ***Hybrid Multilevel Inverter with Single DC Source***

2.7.1 ASYMMETRIC HYBRID MULTILEVEL INVERTER [1,2]

In previous description of cascaded multilevel inverter the DC voltages of each cell are equal. However it is possible to have different voltage levels among the cells [42], [43] and such circuit is called as asymmetric hybrid multilevel inverter. Fig. 2.7 shows an example of two separate DC-bus levels one with low voltage switches and the other with high voltage switches. Switches S_1- S_4 are low voltage switches like IGBT and switches S_{11}- S_{41} are high voltage switches like GTO. With unequal DC voltages the number of voltage levels can be increased without necessarily increasing the number of H-bridge cells in cascade. This allows more voltage steps in the inverter output voltage waveform for a given number of power cells [42, 44].

[1]Hina B. Chandwani and Meeta K. Matnani "A review of hybrid multilevel inverter configurations and their comparison" is published Elixirjournal Elixir Power Elec. Engg, May 2012, pp. 8483-8486.

[2] Hina B. Chandwani and Meeta K. Matnani, "A review and comparative study of hybrid multilevel inverter configuration" is published Elixirjournal Elixir Power Elec. Engg July 2012, pp. 9690-9692

Depending on the availability of DC sources the voltage levels are not limited to a specific ratio. This feature allows more levels to be created in the output voltage and thus reduces the harmonic contents with less cascaded cells.

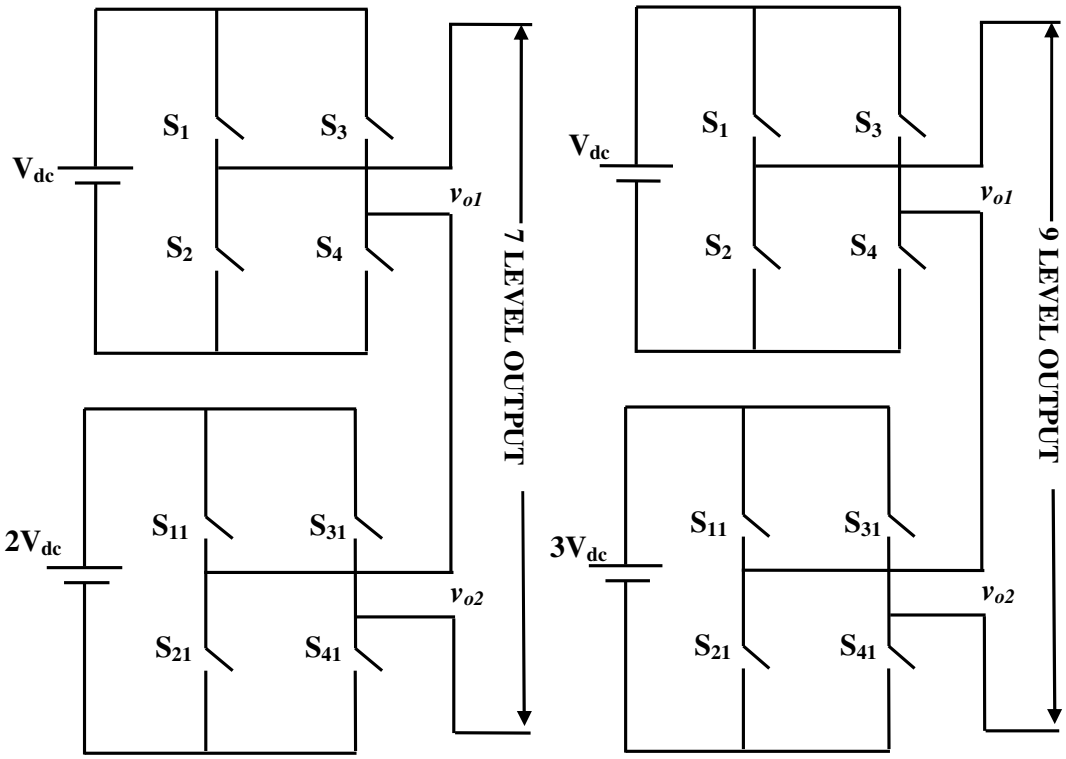


Fig. 2.7 Asymmetric hybrid multilevel inverter (a) seven level (b) nine level

Fig. 2.7 shows two inverter topologies, where the DC voltages for the H bridge cells are not equal. In the seven-level topology the DC voltages for H bridge1 and H bridge2 are V_{dc} and $2V_{dc}$ respectively. The two-cell inverter leg is able to produce seven voltage levels: $3V_{dc}$, $2V_{dc}$, V_{dc}, 0, $-V_{dc}$, $-2V_{dc}$, and $-3V_{dc}$. The relationship between the voltage levels and their corresponding switching states is summarized in Table 2.3. In the nine-level topology, the DC voltage of H bridge2 is three times that of H bridge1. All the nine voltage levels can be obtained by replacing the H bridge2 output voltage of $v_{o2} = \pm 2\ V_{dc}$ in Table 2.4 with $v_{o2} = \pm 3\ V_{dc}$ and then calculating the inverter phase voltage.

There are some drawbacks associated with the CHB inverter using unequal DC voltages. The merits of the modular structure are essentially lost. In addition, switching pattern design becomes much more difficult due to the reduction in redundant switching states [44] Therefore, this inverter topology has limited industrial applications. Even with the same voltage level among them, it is also possible to use high-frequency PWM for

one cell, while the other switches at a lower rate. Fig. 2.7 shows an example with two different devices. The top full-bridge cell uses the insulated gate bipolar transistor (IGBT), and the low cell uses the gate-turn-off thyristor (GTO) as its switching device. The GTO-based cell switches at a lower frequency, typically the fundamental frequency, and the IGBT-based cell switches at a PWM frequency to smooth the waveform [42], [43].

Table 2.4 Switching states for AHMLI

Switching State				Output Voltage		
S_1	S_3	S_{11}	S_{31}	v_{o1}	v_{o2}	$v_o = v_{o1} + v_{o2}$
1	0	1	0	V_{dc}	$2\ V_{dc}$	$3\ V_{dc}$
1	1	1	0	0	$2\ V_{dc}$	$2\ V_{dc}$
0	0	1	0	0	$2\ V_{dc}$	
1	0	1	1	V_{dc}	0	V_{dc}
1	0	0	0	V_{dc}	0	
0	1	1	0	$-V_{dc}$	$2\ V_{dc}$	
0	0	0	0	0	0	0
0	0	1	1	0	0	
1	1	0	0	0	0	
1	1	1	1	0	0	
1	0	0	1	V_{dc}	$-2\ V_{dc}$	$-V_{dc}$
0	1	1	1	$-V_{dc}$	0	
0	1	0	0	$-V_{dc}$	0	
1	1	0	1	0	$-2\ V_{dc}$	$-2\ V_{dc}$
0	0	0	1	0	$-2\ V_{dc}$	
0	1	0	1	$-V_{dc}$	$-2\ V_{dc}$	$-3\ V_{dc}$

2.7.2 HYBRID MULTILEVEL INVERTER BASED ON HALF-BRIDGE MODULES

Cascaded half-bridge inverters [45]–[49] employ half-bridge modules connected in series instead of the H Bridges. These inverters are one of the alternatives to the conventional cascaded H Bridge inverters. The modular multilevel inverter [45]–[48] employ series connections of pairs of half-bridge modules. These modules are connected in delta forming a three phase system and the capacitors of DC links do not need isolated DC supplies [45], [46] since the voltage across each half-bridge module DC link capacitor can be actively controlled. The hybrid cascaded half-bridge inverter [49] uses an alternative connection of half-bridge modules to eliminate the output DC level. The three phase system is reached through a Y connection. The modules are also connected in pairs and the inverter is able to provide just odd levels in the output phase voltages. This type of inverter requires a higher number of insulated DC sources for the same

number of levels of a CHB. However, lower active power levels are processed in the DC sources.

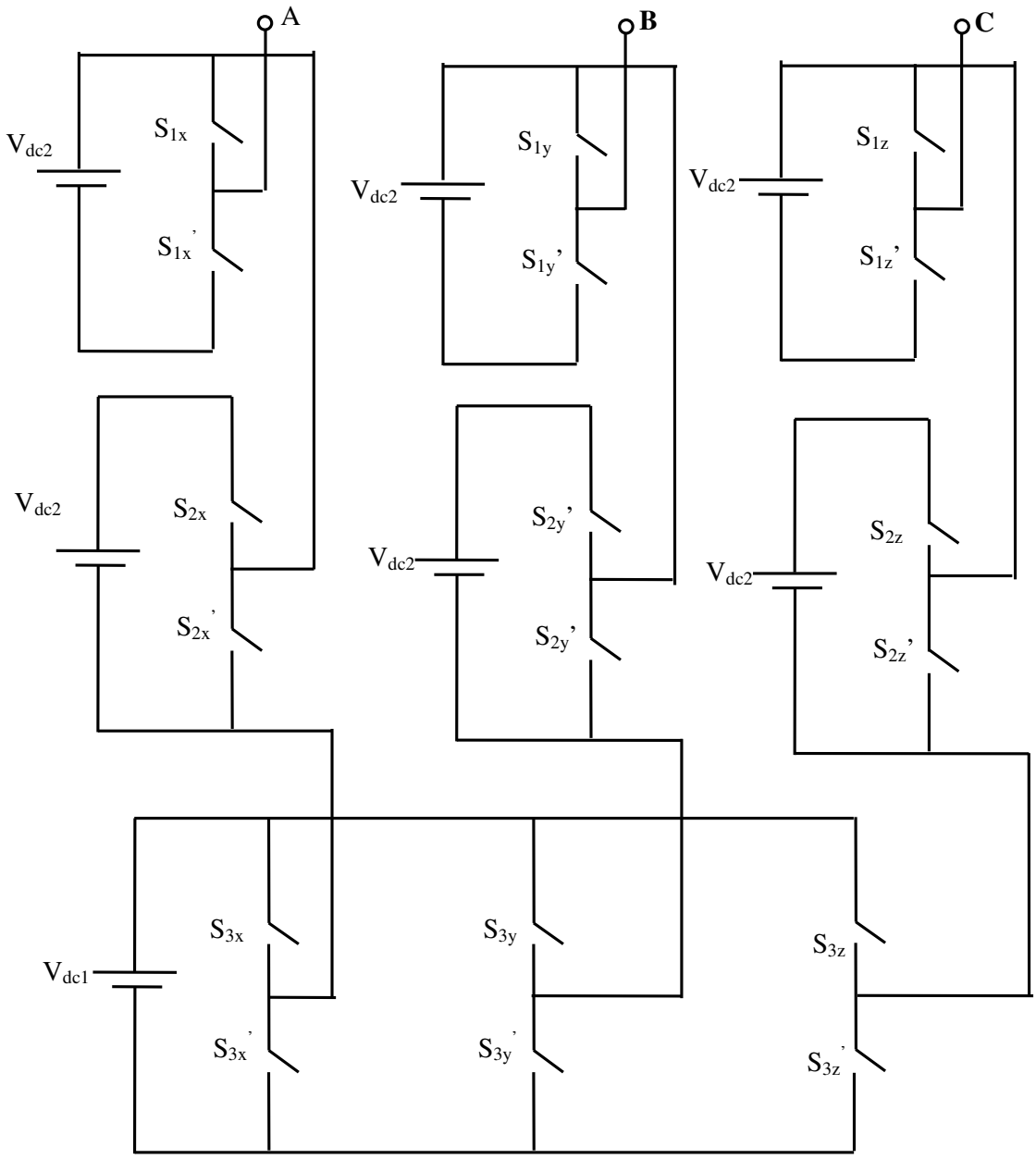


Fig. 2.8 Hybrid multilevel inverter based on half-bridge modules

This hybrid cascaded half-bridge inverter makes use of a three-phase inverter shown as a VSI in Fig. 2.8 where each output is series connected to a pair or multiple pairs (cascade) of half-bridge inverters connected with inverse polarity as shown in Fig. 2.8. Here the special connection of the half-bridge modules [49] guarantees that no DC level is observed at the output voltages. In the symmetrical version the modularity is preserved. Even though the number of insulated sources is increased for the same number of voltage

levels as for the CHB or HCHB this inverter lowers the ratings of these devices since the average current that is drawn from each 6-pulse rectifier feeding a half-bridge module is lower when compared to an H-bridge based inverter. Thus, higher power levels can be achieved for a given transformer/rectifier circuit. The assumptions made for the analysis of circuit are: (i) the switching devices are ideal (ii) the DC sources are constant positive voltages (iii) parasitics are neglected (iv) the virtual center point of the VSI´s DC-link drawn in Fig. 2.8 is assumed as reference for the voltages.

It is observed that the output voltage v_A can assume six different values, which are given for v_o, with o = x;y;z, in Table 2.5. These output voltage levels depend on the DC sources voltages V_{dc2} and V_{dc1} and on the states of switches Sjo and Sjo0 , with j = 1; 2; 3. Based on these results, the hybrid cascaded half-bridge inverter can be operated with a number of levels N_{level} varying from four to six given that

$N_{level} = 4$; if $V_{dc2} = V_{dc1}$

$N_{level} = 5$; if $V_{dc2} = V_{dc1}/2$

$N_{level} = 6$; if $V_{dc1} \neq V_{dc2} \neq V_{dc1}/2$

Table 2.5 Resulting output phase voltage

S_{1o}	S_{2o}	S_{3o}	v_o	Case 1 $V_{dc2}=V_{dc1}=V_{dc}$	Case 2 $V_{dc2}=V_{dc1}/2=V_{dc}$	Case 3 $V_{dc2}=V_{dc1}/3=V_{dc}$
0	0	0	$-V_{dc2}-V_{dc1}/2$	$-3V_{dc}/2$	$-2V_{dc}$	$-5V_{dc}/2$
1	0	0	$-V_{dc1}/2$	$-V_{dc}/2$	$-V_{dc}$	$-3V_{dc}/2$
0	1	0	$-V_{dc1}/2$	$-V_{dc}/2$	$-V_{dc}$	$-3V_{dc}/2$
1	1	0	$V_{dc2}-V_{dc1}/2$	$+V_{dc}/2$	0	$-V_{dc}/2$
0	0	1	$-V_{dc2}+V_{dc1}/2$	$-V_{dc}/2$	0	$+V_{dc}/2$
1	0	1	$+V_{dc1}/2$	$+V_{dc}/2$	$+V_{dc}$	$+3V_{dc}/2$
0	1	1	$+V_{dc1}/2$	$+V_{dc}/2$	$+V_{dc}$	$+3V_{dc}/2$
1	1	1	$+V_{dc2}+V_{dc1}/2$	$+3V_{dc}/2$	$+2V_{dc}$	$+5V_{dc}/2$

2.7.3 NEW SYMMETRICAL HYBRID MULTILEVEL INVERTERS

With a proper driving pattern for switches $S_1 – S_4$, and for the switches of the H-Bridge, it is possible to obtain a voltage waveform between the points a-b as shown in Fig. 2.10. Then the circuit of Fig. 2.9 behaves as a five-level output voltage single-phase inverter. The single leg switches block voltages of value ´ V_{dc}´ and with proper modulation strategy they operate at high frequency (a few kHz). On the other hand, the H-bridge switches S_5, S_6, S_7 and S_8 must block a higher voltage level of '$2V_{dc}$'. However, these switches operate only in a semi cycle of the output voltage. Thus, they operate at low frequency commutating at zero voltage. Thus this inverter can also be classified among the hybrid multilevel inverters group.

As shown in [11] and [28], the multilevel inverters based on the H-bridge symmetrical cascade have a number of levels in its output voltage given by 2N+1. For circuit shown in Fig. 2.9 output voltage levels are also obtained through the same expression 2N+1 levels where N is the number of DC sources.

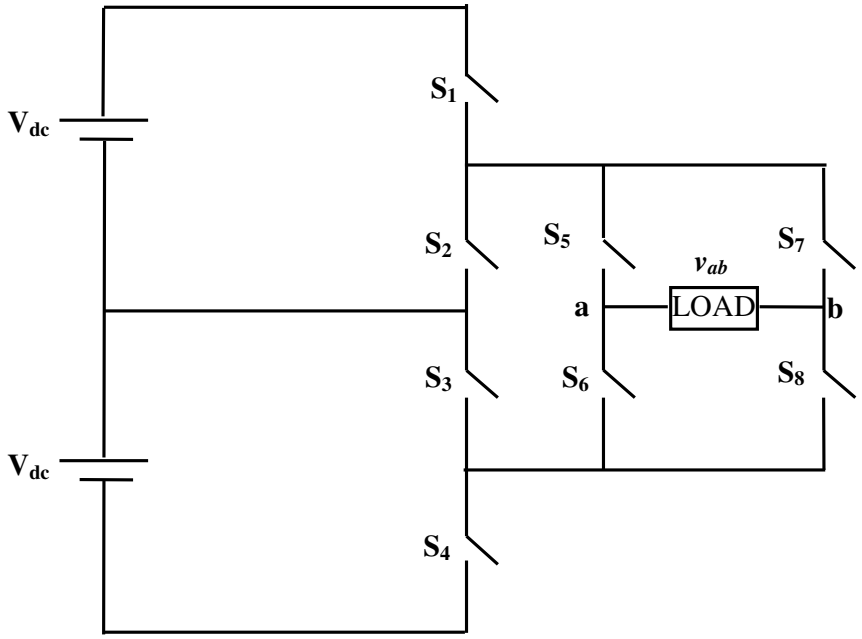


Fig. 2.9 New symmetrical hybrid multilevel inverter

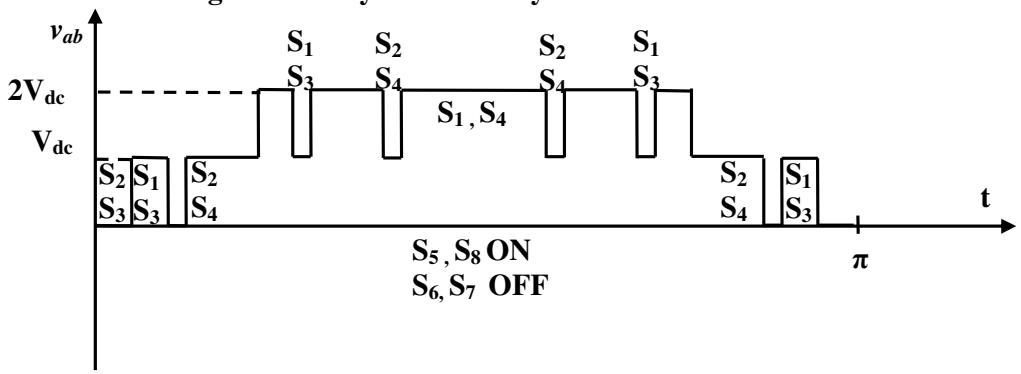


Fig. 2.10 Output voltage waveform for new symmetrical hybrid multilevel inverter

This can be implemented with the configuration shown in Fig. 2.9 where switches S_5 to S_8 are connected as a full-bridge inverter that is responsible for switching the load terminals according to the gate's signals. Fig. 2.10 shows the possible load voltage v_{ab} for the specified switching conditions. It is seen that the pairs S_5/S_8 and S_6/S_7 are turned on complementarily in order to generate, respectively, negative and positive voltages. The three-level DC–DC inverter switches S_1 to S_4 are switched according to a proper modulation pattern in order to generate a desired load voltage. Therefore, the inverter shown in Fig. 2.9 is a five-level single-phase inverter where switches S_1 to S_4

operate at high frequency and are rated for half of the DC-link voltage *E*. Switches S_5 to S_8 are rated for the full DC-link voltage $2V_{dc}$. On the other hand, switches S_5 to S_8 can be implemented with low-frequency devices such as GTOs, integrated gate commutated thyristors (IGCT), and others, since they switch a single time per load-voltage period under zero voltage. Based on this strategy, the proposed inverter is a symmetric (equal DC sources) hybrid (multiple carrier frequencies) multilevel inverter. Furthermore, the number of levels can be increased by cascading multiple single-phase inverters. This can be achieved with other topologies as well. As shown in [11] and [28], the total number of level across the load terminals v_{ab} for the mentioned topology is given by $v_{ab} = 2N + 1$ where *N* is the total number of DC sources

2.7.4 HYBRID CLAMPED FIVE-LEVEL INVERTER TOPOLOGY

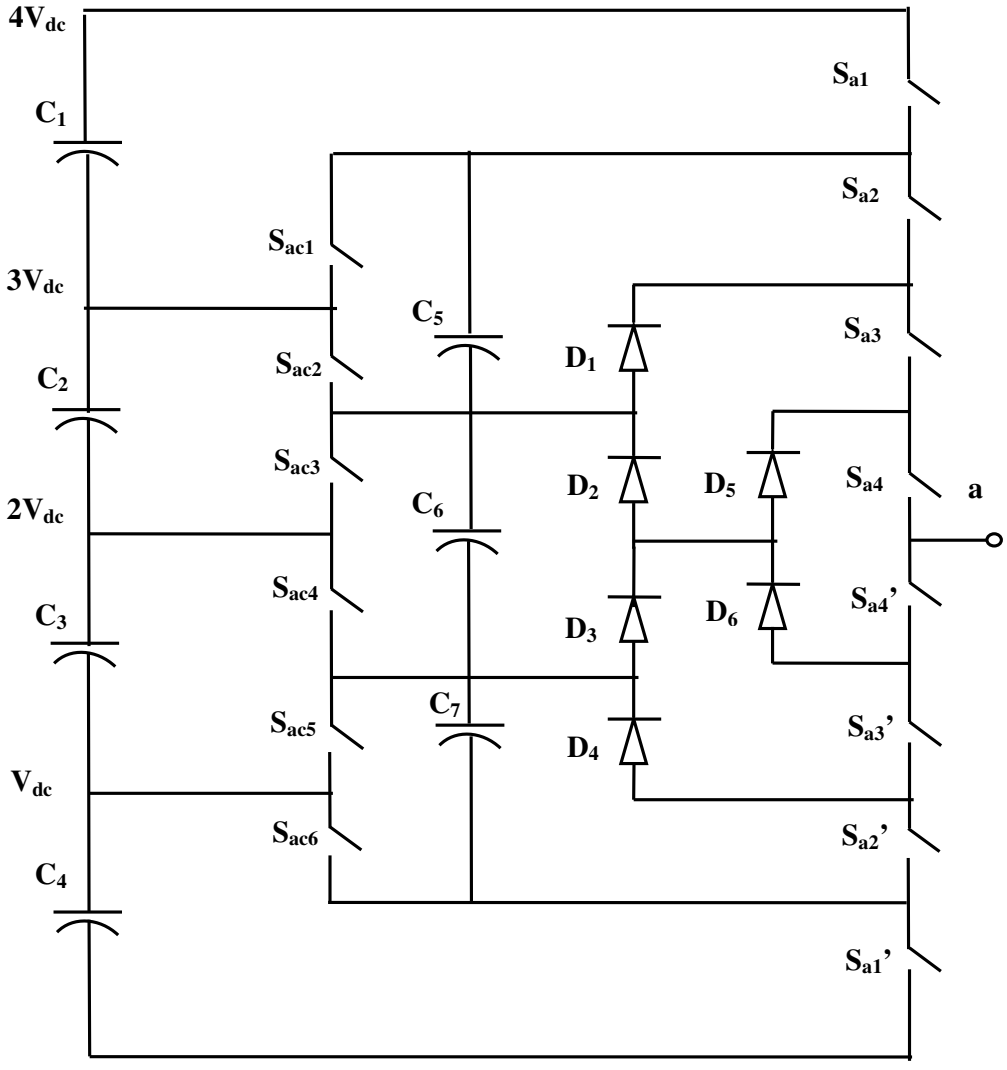


Fig. 2.11 Hybrid clamped five level inverter

A hybrid clamped multilevel inverter topology with self voltage balancing is discussed in

[50]. Fig. 2.11 shows one leg of the five-level topology. The main switching devices S_{a1}, S_{a2}, S_{a3} and S_{a4} are complementary with S_{a1}', S_{a4}', S_{a3}' and S_{a2}' respectively and S_{a1} is complementary with S_{ac1}.

Among the clamping switching devices S_{ac1} - S_{ac6} the adjacent switching devices are complementary. Self-voltage balancing in capacitors is realized by switching from one kind of device switching mode combination to another by turns.

Switching states are shown in Table 2.6 while Table 2.7 lists all the switching modes conversions for a hybrid clamped five-level inverter topology. From Table 2.7 it can be seen that there are two cases of switching modes conversions: (1) Switching modes conversions with the different output levels (2) Switching modes conversions with the same output levels. V_{dc} is equal to the voltage of one capacitor.

Table 2.6 Switching mode combinations

SWITCHING STATES				Output Voltage
S_1	S_2	S_3	S_4	
ON	ON	ON	ON	$2V_{dc}$
OFF	ON	ON	ON	V_{dc}
ON	OFF	ON	ON	V_{dc}
ON	OFF	OFF	ON	0
OFF	OFF	ON	ON	0
ON	ON	OFF	OFF	$-V_{dc}$
OFF	OFF	OFF	ON	$-V_{dc}$
OFF	OFF	OFF	OFF	$-2V_{dc}$

Table 2.7 Switching modes conversions for a hybrid clamped five-level inverter

Switching modes conversions	**Output level conversions**	**Switching modes conversions**	**Output level conversions**
1111→0111	$2V_{dc} \rightarrow V_{dc}$	1001→0011	$0 \rightarrow 0$
1111→1011	$2V_{dc} \rightarrow V_{dc}$	0011→0001	$0 \rightarrow -V_{dc}$
0111→1111	$V_{dc} \rightarrow 2V_{dc}$	1001→1000	$0 \rightarrow -V_{dc}$
1011→1111	$V_{dc} \rightarrow 2V_{dc}$	0001→0011	$-V_{dc} \rightarrow 0$
0111→1011	$V_{dc} \rightarrow V_{dc}$	1000→1001	$-V_{dc} \rightarrow 0$
1011→0111	$V_{dc} \rightarrow V_{dc}$	0001→1000	$-V_{dc} \rightarrow -V_{dc}$
0111→0011	$V_{dc} \rightarrow 0$	1000→0001	$-V_{dc} \rightarrow -V_{dc}$
1011→1001	$V_{dc} \rightarrow 0$	0001→0000	$-V_{dc} \rightarrow -2V_{dc}$
0011→0111	$0 \rightarrow V_{dc}$	1000→0000	$-V_{dc} \rightarrow -2V_{dc}$
1001→1011	$0 \rightarrow V_{dc}$	0000→0001	$-2V_{dc} \rightarrow -V_{dc}$
0011→1001	$0 \rightarrow 0$	0000→1000	$-2V_{dc} \rightarrow -V_{dc}$

2.7.5 DISTINCT SERIES CONNECTED CELLS HYBRID MULTILEVEL INVERTER

In distinct series connected hybrid multilevel inverters two, three and five-level

cells connected in series as shown in Fig. 2.12[51]

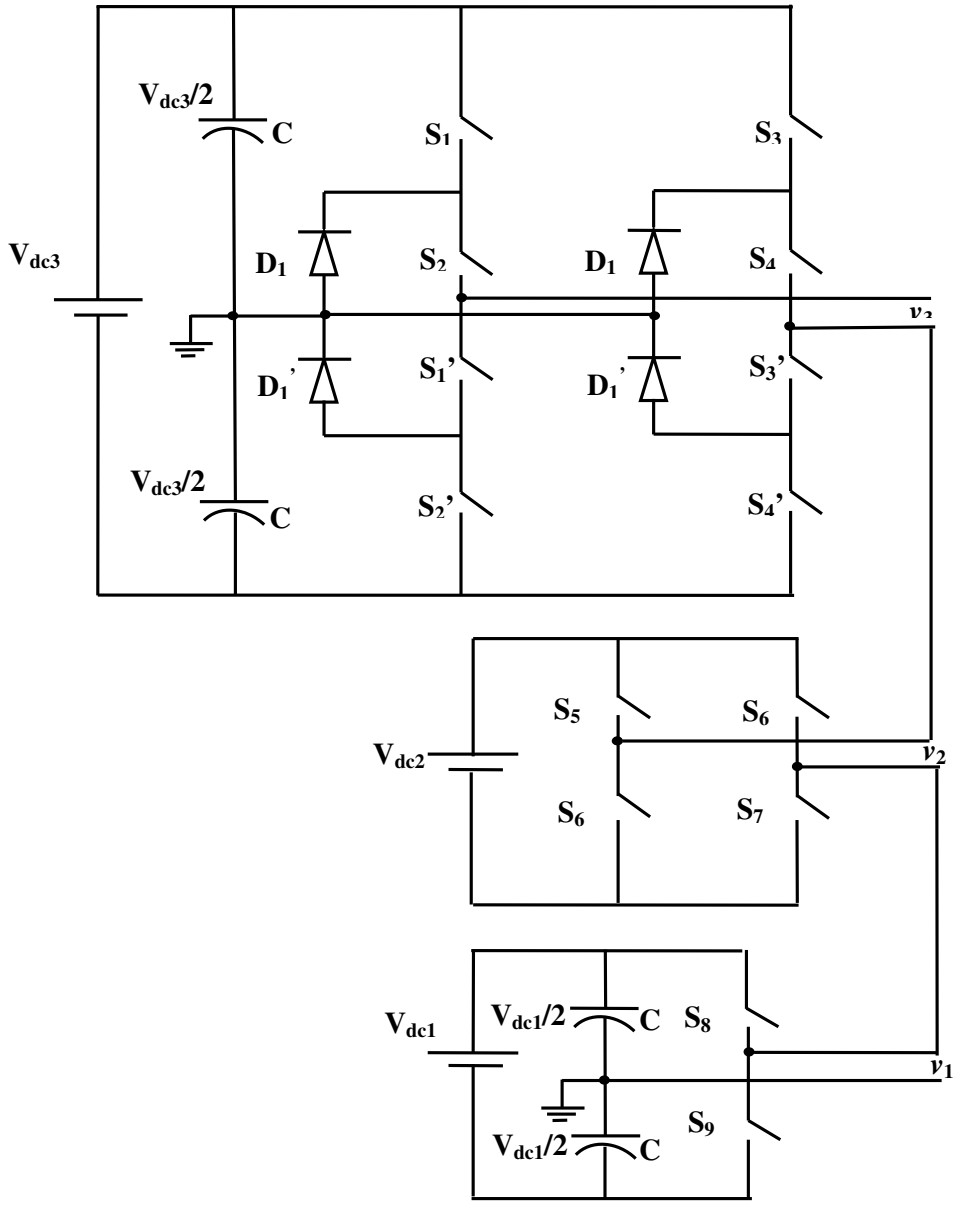


Fig. 2.12 Distinct series connected cells hybrid multilevel inverter

The first cell synthesizes two levels with 1-p.u. voltage step, the second cell generates three levels also with 1-p.u. voltage step and the third cell synthesizes five levels with 3-p.u. voltage steps. The switching devices of the two-level cell operate at high frequency, while the switches that compose the five-level cell operate at fundamental frequency. As v_1, v_2, and v_3 satisfy equation, the phase-voltage waveform with 16 levels is modulated at high frequency among any adjacent levels.

$$v_j \leq \sum_{k=1}^{j-1} (m_{k-1}) V_k$$

This example demonstrates the wide variety of arrangements that can be adopted to obtain a given number of levels. Thus it is essential to develop a design methodology to define the main parameters of a hybrid inverter such as the number of series-connected cells DC voltage levels and topologies used in each cell.

2.7.6 MEDIUM-VOLTAGE HYBRID MULTILEVEL INVERTER BASED ON A NPC INVERTER

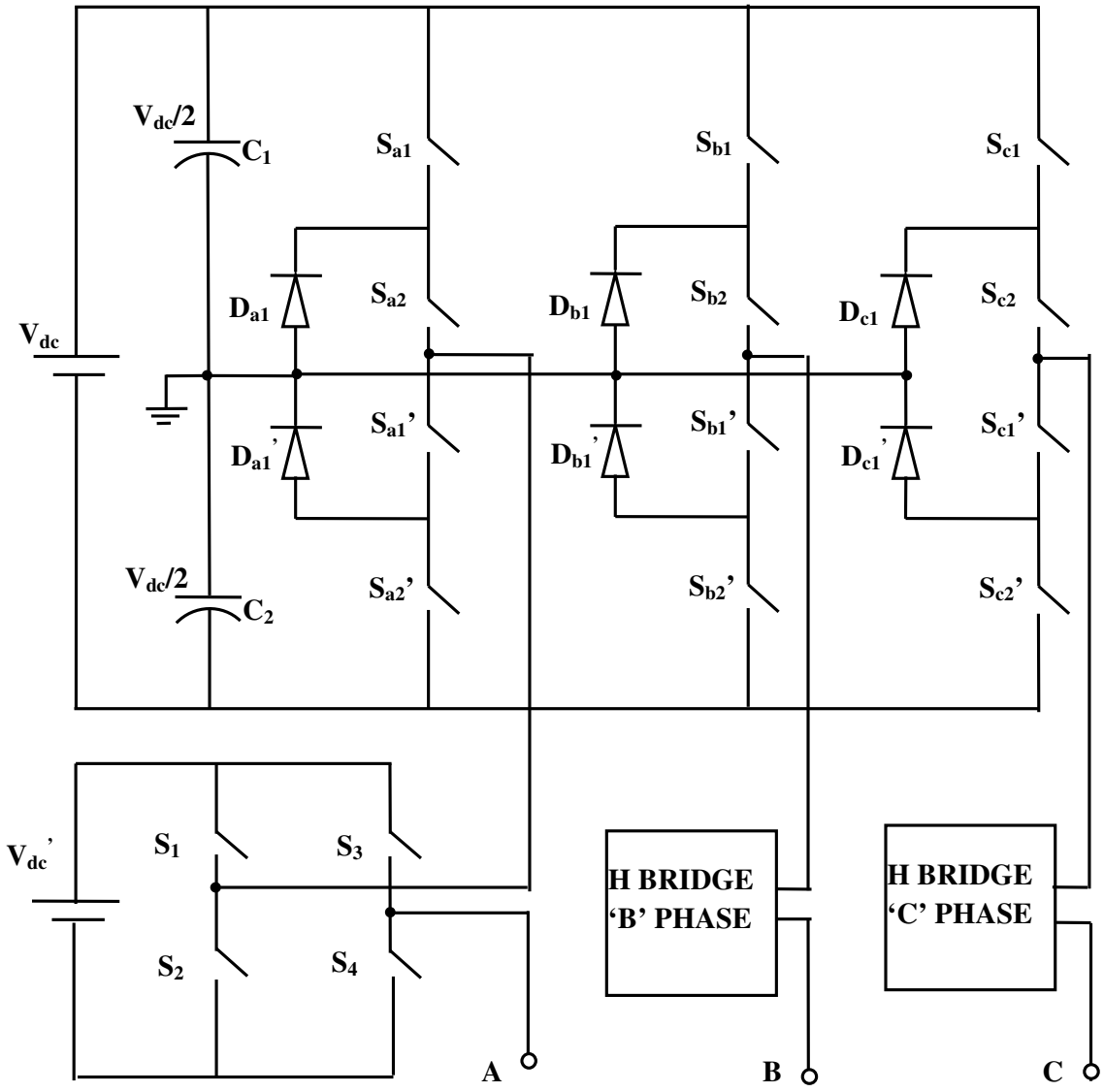


Fig. 2.13 Hybrid medium voltage inverter based on NPC inverter

This hybrid topology is composed of a traditional three-phase three-level NPC inverter and single phase H bridge inverter in series with each output phase [52]–[54].

The power circuit is illustrated in Fig.2.13 with only the H bridge of phase *a* shown in detail. As shown the DC source for the NPC inverter is provided by two series connected diode bridge rectifiers arranged in a 12-pulse configuration.

The H bridge DC links are not connected to an external DC power supply but they consist only of floating capacitors kept at a constant voltage by the control strategy. In this hybrid topology the NPC inverter provides the total active power flow. For a high-power medium-voltage NPC, there are advantages to using latching devices, such as integrated gate-commutated thyristors (IGCTs), rather than insulated-gate bipolar transistors (IGBTs) due to their lower losses and higher voltage blocking capability [52], [54], [55] imposing a restriction on the switching frequency. In contrast the H bridges are rated at a lower voltage and need to be commutated at a higher frequency for an effective active filtering effect. This calls for the use of the IGBT.

The first interpretation is as a single hybrid multilevel inverter with a nine-level phase voltage, achieved by the cascade connection of a three-level NPC leg and an HB per phase. The second interpretation is as an NPC inverter with a series active filter that compensates for the harmonic content introduced by the low switching NPC stage. If the NPC bridge is to be modulated at a low switching frequency the second interpretation would seem to be more appropriate in devising a control algorithm, leading to the following two design challenges: 1) To determine the lowest value of the HB DC-link voltage V_{dc} that achieves adequate voltage harmonic compensation. 2) To devise a control algorithm that ensures that the floating DC links are properly regulated at this value.

2.7.7 HYBRID MULTILEVEL INVERTER BASED ON MAIN INVERTER AND CONDITIONING INVERTER

With minor changes in hybrid medium-voltage inverter based on a NPC inverter, hybrid multilevel inverter based on main inverter and conditioning inverter is obtained. Modifications done are shown in Fig. 2.14 the conditioning inverter is supplied by ultra capacitors as the DC source. The main and the conditioning inverters are in series. The output voltage of the main inverter is denoted v_1 and the output voltage of the conditioning inverter is denoted v_2 so the output voltage of the hybrid multilevel inverter is $v_o = v_1+v_2$

To explain the analysis of this circuit only one H bridge power cell is considered in each phase which means N=1 in Fig. 2.14, so the main inverter can be considered as a 3- level inverter. Its output voltage v_1 can be $+V_{dc}'$, 0 and $-V_{dc}'$.

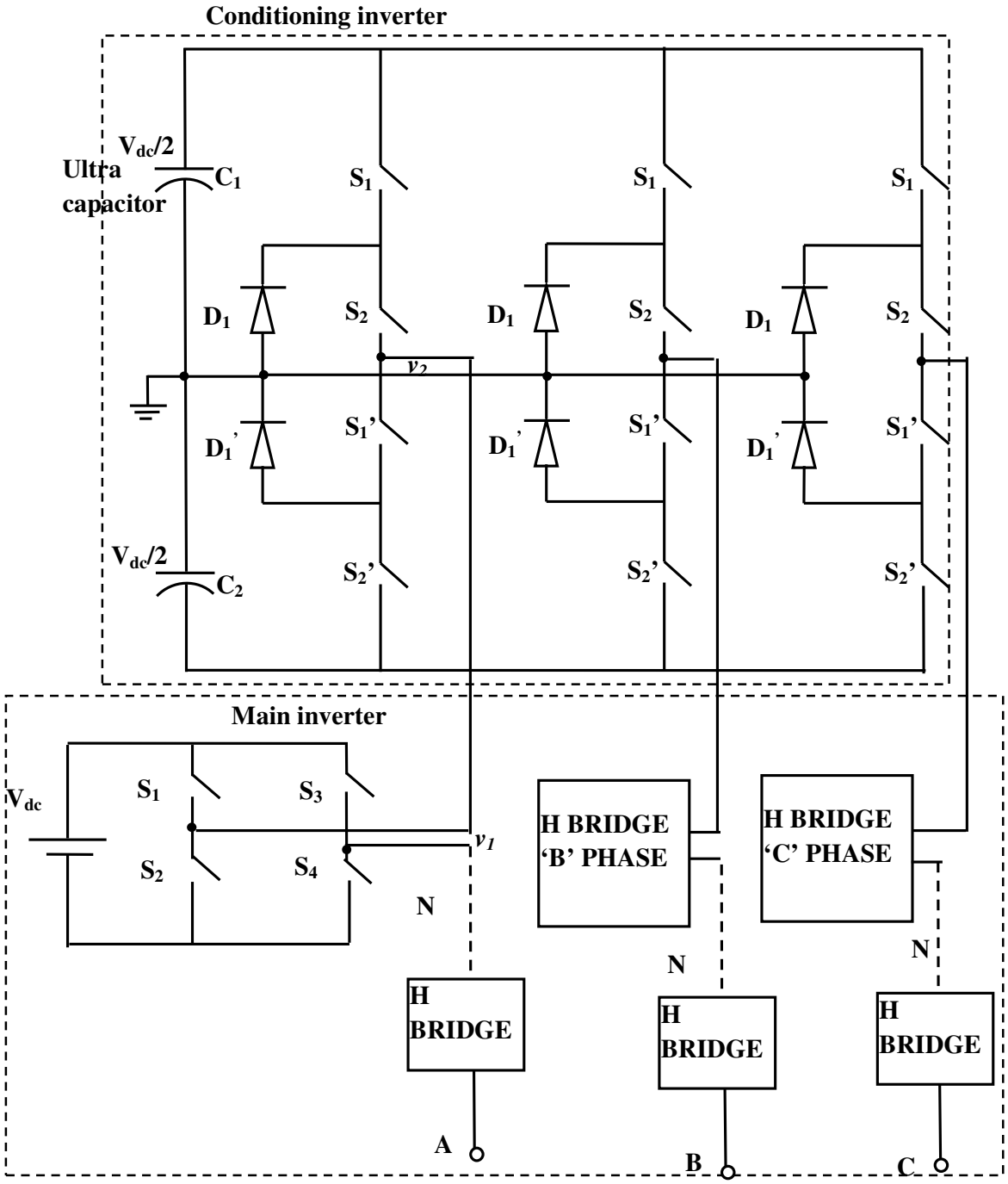


Fig. 2.14 Hybrid multilevel inverter based on main inverter and conditioning inverter

For the NPC conditioning inverter two ultra capacitors are in series and connected to the DC-link. If the DC voltage is considered as V_{dc}', and the two ultra capacitors are the same i.e.V_1= -V_2= V_{dc}/2. So the conditioning inverter output voltage v_c can be + V_{dc}/2, 0 and -V_{dc}/2. Therefore the inverter output voltage v_o can be -(V_{dc}'+V_{dc}/2), -V_{dc}',-(V_{dc}'-V_{dc}/2), -V_{dc}/2, 0, V_{dc}/2, (V_{dc}'-V_{dc}/2), V_{dc}' and (V_{dc}'+ V_{dc}/2) 9 possible output levels. When the ratio of V_{dc}':V_{dc}/2=1, the inverter can output 5 voltage

levels. When V_{dc}': $V_{dc}/2=3$, the inverter can output 9 voltage levels, which is called the maximal distension in the reference [56],[57].

This hybrid inverter is based on the traditional H-bridge topology incorporated with the conditioning inverter, thus some advantages can be obtained: 1) The conditioning inverter can be used as an energy storage device, which can store and reuse the braking energy of the motor. As a result, it improves the inverter efficiency. 2) The three-level NPC inverter can generate three different voltages, as the H-bridge cells do. So one H-bridge cell of each phase can be reduced by the conditioning inverter. This leads to a simplification of the feeding transformer. 3) The conditioning inverter can be considered as a SVC, which can deliver reactive power and improve the power factors of the system. 4) The conditioning inverter can be used to redundantly provide instantaneous energy when the main inverter cell is broken.

2.7.8 NEW HYBRID ASYMMETRICAL MULTILEVEL H-BRIDGE INVERTER

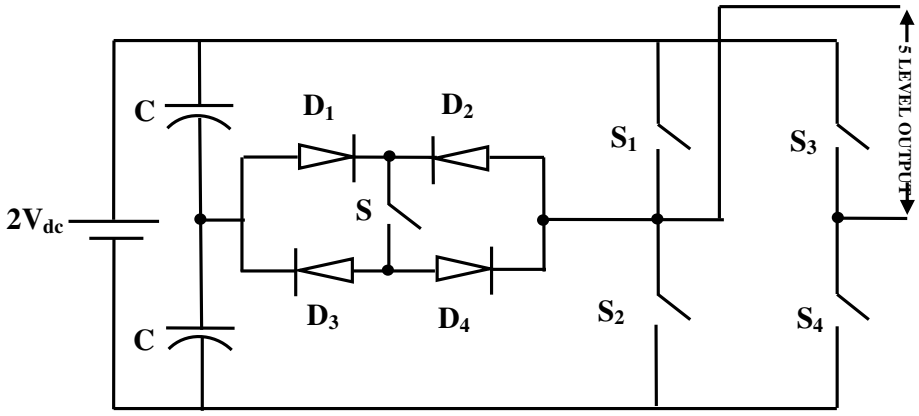


Fig. 2.15 New hybrid asymmetrical H-bridge multilevel inverter

Following the principle of increasing the number of output waveform voltage levels with less switching devices inverter topology is shown in Fig. 2.15. The new H-bridge topology with an auxiliary bidirectional switch can output maximum five level voltage waveform ($2V_{dc}$, V_{dc}, 0, $-2V_{dc,}$ $2V_{dc}$). The switching combinations required to generate the five-level output waveform is as given in Table 2.8. In this configuration the two capacitors in the capacitive voltage divider are connected directly across the DC bus and since all switching combinations are activated in an output cycle the dynamic voltage balance between the two capacitors is automatically restored[55,58].

Table 2.8 Switching combinations for five level output voltage

S	S_1	S_2	S_3	S_4	Output Voltage
OFF	ON	OFF	OFF	ON	2 V_{dc}
ON	OFF	OFF	OFF	ON	V_{dc}
OFF	OFF	ON	OFF	ON	0
ON	OFF	OFF	ON	OFF	- V_{dc}
OFF	OFF	OFF	ON	OFF	-2 V_{dc}

2.7.9 HYBRID MULTILEVEL INVERTER WITH SINGLE DC SOURCE

This inverter includes a standard full bridge 3-leg inverter (one leg for each phase) and an H-bridge in series with each inverter leg as shown in Fig. 2.16.

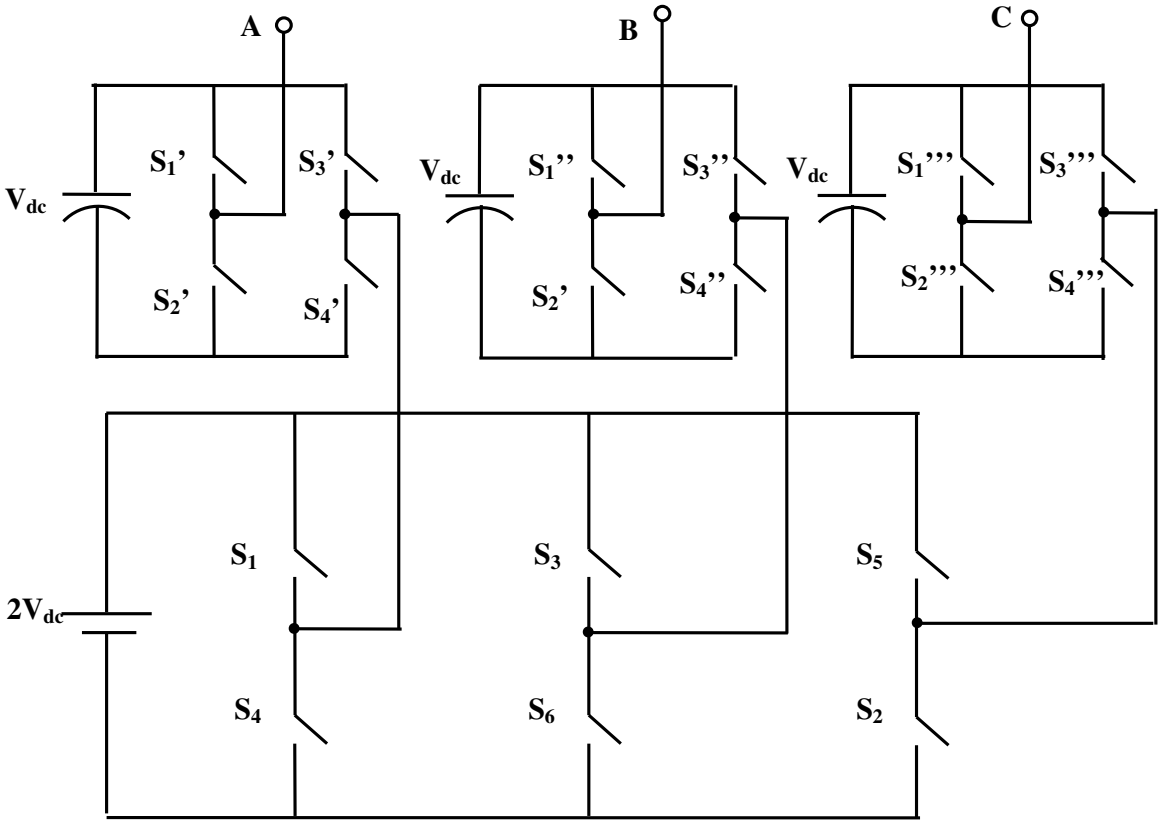


Fig. 2.16 Three phase hybrid multilevel inverter with single DC source

It uses only a single DC power source to supply a standard 3-leg inverter along with three full H-bridges supplied by capacitors or batteries. Traditionally, each H-bridge requires a DC power source [11,12,59-63]. The inverter can be used in electric vehicles (EV) / hybrid electric vehicles (HEV) to drive electric motor. And it can be applied for utility interface. As shown in Fig. 2.17 the output voltage v_1 of single leg (with respect to the ground) is either $+V_{dc}$ (S_5 closed) or $-V_{dc}$ (S_6 closed). This leg is connected in series

with a full H-bridge which in turn is supplied by a capacitor voltage. If the capacitor is used and kept charged to V_{dc}, then the output voltage of the H-bridge can take on the values + V_{dc} (S_1, S_4 closed), 0 (S_1, S_2 closed or S_3, S_4 closed), or – V_{dc} (S_2, S_3 closed).

Fig. 2.18 shows an output voltage example. The capacitor's voltage regulation control method consists of monitoring the output current and the capacitor voltage so that during periods of zero voltage output either the switches S_1, S_4, and S_6 are closed or the switches S_2, S_3, S5 are closed depending on whether it is necessary to charge or discharge the capacitor. This method depends on the voltage and current not being in phase. That means one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently the amount of capacitor voltage the scheme can regulate depends on the phase angle difference of output voltage and current [64-68].

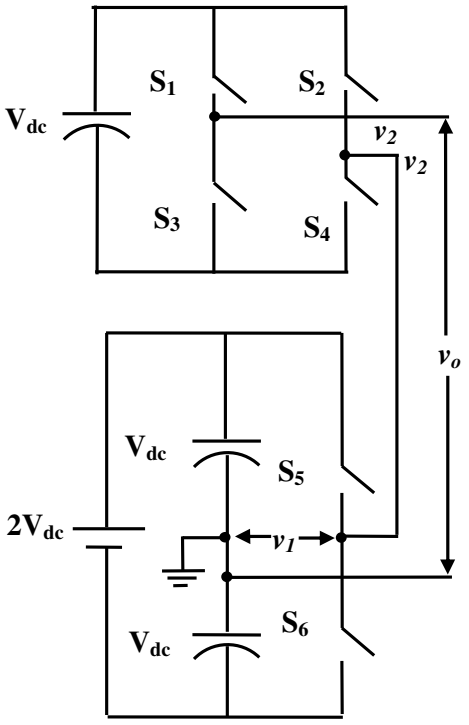


Fig. 2.17 Single phase hybrid multilevel inverter with single DC source

When the output voltage $v = v_1+v_2$ is required to be zero, one can either set v_1= + V_{dc} and v_2 = – V_{dc} or v_1 = + V_{dc} and v_2 = + V_{dc}. It is this flexibility in choosing how to make that output voltage zero that is exploited to regulate the capacitor voltage. During $\theta 1 \leq \theta \leq \pi$, the output voltage in Fig. 2.19 is zero and the current i > 0. If S_1 and S_4 are closed (so that v_2 = + V_{dc}) along with S_6 closed (so that v_1 = – V_{dc}), then the capacitor is *discharging* (ic = –i < 0 see Fig. 2.18) and $v = v_1+v_2 = 0$. On the other hand, if S_2 and S_3

are closed (so that $v_2 = -V_{dc}$) and S_5 is also closed (so that $v_1 = +V_{dc}$), then the capacitor is *charging* (ic = i > 0 see Fig. 2.18) and $v = v_1+v_2 = 0$. The case i < 0 is accomplished by simply reversing the switch positions of i > 0 case for charge and discharge of the capacitor.

As Fig. 2.19 illustrates, this method of regulating the capacitor voltage depends on the voltage and current not being in phase. That is, one needs positive (or negative) current when the voltage is passing through zero in order to charge or discharge the capacitor. Consequently, the amount of capacitor voltage the scheme can regulate depends on the power factor. Thus by maintaining the regulation of the capacitor voltage simultaneously achieves an output voltage waveform which is 25% higher than that obtained using a standard 3-leg inverter by itself.

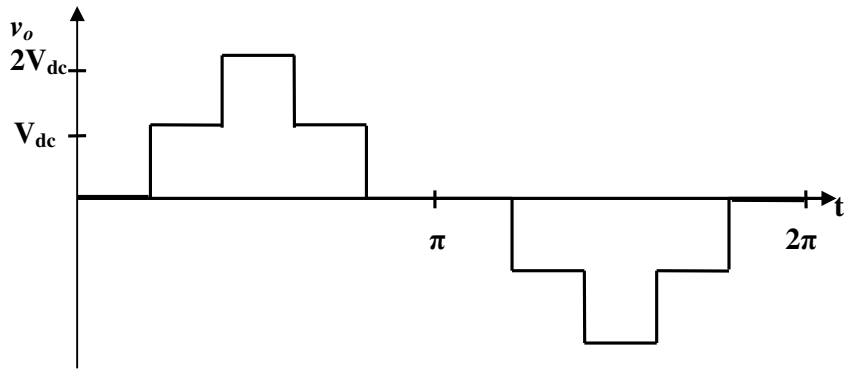


Fig. 2.18 Output voltage for single phase hybrid multilevel inverter with single DC source

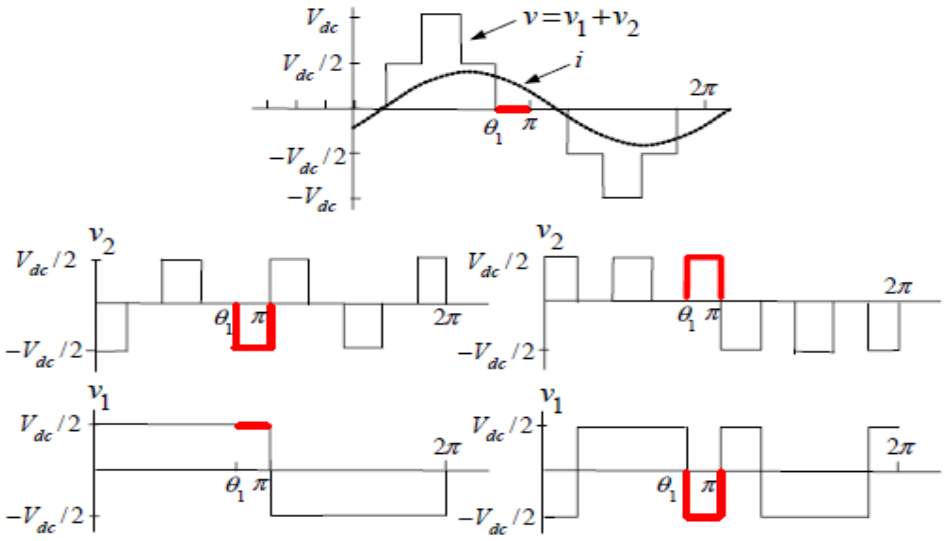


Fig. 2.19 Capacitor voltage regulation

2.8 SUMMARY

Thus comparative study for different multilevel inverters carried out in this research work is described and discussed. It can be concluded that every topology has its own advantages and disadvantages. Thus as per the application topology can be chosen and implemented. As asymmetrical multilevel inverters are alternative to minimize the harmonic distortion of the output voltages without increasing the number of power devices. The use of different DC voltage values naturally leads to hybrid multilevel topologies, which employ distinct types of semiconductors and modulation strategies, in an effort to optimize the power processing of the overall system. On the other hand, these features increase significantly the flexibility and complexity of hybrid multilevel inverter design. Distinct series connected cells hybrid multilevel inverter reduces the complexity for hybrid topology for distinct applications thus minimizing the number of switching devices and reducing the circulating energy among the series-connected cells. Compared with an H-bridge cascaded multilevel inverter, the number of overall insulated DC sources is reduced in the single phase hybrid symmetrical multilevel inverter while the number of semiconductors is kept the same. Thus, this concept appears as a useful and suitable solution for medium voltage applications where input-side insulation is required along with high efficiency and modularity. Furthermore, by reducing the number of insulated DC supplies, the number of cables connecting the input transformer terminals to the rectifying bridges is reduced.

New hybrid asymmetrical multilevel H-bridge inverter reduces the harmonic components of output voltage. Hybrid multilevel inverter based on main inverter and conditioning inverter topology is very suitable for the applications which need motors accelerating and braking frequently. The braking energy can be stored in the floating ultra capacitors of conditioning inverter to improve the efficiency and performance of the system. Hybrid multilevel inverter employing half-bridge modules and a three-phase inverter is able to provide better losses distribution among the power semiconductors and to limit the maximum device loss to a lower level when compared to a fully high frequency switched inverter. In this case devices are replaced with lower speed and lower forward voltage drop IGBTs for the four-level hybrid inverter which is able to achieve higher efficiency figures. In hybrid multilevel inverter with single DC source topology capacitor voltage balancing is of importance. This topology is generally used for HEV and EV applications, while hybrid clamped multilevel inverter reduces filter size.

CHAPTER 3

NOVEL MODULATION TECHNIQUES for MULTILEVEL INVERTER and HYBRID MULTILEVEL INVERTER

In different hybrid multilevel inverter topologies various modulation techniques can be applied. Every modulation technique has its own advantages and disadvantages. Depending on modulation index with respect to amplitude and frequency different modulation techniques can be studied.[1,2]

3.1 CLASSIFICATION OF DIFFERENT MODULATION TECHNIQUES

Various modulation techniques are as shown in block diagram:

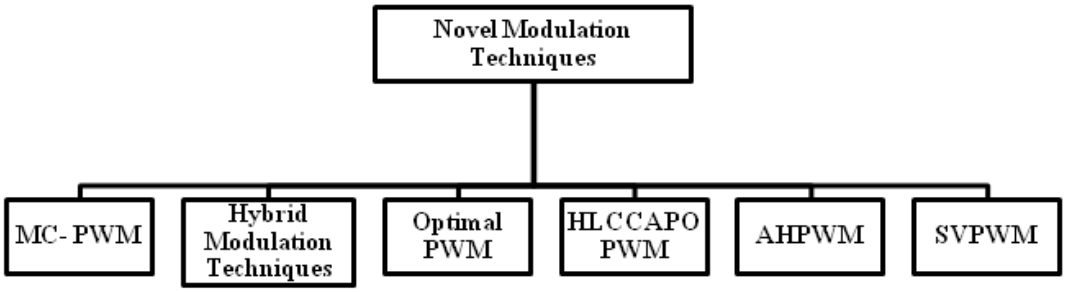


Fig. 3.1 Block diagram for novel modulation techniques

1. Multi carrier Pulse Width Modulation (MC-PWM).
2. Hybrid modulation techniques.
3. Synchronous pulse width modulation and higher frequency sub harmonic PWM
4. Higher and Lower Carrier Cells and Alternative Phase Opposition PWM (HLCCAPOPWM)
5. Alternative hybrid PWM (AHPWM).
6. Space vector PWM (SVPWM).

These modulation techniques can also be applied for other multilevel inverter configurations like diode clamped MLI, flying capacitor MLI and cascaded MLI. These modulation techniques are explained in general. Some modulation techniques are easily applicable to particular MLI but have to be modified for some other configurations. Modulation ratio plays an important role in all the techniques. Modulation can be over modulation or under modulation depending on modulation ratio and accordingly total harmonic distortion (THD) varies. While describing modulation techniques MLI topology, modulation ratio and THD are considered as major factors.

Following definitions are to be considered for further description:

- Amplitude Modulation ratio (m_a), defined as $m_a=A_m/A_c$, where A_m is the amplitude of the reference signal and Ac is the peak-to-peak amplitude of carrier signal. (For a N-level inverter, this ratio is defined as $m_a = A_m/(N-1)A_c$.

[1] Hina B. Chandwani and Meeta K. Matnani, "A review of modulation techniques for hybrid multilevel inverter" Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), December 2012, pp. 1-7.
[2]Hina B. Chandwani and Meeta K. Matnani ,"A Review of Multicarrier Modulation Techniques for Various Hybrid Multilevel Inverter" International Journal of Engineering Associates Volume 2 Issue 4, pp. 20-25.

- Frequency modulation ratio (m_f), defined as $m_f = f_c/f_r$, where f_r is the reference signal frequency and f_c is the carrier signal frequency.
- β angle that the relative phase displacement between the carrier and the reference signal and in this analysis it is assumed to be zero.

3.2 MULTI CARRIER PULSE WIDTH MODULATION

The following section describes different multicarrier PWM techniques. The multicarrier PWM can be broadly classified as shown in Fig. 3.2.

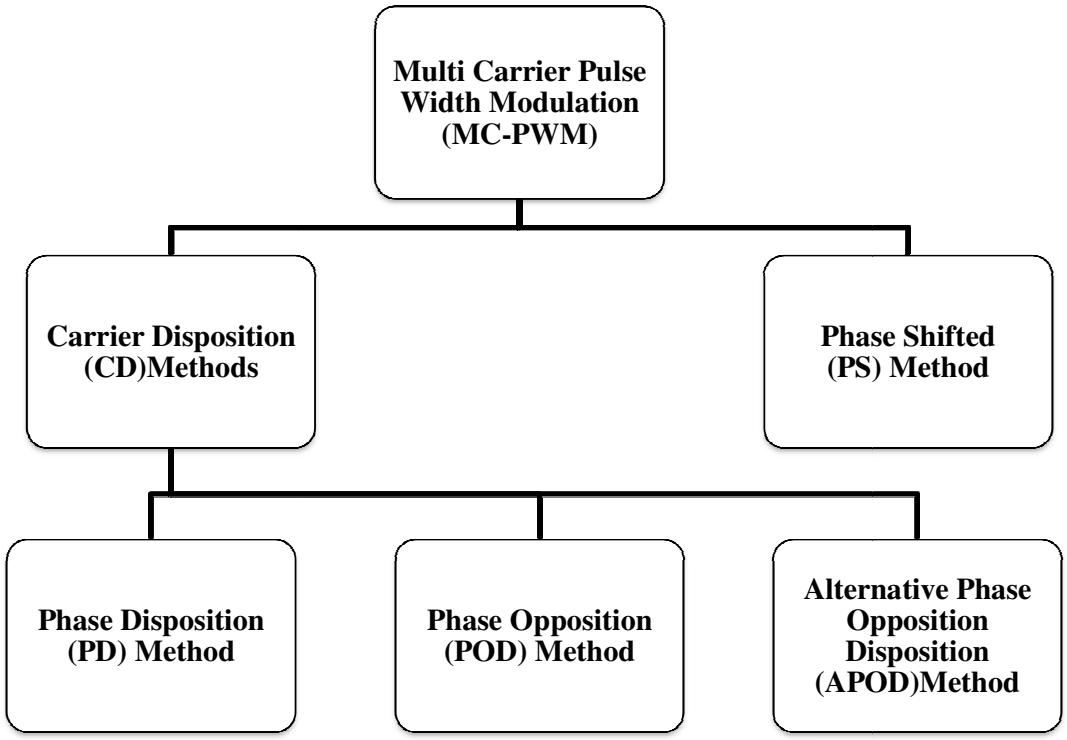


Fig. 3.2 Classification for multicarrier pulse width modulation

The multicarrier PWM technique uses several triangular carrier signals keeping only one modulating sinusoidal signal. For an n level inverter n-1 carriers are employed [1] – [2]. The carriers have the same frequency and same peak to peak amplitude but are disposed so that the bands they occupy are contiguous. The zero reference is placed in the middle of the carrier set. The modulating signal is a sinusoid of frequency 50 Hz. At every instant each carrier is compared with the modulating signal. Each comparison gives one if the modulating signal is greater than the triangular carrier, zero otherwise. The results are added to give the voltage level which is required at the output terminal of the inverter. Multicarrier PWM technique can be categorized into 2 groups. 1) Carrier disposition techniques (CD) where the reference waveform is sampled through a number of carrier waveforms displaced by contiguous increments of the reference waveform

amplitude. 2) Phase shifted PWM technique, where the multiple carriers are phase shifted accordingly [3].

3.2.1 CARRIER DISPOSITION TECHNIQUES (CD)

This carrier disposition can be classified into the following three techniques i) phase disposition technique ii) phase opposition technique and iii) alternative phase opposition disposition technique. These techniques are usually applied to the neutral point clamped topology [4] - [7]. These techniques may not be used for the H-Bridge inverter applications directly. But by using discontinuous PWM reference signals with phase-shifted carrier strategy may be implemented to apply PD technique to the H-Bridge inverter [8].

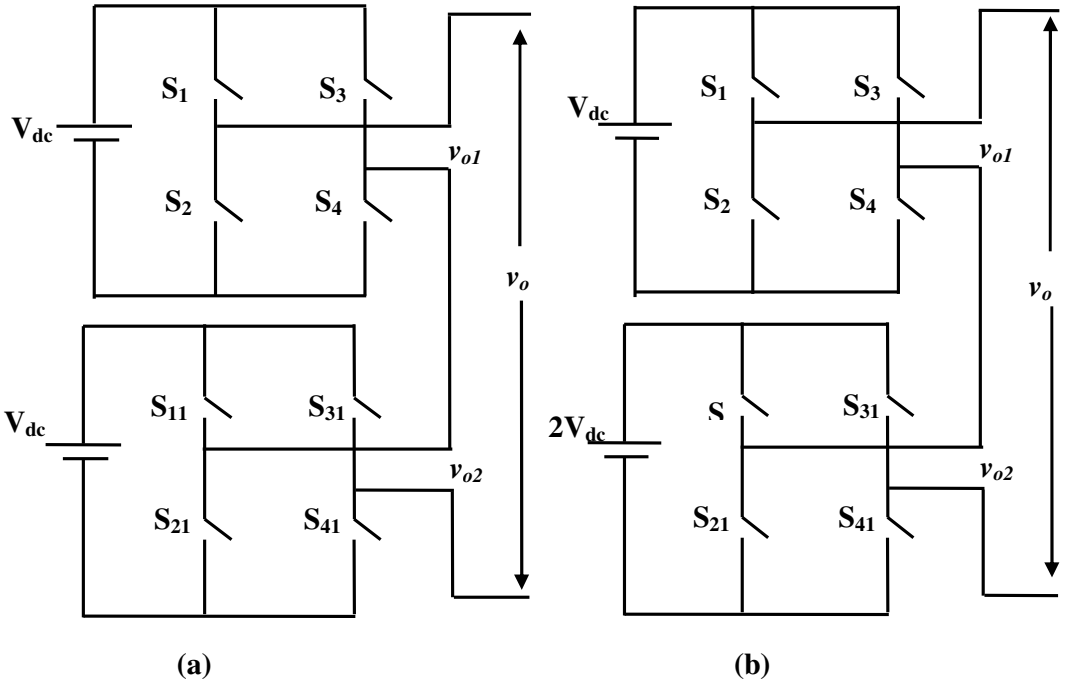


Fig. 3.3 Cascaded H-bridge inverter (a) symmetric five level (b)Asymmetric seven level

For description of the three modulation techniques mentioned a five level symmetric cascaded H-bridge inverter is considered as shown in Fig. 3.3(a). Also these modulation techniques can be applied to asymmetric multilevel inverter, diode clamped MLI, flying capacitor MLI and other hybrid MLI configurations.

3.2.2 PHASE DISPOSITION (PD) TECHNIQUE

The phase disposition technique has all carrier waveforms in phase with same frequency and amplitude, as shown in Fig. 3.4 (a). The zero reference is placed in the middle of the carrier sets. For this technique, significant harmonic energy is concentrated

at the carrier frequency [9]. The PD technique yields only odd harmonics for odd m_f and yields odd and even harmonics for even m_f (β =0) [10]. PD-PWM modulation can also be used in asymmetric multilevel topology [11] and as the number of voltage levels are increased the harmonic contents are decreased. Fig. 3.4 (b) shows output phase voltage for five level MLI using PD modulation technique.

For all simulation results on Y-axis voltage in volts is taken and on X-axis time is taken in seconds.

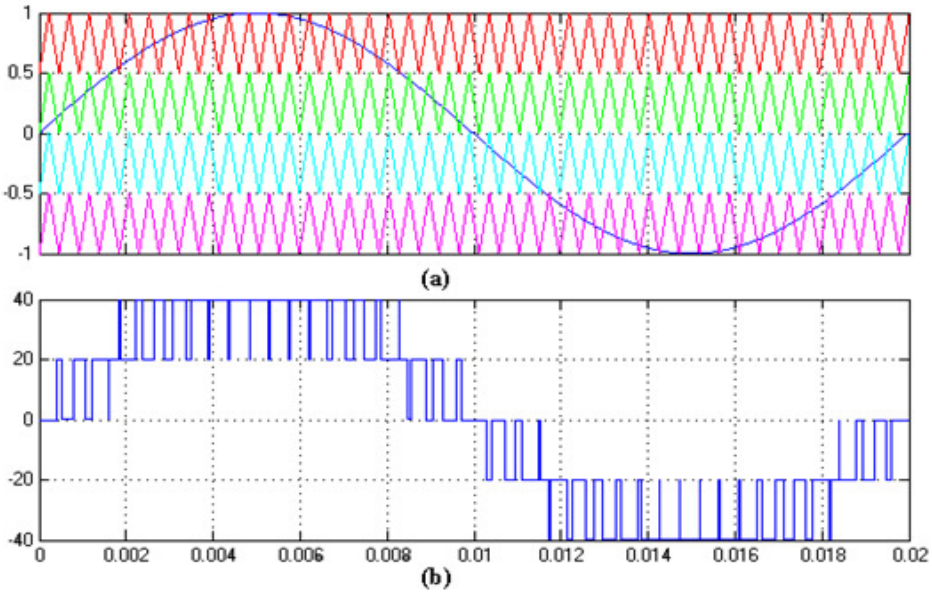


Fig. 3.4 (a) Phase Disposition technique (b) Five level inverter output voltage

3.2.3 PHASE OPPOSITION DISPOSITION (POD) TECHNIQUE

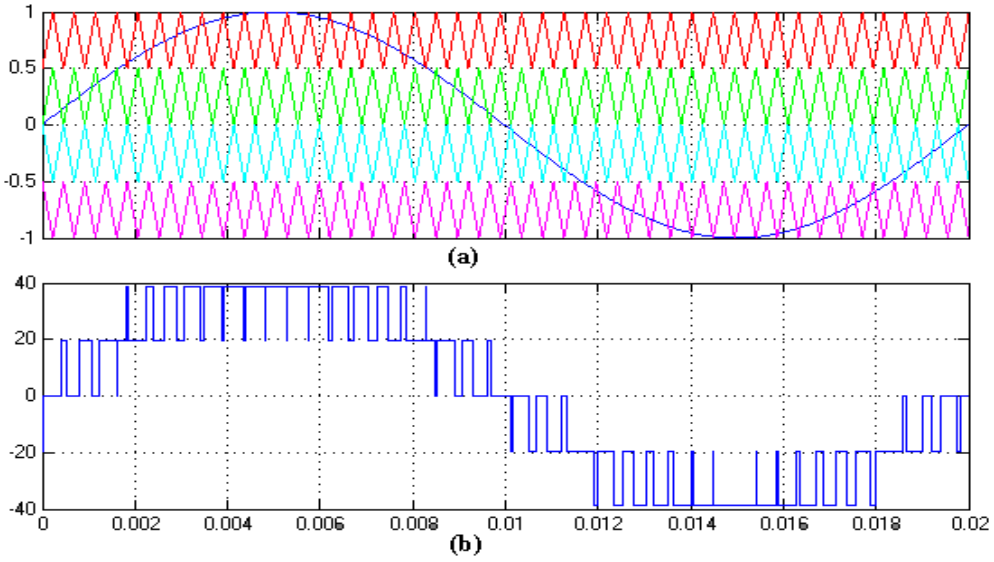


Fig. 3.5 (a) Phase Opposition Disposition technique (b) Five level inverter output voltage

With the POD technique the carrier waveforms above or below the zero reference value are in phase. However, they are phase shifted by 180° between the carrier waveforms above and below zero, as shown in Fig. 3.5 (a). The POD technique yields quarter wave symmetry for even m_f and odd symmetry for odd m_f. In this modulation, dominant harmonics are on the sideband of the first carrier ($m_f \pm 1$) and the phase voltage harmonic at the carrier frequency is not considerable [12]. POD modulation contains significant harmonics in the line voltage spectrum, especially in the first carrier band. Fig. 3.5 (b) shows output phase voltage for five level MLI using POD modulation technique.

3.2.4 ALTERNATIVE PHASE OPPOSITION DISPOSITION (APOD) TECHNIQUE

All carrier waveforms in this APOD technique are phase-displaced by 180° alternatively, as shown in Fig. 3.6 (a).

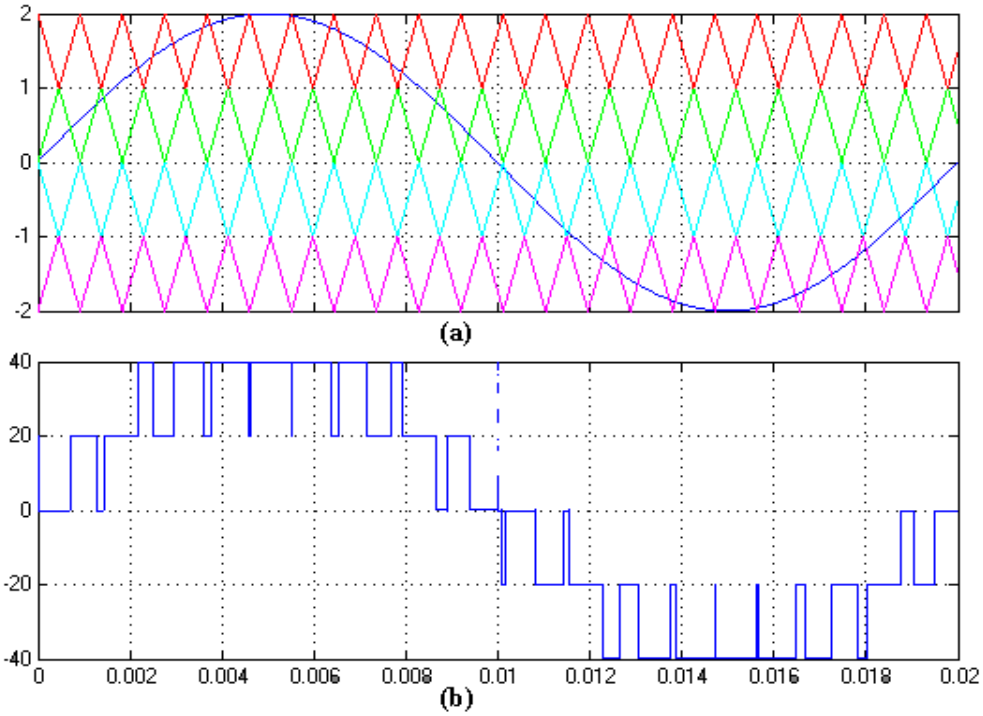


Fig.3.6 Alternative Phase Opposition Disposition technique (b) Five level inverter Output Voltage

This technique requires each of the four carrier waveforms, for a five level inverter output waveform, to be phase displaced from each other by 180° alternately. The voltage at the output of a five level inverter which uses APODPWM control technique is as the following:

- The inverter switches to V/2 if the reference signal is higher than all of carrier signals.
- The inverter switches to V/4 if the reference signal is lower than two above carrier signals and higher than two below carrier signals.
- The inverter switches to –V/4 if the reference signal is lower than two below carrier signals and higher than two above carrier signals.
- The inverter switches to –V/2 if the reference signal is lower than all of carrier signals

It can be seen that APOD modulation does not produce a first carrier harmonic. Instead the dominant harmonics are channeled into the sidebands around the first carrier harmonic. Therefore, since only the triple sidebands away from the carrier frequency cancel in a three phase system, APOD modulation contains some considerable harmonic energy in the line mf is even. If m_f is odd, then the output waveform has odd symmetry. Fig. 3.6 (b) shows output phase voltage for five level MLI using APOD modulation technique.

3.2.5 PHASE SHIFTED (PS) TECHNIQUE

In the phase-shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak-to-peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by Φcr = 360°/(m – 1) where m is voltage level of multilevel inverter.

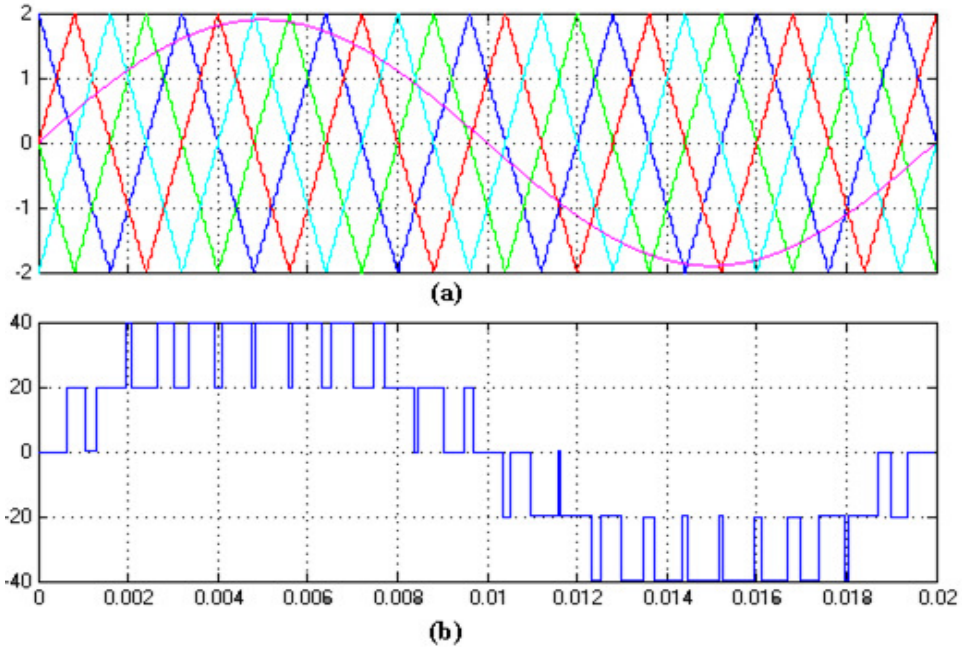


Fig.3.7 (a) Phase Shifted Technique (b) Five level inverter Output Voltage

In general, a multilevel inverter with m voltage levels requires (m – 1) triangular carriers. The gate signals are generated by comparing the modulating wave with the carrier waves. It means for the five level inverter, four triangular carriers are needed with a 90° phase displacement between any two adjacent carriers as shown in Fig. 3.7 (a) Fig. 3.7 (b) shows output voltage for five level MLI [13].

3.3 HYBRID MODULATION TECHNIQUES

Hybrid PWM (H-PWM) is an extension of PWM for CHB with unequal dc sources [14]. The hybrid PWM is the combination of low frequency PWM and high frequency SPWM. The main challenge is to reduce the switching losses of the inverter by reducing the switching frequency of the higher power cells. Therefore, instead of using high frequency carrier-based PWM techniques in all the cells, the high-power cells are operated with square waveform patterns, switched at low frequency, while only the low power cell is controlled with unipolar PWM. An optimized hybrid PDPWM technique commutates the power switches at high frequency and low frequency sequentially.

3.3.1 HYBRID MODULATION STRATEGY

A hybrid modulation strategy combines fundamental frequency switching for higher power cells and open loop PWM control for the low power cell switching at higher frequency [14]-[17]. Fig. 3.8 shows basic block diagram for such technique to be implemented. With this modulation technique the effective spectral response of the output depends on low power cell like IGBT switching while the overall voltage generation is decided by voltage ratings of higher power cells like GTO.

As shown in Fig. 3.8 the command signal is compared with a threshold voltage. If it is larger than the threshold then high voltage cell inverter contributes to the output. The difference between the output of the high voltage inverter and the command signal is then compared against a PWM (ramp) signal to modulate the low voltage cell inverter. The resultant phase voltage obtained is shown in Fig. 3.11. The switching patterns for the high voltage cell inverter and low voltage cell inverter are shown in Fig. 3.9 and 3.10. It may be seen that although the high voltage cell inverter switching is stepped (Fig. 3.9), the overall waveform quality is mainly decided by the intermediate low voltage cell inverter switching (Fig. 3.10). The high voltage cell inverter participates in synthesizing the required high voltage level while the low voltage cell inverter acts as a harmonic compensator.

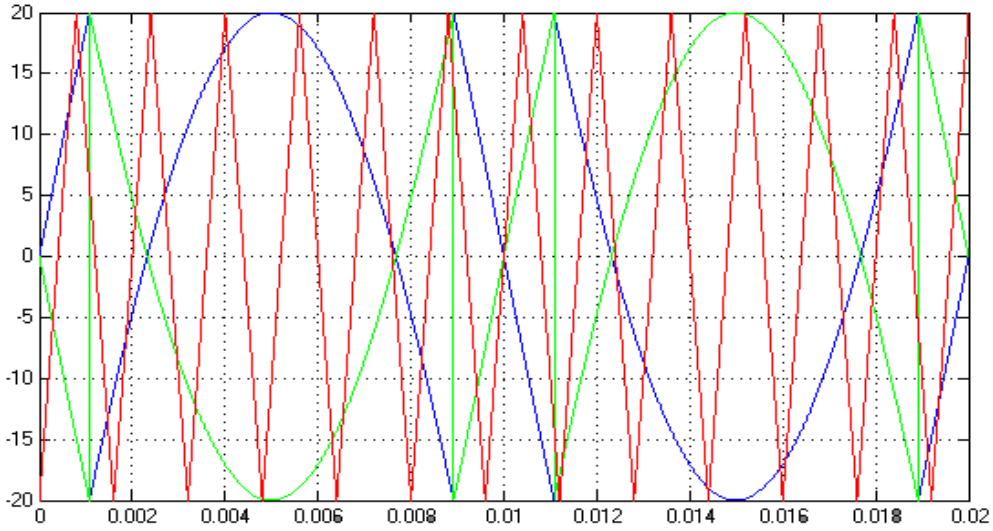


Fig. 3.8 Hybrid modulation strategy

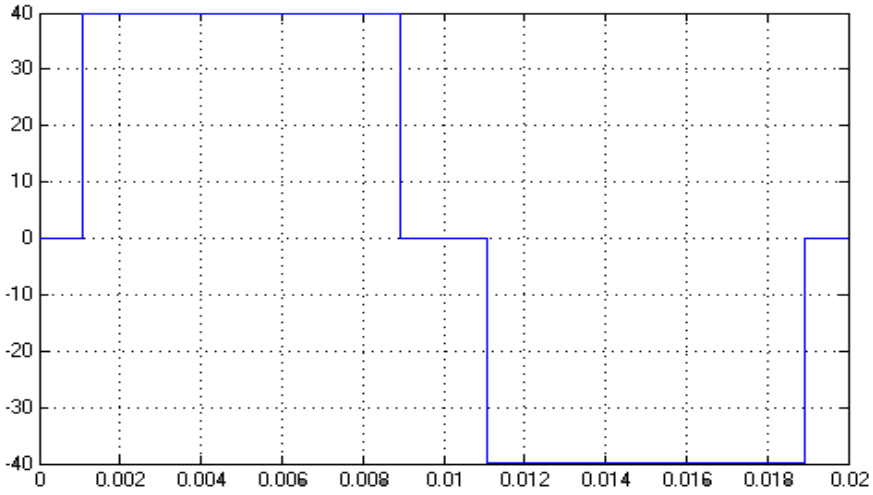


Fig. 3.9 High power cell switching

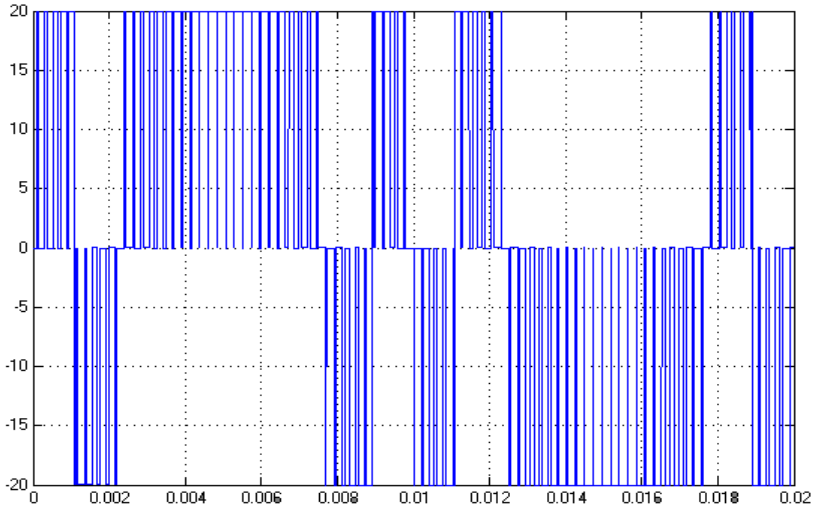


Fig. 3.10 Low power cell switching

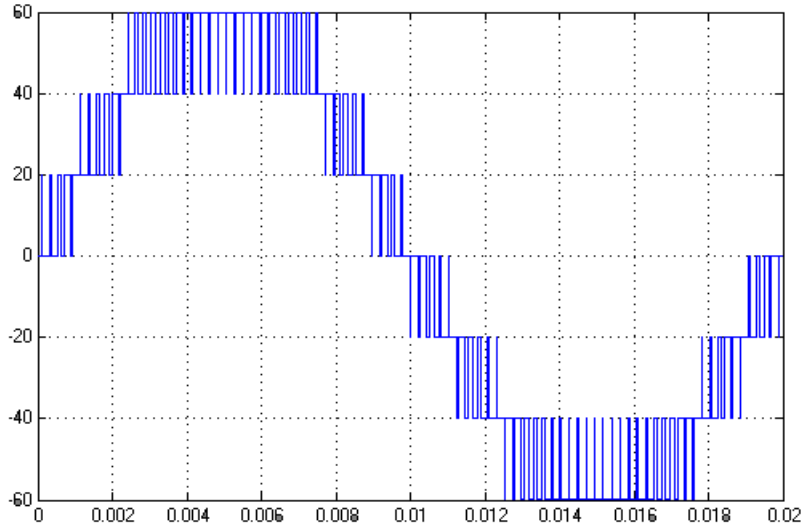


Fig. 3.11 Output phase voltage

3.3.2 INVERTED SINE CARRIER PWM (ISCPWM)

This control strategy replaces the conventional triangular based carrier waveform by inverted sine wave which has a better spectral quality and a higher fundamental output voltage without any pulse dropping [18]. This technique combines the advantage of inverted sine and constant or variable frequency carrier signals as shown in Fig. 3.12 and Fig. 3.13 respectively. However, the fixed frequency carrier based PWM affects the switch utilization in multilevel inverters. In order to balance the switching duty among the various levels in inverters, a variable frequency carrier based PWM has been shown [19]-[20]. Both the techniques are explained in brief.

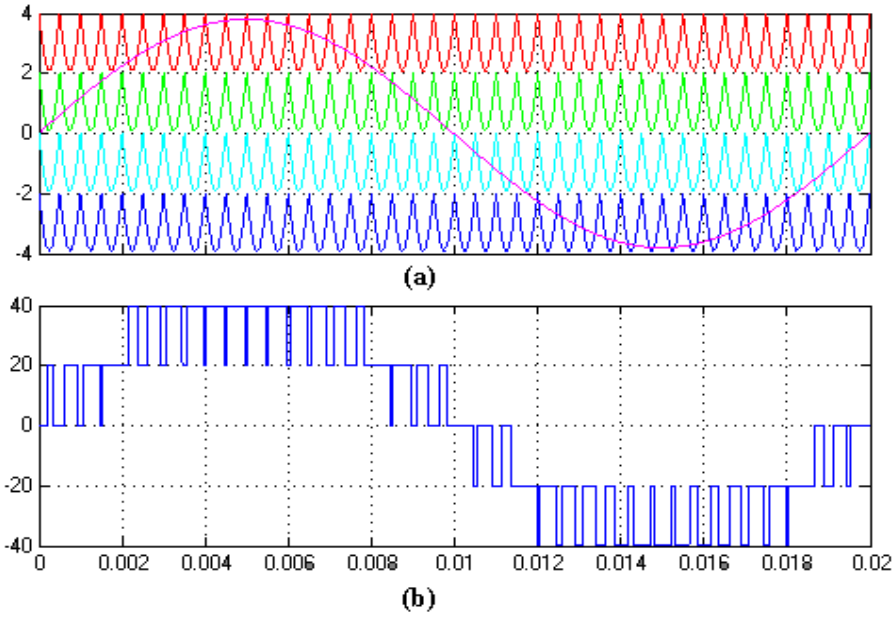


Fig. 3.12 (a) Inverted sine technique (b) Five level inverter output voltage

Fig. 3.12 shows application of unipolar PWM to inverted sine carrier which results in the reduction of carrier frequencies or its multiples and significant reduction in switching losses. Thus advantage of inverted sine and unipolar PWM are combined to improve the performance of the hybrid multilevel inverter. The inverted sine carrier PWM (ISCPWM) technique uses the sine wave as reference signal while the carrier signal is an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. From the Fig. 3.18 it is clear that the pulses are generated whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave.

3.3.3 VARIABLE FREQUENCY INVERTED SINE CARRIER PWM (VFISPWM)

The VFISPWM technique provides an enhanced fundamental voltage, lower THD and minimizes the switch utilization among the bridges in inverters [21]. The number of active switching among the bridges is balanced by varying the carrier frequency based on the slope of the modulating wave in each band. The frequency ratio for each band should be set properly for balancing the switching action for all bridges. Using the slope values of the carrier bands, the new frequencies are calculated. The number of switching actions is balanced for all the switches in bridge with low voltage level switches using the VFISPWM technique. The band dwell time of the modulating wave in each carrier and the frequency ratio (m_f) can be calculated.

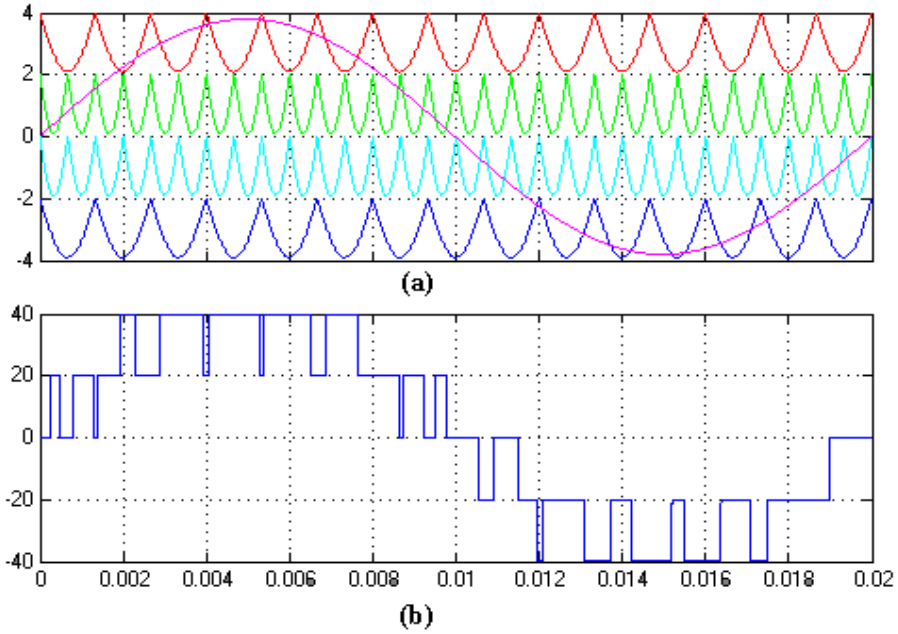


Fig. 3.13 (a)Variable Frequency Inverted Sine Carrier (b) Five level inverter output voltage

As seen hybrid PWM is the combination of low frequency PWM and high frequency SPWM. In each cell of cascaded inverter, the four power devices are operated at two different frequencies, two being commutated at low frequency, i.e. the fundamental frequency of the output, while the other two power devices are pulse width modulated at high frequency. This arrangement causes the problem of differential switching losses among the switches.

An optimized sequential signal is added to the hybrid PWM pulses to overcome this problem. The low and high frequency PWM signal are shown in Fig. 3.14 (c.f [22]). An optimized hybrid PDPWM technique commutates the power switches at high frequency and low frequency sequentially.

A common sequential signal and low frequency PWM signals are used for all cells in cascaded inverter. A high frequency SPWM for each cell is obtained by the comparison of the rectified modulation waveform with corresponding phase disposition carrier signal. The low frequency PWM signal should be synchronized with the modulation waveform. In Fig. 3.15 (c.f [22]) the gate pulses are generated by a hybrid PWM controller. This controller is designed to mix the sequential signal low frequency PWM and high frequency phase disposition sinusoidal PWM and to generate the appropriate gate pulses for cascaded inverter.

3.3.4 OPTIMIZED HYBRID PDPWM

An optimized hybrid PDPWM switching pattern can be generalized for N level inverter. Let N be the number of levels of the cascaded inverter. M is the number of inverter cells, M=N-1/2. The modulation index is therefore defined as ma= A_m /MA_c and the definition of the frequency ratio mf= f_m/f_c, where f_c as carrier frequency and f_m as modulating signal frequency. The modulating signal A_m is modified based on number of levels and modulation index. A modified sinusoidal modulating signal is then compared with each phase disposition carrier signal separately to generate M number of high frequency sinusoidal PWM signals. A hybrid PWM controller is used to mix low frequency PWM and the corresponding high frequency SPWM for M^{th} inverter cell. This hybrid PWM for M^{th} inverter cell is then optimized with sequential signal in order to equalize switching transitions. Similarly, hybrid PWM pulses are developed for all cells in any level cascaded inverter [22].

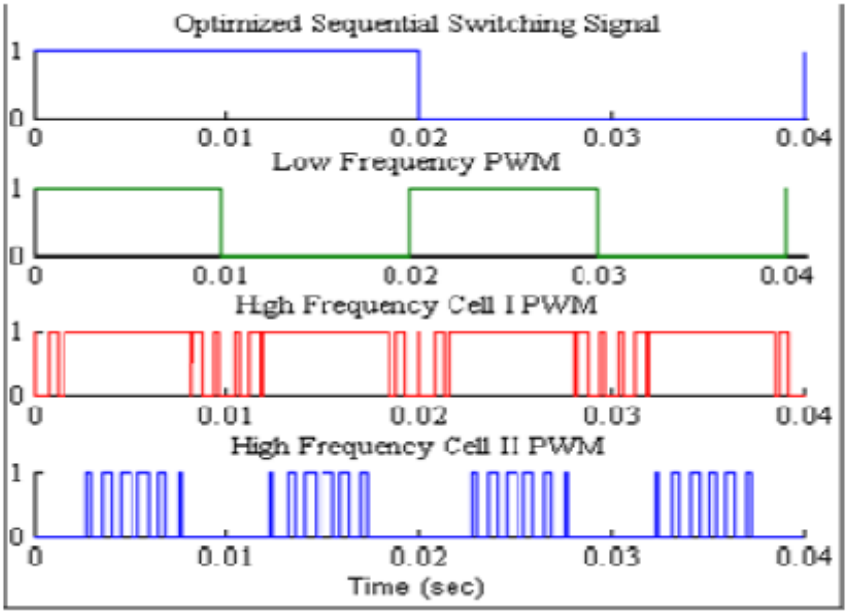


Fig. 3.14 Low and high frequency PDPWM

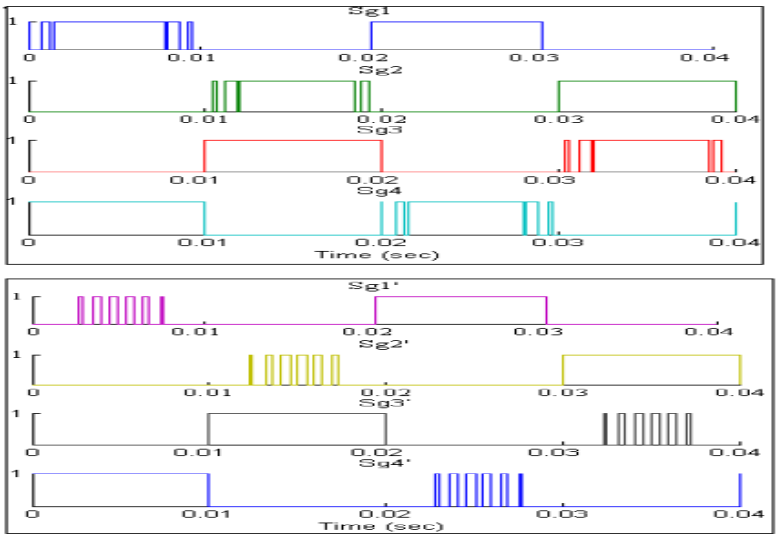


Fig. 3.15 Optimized hybrid PDPWM switching pattern for five level cascaded MLI

3.4 SWITCHING FREQUENCY OPTIMAL PWM

When the carrier wave is synchronized with the modulating wave (mf is an integer), the modulation scheme is known as synchronous PWM. The synchronous PWM scheme is more suitable for implementation with a digital processor. For a m-level inverter, m-1 carriers with the same frequency fc and the same amplitude Ac are disposed such that the bands they occupy are contiguous [28]. The reference wave form has peak to peak amplitude Am, the frequency fm, and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If

the reference is greater than s carrier signal, then they active device corresponding to that carrier is switched off. This technique is further explained in following section.

3.4.1 MULTI CARRIER SWITCHING FREQUENCY OPTIMAL PWM (MC-SFO PWM)

The other technique to improve the gain of pulse width modulator in a multilevel inverter is Switching Frequency Optimal PWM (SFO-PWM) [23]. This modulation is similar to the group of pure sinusoidal PWM (SPWM) and applicable for three-phase systems but the zero sequence (3rd harmonic) of voltage is injected to each reference signals [24]. This technique calculates the average value of maximum and minimum of instantaneous reference voltages and for all the modulation waveforms subtract this value from the reference voltage.

$$V_{offset} = \mathrm{Max}(V_a, V_{b,} V_c) + \mathrm{Min}(V_a, V_{b,} V_c)$$

$$V\_aSFO = V\_a - V\_offset$$

$$V\_bSFO = V\_b - V\_offset$$

$$V\_cSFO = V\_c - V\_offset$$

Analog circuit to make the reference signal of SFO-PWM is shown in Fig. 3.16 [25] – [27]. Fig. 3.17 shows the SFO-PWM with injection of a third-harmonic into the reference waveforms which achieves a 15% increase in modulation index over sinusoidal PWM before over modulation nonlinearities occur. It is simply because of the reduced height of the three phase reference envelope that is achieved by third-harmonic injection. In this technique, the 3rd harmonic is cleared in three-phase system.

The results indicate that the third-harmonic injection offers minimal harmonic advantage for PWM of multilevel inverters, since the harmonic distribution of line voltage spectrum is not improved significantly. Therefore, this optimization only has the value to increase the available linear modulation region if this is required [36].

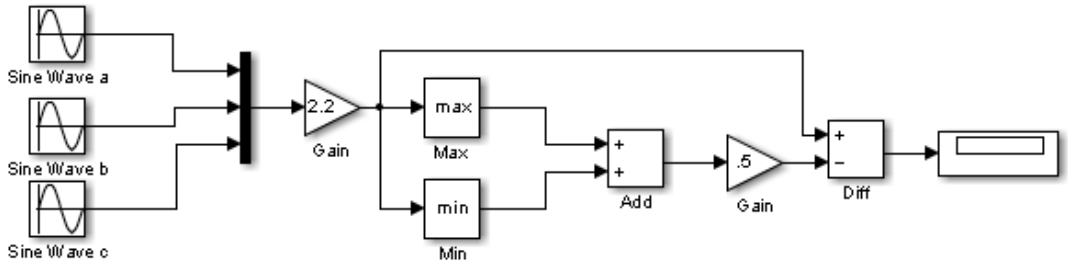


Fig. 3.16 Analog circuit to make the reference signals in SFO-PWM technique

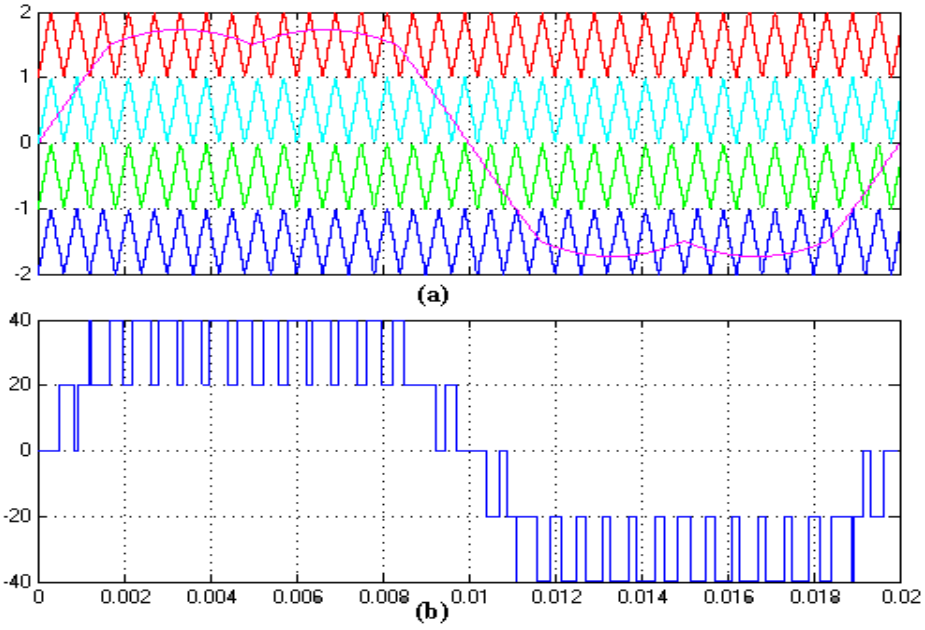


Fig. 3.17 SFO-PWM technique for a 9-level asymmetric inverter output

3.4.2 PHASE SHIFTED CARRIER SWITCHING FREQUENCY OPTIMAL PULSE WIDTH MODULATION (PSC-SFO PWM) OR PHASE-SHIFTED SUBOPTIMAL CARRIER PWM (PS-SUB-PWM)

Fig.3.18 shows the phase shifted carrier SFO PWM modulating signal generation [28]. The technique takes the instantaneous average of the maximum and minimum of the three reference voltages (Va, Vb, Vc) and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms, which is shown in Fig.3.19. From the above criteria the following equation are obtained.

Vcarrier = {max (Va,Vb,Vc) + min (Va,Vb,Vc)} / 2

VaSFO = Va – Vcarrier

VbSFO = Vb – Vcarrier

VcSFO = Vc – Vcarrier

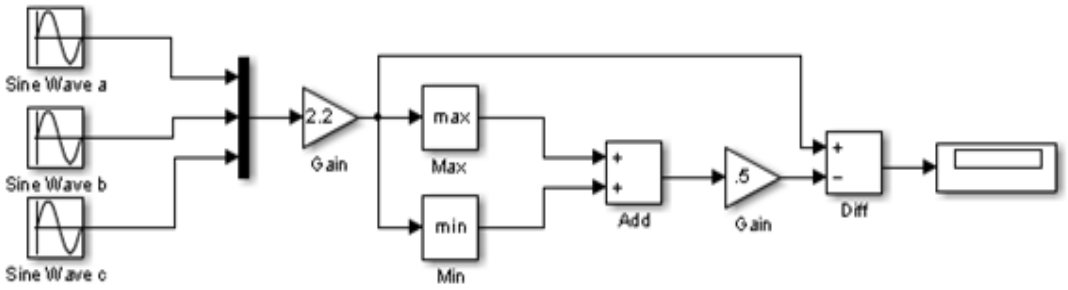


Fig.3.18 PSC-SFO PWM modulating signal generation

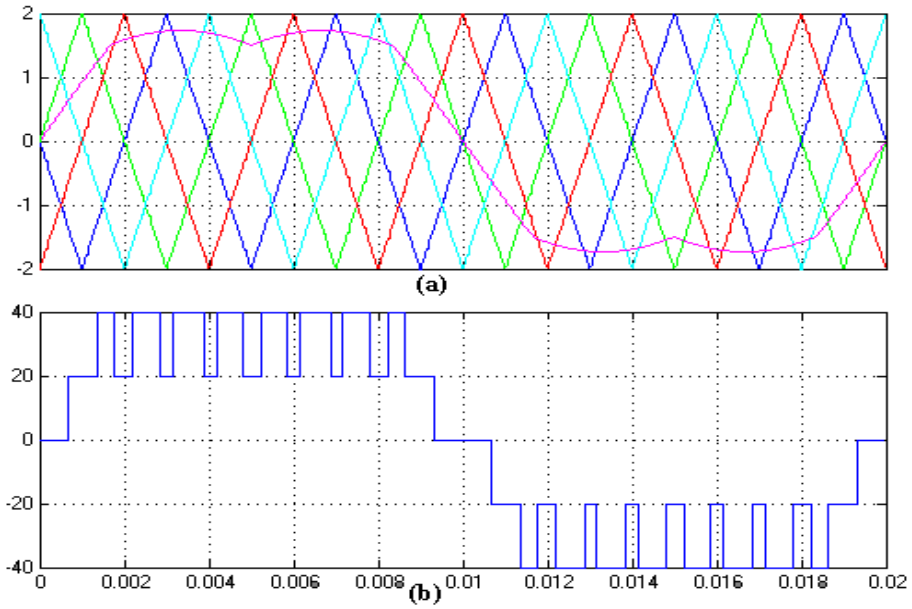


Fig. 3.19 Phase shifted carrier switching frequency optimal pulse width modulation

The carrier voltage is the average of maximum and minimum value of Va,Vb,Vc. The phase voltage using SFO is the difference between reference voltages to carrier voltage. The zero sequence modification made by the SFO PWM technique restricts its use to three phase three wire system, however it enables the modulation index to be increased by 15% before over modulation or pulse dropping occurs.

Fig. 3.19 shows an example of the five-level PS-SUB-PWM technique where switching angles in 1/4-period are defined.

3.5 HIGHER AND LOWER CARRIER CELLS AND ALTERNATIVE PHASE OPPOSITION PW (HLCCAPOPWM)

The PWM control technique based on the improvement of carrier phase disposition PWM (PDPWM) is called higher and lower carrier cells alternative phase opposition PWM (HLCCAPOPWM) for the hybrid-clamped multilevel inverter Fig. 3.20 [30].

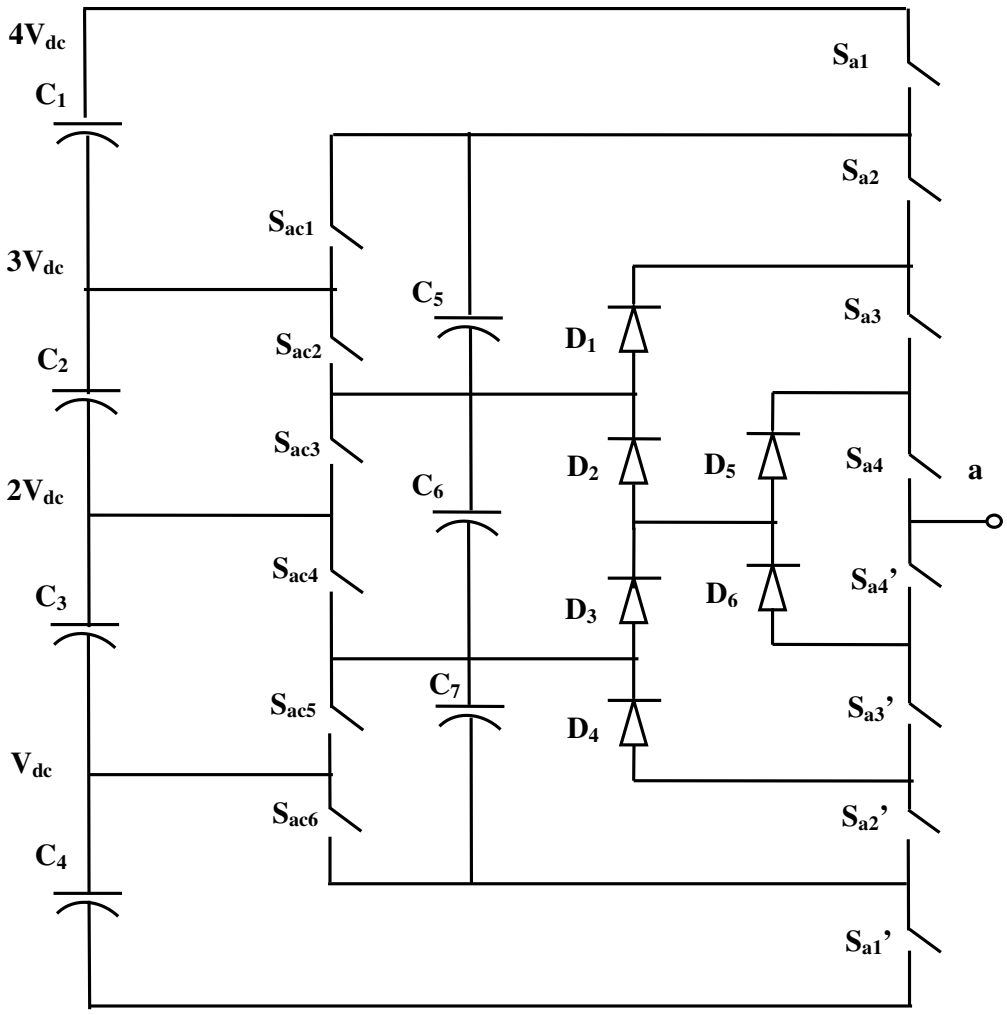


Fig. 3.20 Hybrid clamped five level inverter

3.5.1 PRINCIPLE OF HLCCAPOPWM

The principle of the HLCCAPOPWM technique is explained by introducing the concept of carrier cell. When the carrier waveforms are divided according to the carrier period then the individual triangle wave is called carrier cell as shown in Fig. 3.21[30].. This technique can reduce switching losses and improve the output harmonic performance in low harmonic bands. The concept of carrier cell provides a new clue for improving carrier waveforms of switching devices for the hybrid-clamped multilevel inverter. The novel PWM technique can effectively reduce the number of device switching on or off in different degrees hence reducing switching losses within broad modulation index range. In other words the switching frequency with the HLCCAPOPWM technique can be increased under the condition of the same switching losses with the PDPWM technique and then the harmonic content of output voltage will

be further lowered. In addition the energy of lower harmonics transfers to higher harmonics band with the HLCCAPOPWM technique. The reduction of the energy of lower harmonics can simplify the design of output filter and reduce its size.

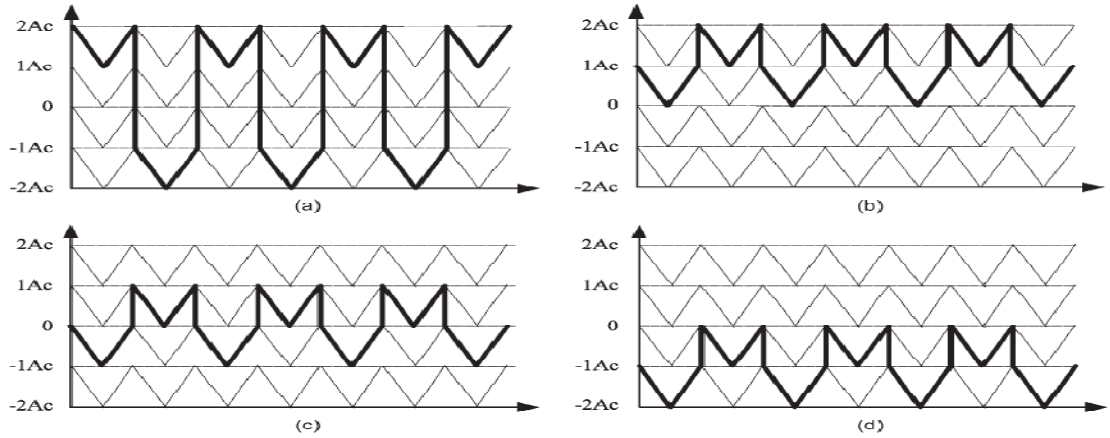


Fig. 3.21 Carrier waveforms of the upper four main switching devices for a hybrid-clamped five-level inverter with the PDPWM technique. (a) Carrier of S_{a1}. (b) Carrier of S_{a2}. (c) Carrier of S_{a3}. (d) Carrier of S_{a4}

3.5.2 HLCCAPOPWM CONTROL TECHNIQUE

Using the concept of carrier cell, it can be seen from Fig. 3.21 that the carrier waveforms of the PDPWM technique for hybrid-clamped multilevel inverters have two features: 1) all the carrier cells are in phase and 2) the carrier cells of main switching devices S_{a1}, S_{a2}, S_{a3}, and S_{a4} are positioned on the higher and lower carrier bands respectively. Furthermore the higher and the lower carrier cells alternate by turns constantly [31]. For S_{a1} the higher carrier cells are positioned on the first carrier band and the lower ones on the fourth carrier band. For S_{a2} the higher carrier cells are positioned on the first carrier band and the lower ones on the second carrier band. For S_{a3} the higher carrier cells are positioned on the second carrier band and the lower ones on the third carrier band. For S_{a4} the higher carrier cells are positioned on the third carrier band and the lower ones on the fourth carrier band. If the higher carrier cells and the lower ones are in phase the corresponding PWM pulse waveform is shown in Fig. 3.22(a) [31] which is produced by a higher carrier cell intersecting the modulation wave. As it is known the device controlled by this PWM pulse waveform will turn on or off four times. If the higher carrier cells are reversed then the higher carrier cells and the lower ones are in phase opposition. In addition the corresponding PWM pulse waveform is shown in Fig. 3.22 (b) c.f [31] which is also produced by a higher carrier cell intersecting the same modulation wave. It is clear that the number of device switching on or off is two, only

half of that shown in Fig. 3.22 (a). Fig. 3.23 c.f [31] shows two PWM pulse waveforms respectively produced by two kinds of carrier cells in phase opposition intersecting a certain modulation waveform.

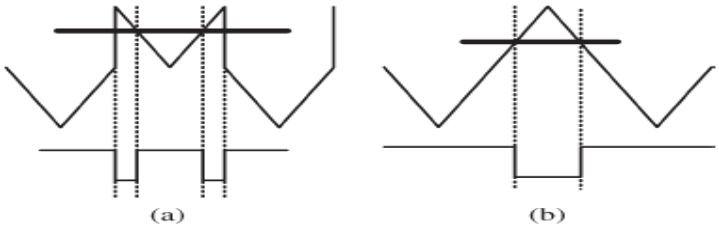


Fig. 3.22 Device switching on or off (a) Higher carrier cells and lower carrier cells in phase. (b) Higher carrier cells and lower carrier cells in phase opposition

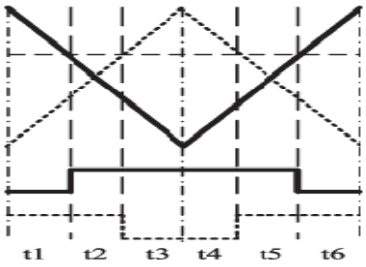


Fig. 3.23 PWM pulse waveforms respectively produced by the carrier cells in phase opposition intersecting a certain modulation wave

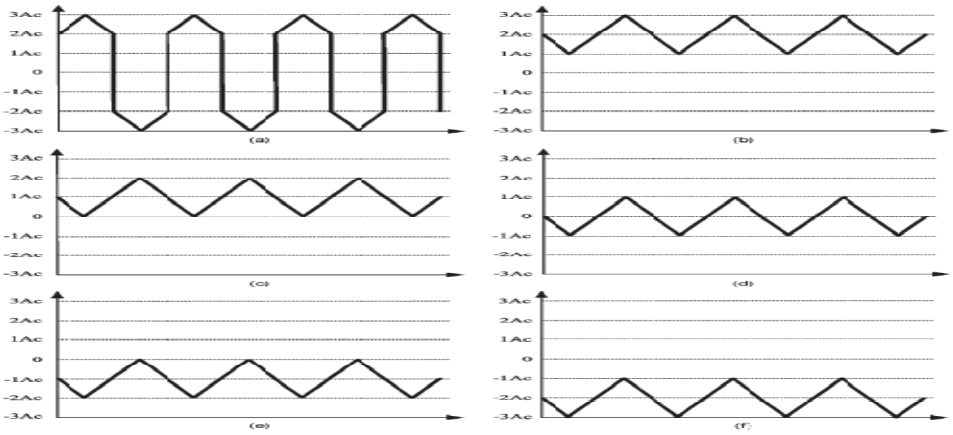


Fig. 3.24 Carrier waveforms of the upper six main switching devices for a seven level inverter with the HLCCAPOPWM technique. (a) Carrier of S_{a1}. (b) Carrier of S_{a2}. (c) Carrier of S_{a3}. (d) Carrier of S_{a4}. (e) Carrier of S_{a5}. (f) Carrier of S_{a6}

If the duty cycles during one carrier period of two PWM pulses are equal then the instantaneous values of the output voltage fundamental component are also equal so the modulation performance of two kinds of carrier cells in phase opposition as shown in Fig. 3.23 are identical. Therefore it is feasible to improve the carrier waveforms of every switching device shown in Fig. 3.21 by reversing all the higher carrier cells to reduce the

number of device switching on or off. As a result the higher and lower carrier cells will be in phase opposition for every switching device. The improved carrier waveforms for switching devices S_{a1}, S_{a2}, S_{a3}, and S_{a4} are shown in Fig. 3.24 c.f [31].

3.6 ALTERNATIVE HYBRID PWM (AHPWM)

Fig. 3.25 [32] shows the carriers of another PDPWM technique. The initial phase angle of the triangle carrier waveform is 180^0 so it is called "W" PDPWM technique. Seen from Fig. 3.26 [32] it is known that when the modulation waveform intersects the first carrier band, even if the two adjacent intersecting points respectively locate in the carrier waveforms of two different devices, no switching modes conversion occurs at the edge of the two kinds of carrier waveforms, which means no unexpected output levels will emerge when the modulation waveform intersects the second or the third or the fourth carrier band and the two adjacent intersecting points respectively locate in the carrier waveforms of two different devices, switching modes conversions with the same output levels will occur at the edge of the two kinds of carrier waveforms which means unexpected output levels will emerge.

3.6.1 "W" PDPWM AND "M" PDPWM TECHNIQUE

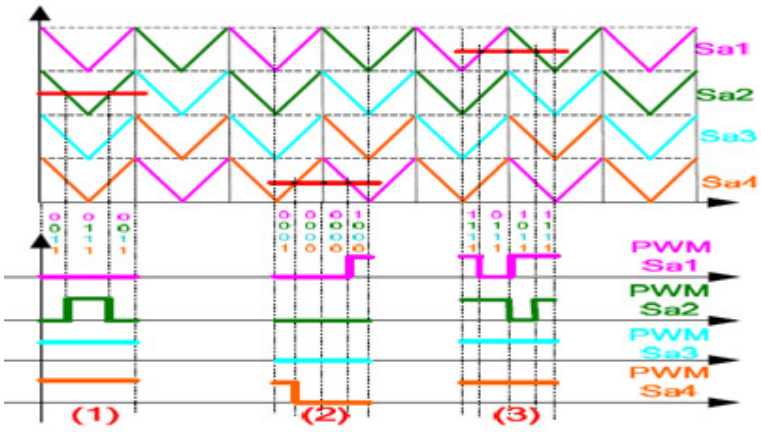


Fig. 3.25 Carrier waveforms and the representative PWM pulse waveforms of the "W" PDPWM technique

In Fig. 3.25 c.f [32], when the modulation waveform intersecting points respectively locate in the carrier waveforms of two different devices, no switching modes conversion occurs at the edge of the two kinds of carrier waveforms, which means no unexpected output level will emerge; when the modulation waveform intersects the first or the second or the third carrier band and the two adjacent intersecting points respectively locate in the carrier waveforms of two different devices, switching modes

conversions with the same output levels will occur at the edge of the two kinds of carrier waveforms, which means unexpected output levels will emerge.

Obviously, if the "M" carriers are applied to the first carrier band and the "W" carriers to the fourth carrier band, the switching modes conversions causing the unexpected output levels can be avoided[4]. On the other hand, in order to avoid the switching modes conversions causing the unexpected output levels for the second and third carrier bands, the carrier cells (triangle waveforms) in opposite phase alternatively are applied to these two carrier bands respectively, as shown in Fig. 3.27 c.f [32], which is called AHPWM (Alternative Hybrid PWM) technique.

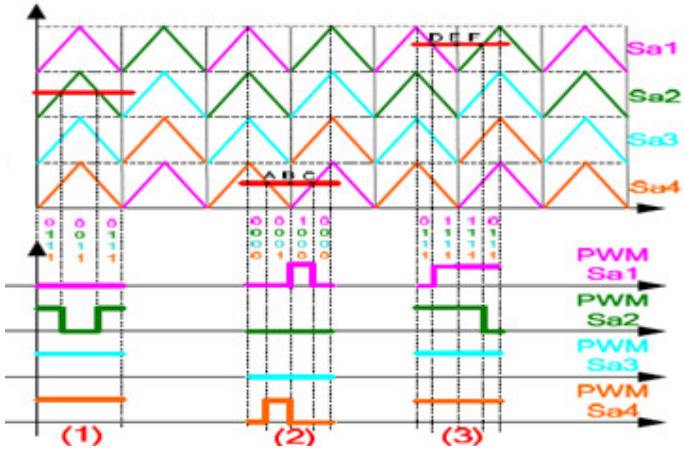


Fig. 3.26 Carrier waveforms and the representative PWM pulse waveforms of the "M" PDPWM technique

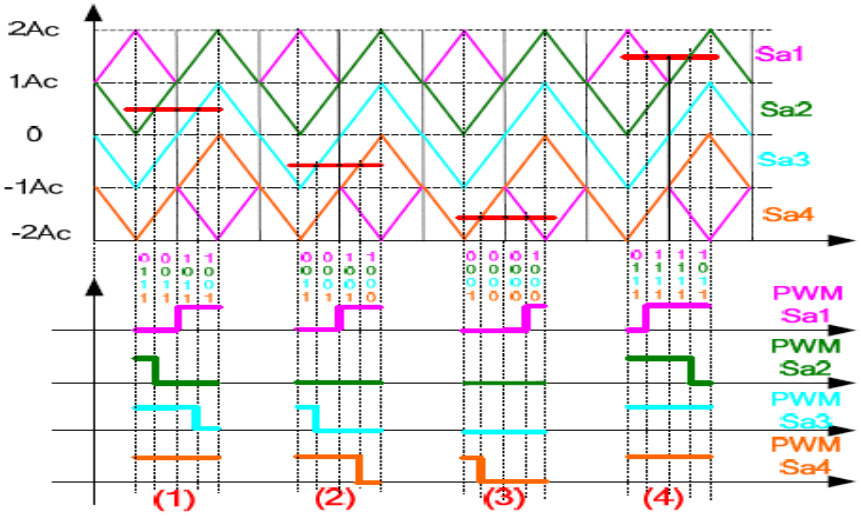


Fig. 3.27 Carrier waveforms and the representative PWM pulse waveforms of AHPWM technique

Fig. 3.27[32] shows four cases of the modulation waveform intersecting four carrier bands respectively. Case "(3)" is similar to the case "(2)" in Fig. 3.25, and case

"(4)" is similar to the case "(3)" in Fig. 3.26 c.f [32], that is to say, no switching modes conversions occur at the edge of two kinds of carrier waveforms with different colors, so no unexpected output levels emerge. In the case of "(1)" and case of "(2)", applying the alternative hybrid carrier cells (triangle waveforms), the switching modes conversions at the edge of two kinds of carrier waveforms with different colors is corresponding to the different output levels respectively, so no unexpected output levels will emerge, which is known from the above analyses [32].

3.7 SPACE VECTOR MODULATION

The space vector modulation technique is based on reconstruction of sampled reference voltage with help of switching space vectors of a voltage source inverter in a sampling period. Each multilevel inverter has several switching states which generate different voltage vectors and can be used to modulate the reference. In SVM, the reference signal is generated from its closest signals. Some vectors have redundant switching states, meaning that they can be generated by more than one switching state this feature is used for balance of capacitor voltages. Multilevel SVM must manage this behavior to optimize the search of the modulating vectors and apply an appropriate switching sequence.

3.7.1 SPACE VECTORS

The space vector modulation (SVM) is also described using symmetrical three-phase systems in the α-ß reference frame. The three-phase reference voltages are represented as a single reference phasor with constant length and angular speed. It substitutes the demanded voltage space vectors by the nearest real voltage space vectors in an appropriate combination in each sampling interval. The basic principles of the SVM is shown in Fig. 3.28 c.f [33] for three level inverter, which involves 27 different inverter switch states (= number of level)^3 [33]. Using a three to two dimensional transformation, the desired output averaged over the switch period and the inverter states are represented as vectors. The visualization and calculation of switching periods is then performed using simple vector math.

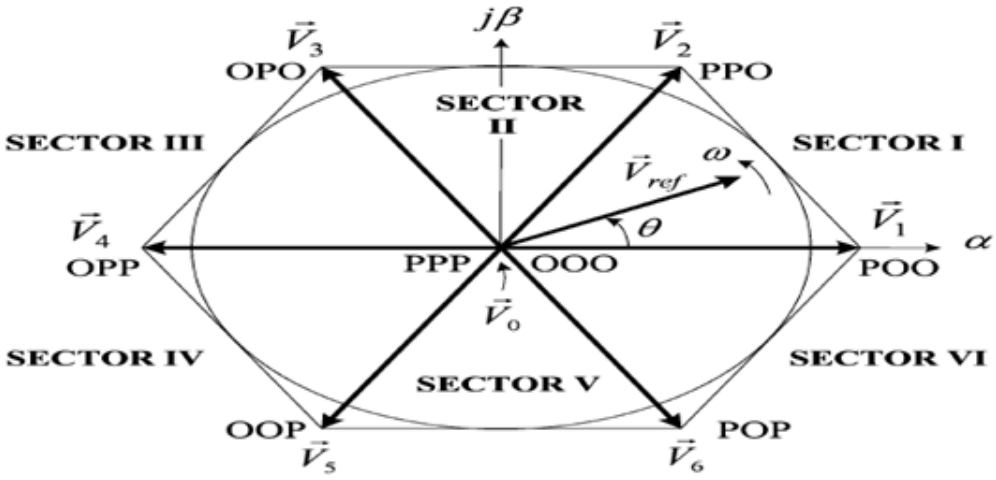


Fig. 3.28 Space vector diagram for the two-level inverter

The voltage common to all three phases can be found at the neutral point of a balanced star connected load. It is known as the zero sequence component. By allowing the neutral point voltage to vary, one phase leg can be held continuously high or low for a 60 degree interval while the other two switch. The correct phase to phase waveforms are still formed. This has two significant advantages.

Firstly, the inverter's full potential modulation depth can be used since the phase to phase voltages are maximized. Secondly, the switching losses are lowered, since the average switching frequency falls to two thirds of its original value. If suitable zero sequence space vectors can be identified for multilevel inverters, the simplicity of multilevel modulator implementations using phase shifted triangular carriers can be retained.

The SVM approach is perhaps the most powerful, because it allows more freedom to control and optimize the switching patterns than any other modulation approach; at the same time, for inverters with higher number of levels it becomes too cumbersome for real-time implementation.

For a given magnitude (length) and position $\overrightarrow{V_{ref}}$ can be synthesized by three nearby stationary vectors, based on which the switching states of the inverter can be selected and gate signals for the active switches can be generated. When $\overrightarrow{V_{ref}}$ passes through sectors one by one, different sets of switches will be turned on or off. As a result, when $\overrightarrow{V_{ref}}$ rotates one revolution in space, the inverter output voltage varies one cycle over time. The inverter output frequency corresponds to the rotating speed of $\overrightarrow{V_{ref}}$ while its output voltage can be adjusted by the magnitude of $\overrightarrow{V_{ref}}$.

The dwell time for the stationary vectors essentially represents the duty-cycle time (on-state or off-state time) of the chosen switches during a sampling period *Ts* of the modulation scheme. The dwell time calculation is based on 'volt-second balancing' principle, that is, the product of the reference voltage $\overrightarrow{V_{ref}}$ and sampling period *Ts* equals the sum of the voltage multiplied by the time interval of chosen space vectors. When $\overrightarrow{V_{ref}}$ falls into sector I as shown in Fig. 3.29 c.f [33] it can be synthesized by $\overrightarrow{V_1}$, $\overrightarrow{V_2}$ and $\overrightarrow{V_0}$.

Table 3.1 Space Vectors, Switching States, and On-State Switches

Space Vector	Switching State (Three Phases)	On-State Switch	Vector Definition
$\overrightarrow{V_0}$	[PPP] [OOO]	S1, S3, S5 S4, S6, S2	$\overrightarrow{V_0} = 0$
$\overrightarrow{V_1}$	[POO]	S1, S6, S2	$\overrightarrow{V_1} = \frac{2}{3} V_d e^{j0}$
$\overrightarrow{V_2}$	[PPO]	S1, S3, S2	$\overrightarrow{V_2} = \frac{2}{3} V_d e^{j\frac{\pi}{3}}$
$\overrightarrow{V_3}$	[OPO]	S4, S3, S2	$\overrightarrow{V_3} = \frac{2}{3} V_d e^{j\frac{2\pi}{3}}$
$\overrightarrow{V_4}$	[OPP]	S4, S3, S5	$\overrightarrow{V_4} = \frac{2}{3} V_d e^{j\frac{3\pi}{3}}$
$\overrightarrow{V_5}$	[OOP]	S4, S6, S5	$\overrightarrow{V_5} = \frac{2}{3} V_d e^{j\frac{4\pi}{3}}$
$\overrightarrow{V_6}$	[POP]	S1, S6, S5	$\overrightarrow{V_6} = \frac{2}{3} V_d e^{j0\frac{5\pi}{3}}$

The coefficient 2/3 is somewhat arbitrarily chosen. The commonly used value is 2/3 or √2/3. The main advantage of using 2/3 is that the magnitude of the two-phase voltages will be equal to that of the three-phase voltages after the transformation. A space vector can be generally expressed in terms of the two-phase voltages in the α-ß plane. The zero vector $\overrightarrow{V_0}$ has two switching states [PPP] and [OOO], one of which seems redundant. The redundant switching state can be utilized to minimize the switching frequency of the inverter or perform other useful functions. Note that the zero and active vectors do not move in space, and thus they are referred to as stationary vectors. On the contrary, the reference vector $\overrightarrow{V_{ref}}$ in Fig. 3.29 rotates in space at an angular velocity $\omega = 2\pi f_1$

where *f*1 is the fundamental frequency of the inverter output voltage.

The angular displacement between $\overrightarrow{V_{ref}}$ and the α axis of the α-ß plane can be obtained by $\theta(t) = \int_0^t \omega(t)dt + \theta(0)$

With the space vectors selected and their dwell times calculated, the next step is to arrange switching sequence. In general, the switching sequence design for a given $\overrightarrow{V_{ref}}$ is not unique, but it should satisfy the following two requirements for the minimization of the device switching frequency: (a) The transition from one switching state to the next involves only two switches in the same inverter leg, one being switched on and the other switched off. (b) The transition for $\overrightarrow{V_{ref}}$ moving from one sector in the space vector diagram to the next requires no or minimum number of switchings.

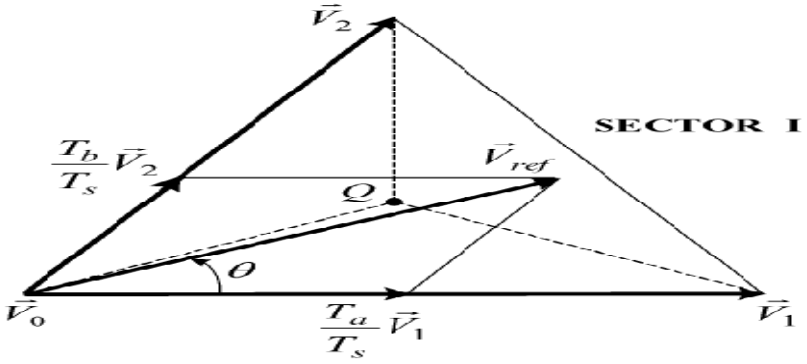


Fig. 3.29 $\overrightarrow{V_{ref}}$ synthesized by $\overrightarrow{V_1}$, $\overrightarrow{V_2}$ and $\overrightarrow{V_0}$

3.7.2 SWITCHING SEQUENCE

Fig. 3.30 c.f [33] shows a typical seven-segment switching sequence and inverter output voltage waveforms for $\overrightarrow{V_{ref}}$ in sector I, where $\overrightarrow{V_{ref}}$ is synthesized by $\overrightarrow{V_1}$, $\overrightarrow{V_2}$ and $\overrightarrow{V_0}$. The sampling period *Ts* is divided into seven segments for the selected vectors.

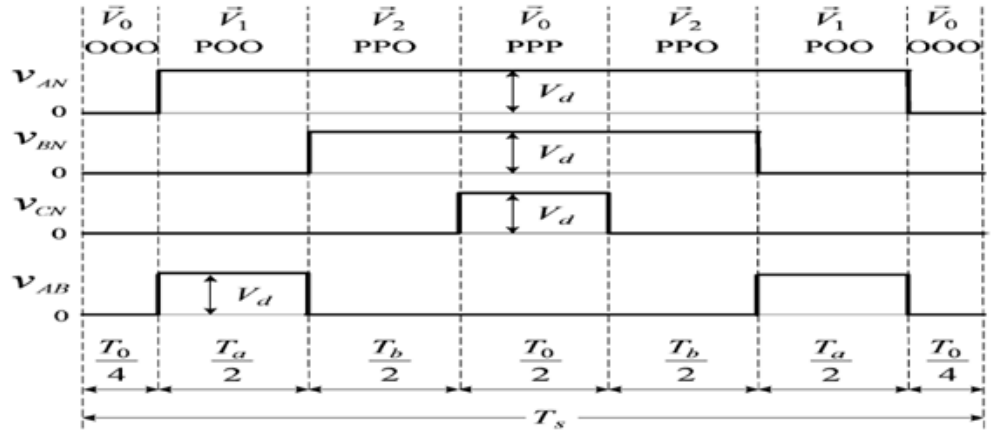


Fig.3.30 Seven-segment switching sequence for $\overrightarrow{V_{ref}}$ in sector I

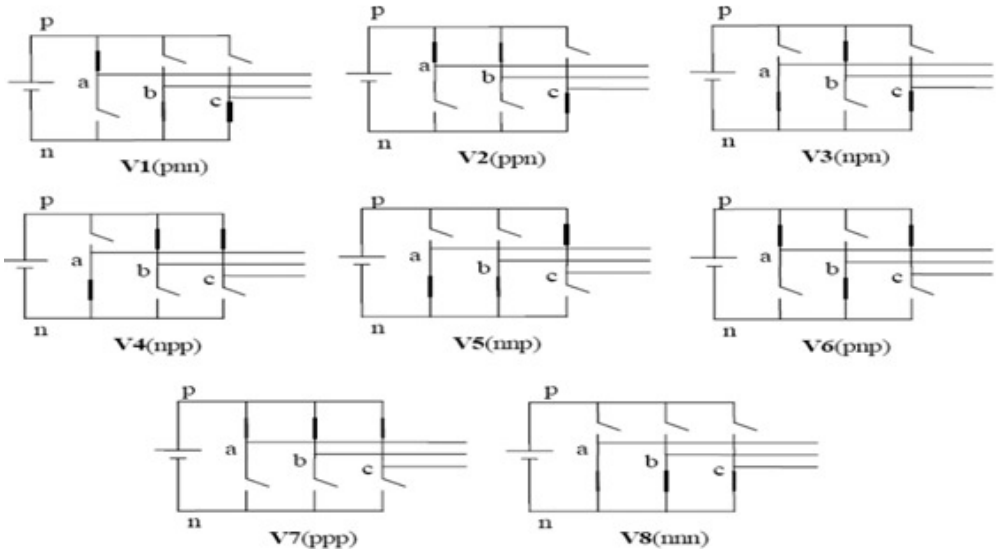


Fig. 3.31 Eight switching state topologies of a voltage source inverter

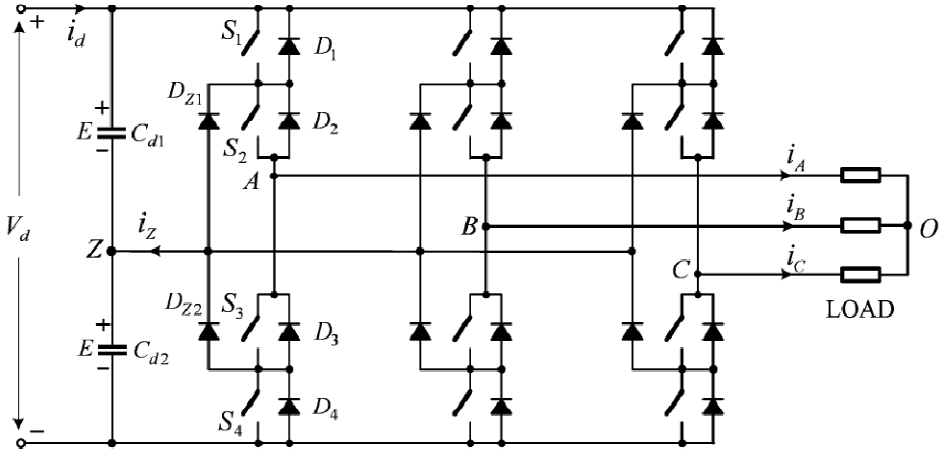


Fig. 3.32 Three-level NPC inverter

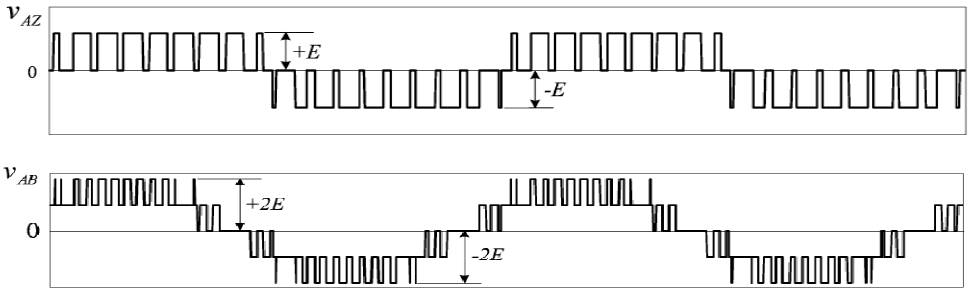


Fig. 3.33 Output voltage waveforms of the NPC inverter

The line-to-line voltage waveform produced by the SVM inverter contains even-order harmonics which can be eliminated by modified SVM scheme. As the switching sequence design is not unique for a given set of stationary vectors and dwell times, switching discontinuity can give discontinuous space vector modulation.

3.8 COMPARISON OF MODULATION TECHNIQUES ON BASIS OF MODULATION INDEX

It is observed that THD varies with type of inverter topology, output level and modulation index. Generally variability in THD is about 10% for different modulation techniques [1-34].

Table 3.2 Modulation techniques summarized

Sr. No	Modulation Technique	Output Voltage level	Topology(Diode Clamped, Flying Capacitor, Cascaded MLI or Hybrid MLI)	THD (Approx) %
1	Phase Disposition (PD) Technique	5 9 7 5	NPC Asymmetrical MLI Hybrid cascaded MLI Cascaded MLI	13 15.7 6.5/5.23 5.2
2	Phase Opposition Disposition (POD) Technique	5	Cascaded MLI	6.56 6.8
3	Alternative Phase Opposition Disposition (APOD)	5	Cascaded MLI	5.68 12.9
4	Phase Shifted (PS) Technique	5	Cascaded MLI	9.72
5	Hybrid modulation techniques	9	Hybrid MLI	13.96
6	Optimized Hybrid PDPWM	7 9 11	Cascaded MLI	17.19 12.87 9.95
7	ISPWM	7	Asymmetric Cascaded Multilevel Inverter	7.98
8	VFISPWM	7	Hybrid MLI	5.92
9	Multi carrier switching frequency optimal PWM (MC-SFO PWM)	5	Cascaded	21.5
10	Phase Shifted Carrier Switching Frequency Optimal Pulse Width Modulation (PSC-SFO PWM)	5	Cascaded	20.5
11	Phase-Shifted Suboptimal Carrier PWM (PS-SUB-PWM)	5	Cascaded	.22
12	Higher and Lower Carrier Cells and Alternative Phase Opposition PWM (HLCCAPOPWM)	5	Hybrid MLI	38.6
13	Alternative hybrid PWM (AHPWM)	5	Hybrid MLI	35.95
14	SPACE VECTOR MODULATION PD POD APOD	5	Cascaded	 4 .45 5.23 10.38

Some modulation techniques are easy to implement but as in hybrid modulation technique if it is implemented directly i.e. by using low frequency and high frequency

modulation with constant carrier frequency then THD is higher as compared with ISPWM, VFISPWM or optimized hybrid PWM. Similarly as the complication of generating and implementing of modulation techniques is increased THD decreases. Also some modulation techniques can be directly applied to multilevel inverters like NPC but modifications are required for implementing same technique to hybrid multilevel inverter. Comparison is briefly summarized in Table 3.2.

Space vector modulation technique has more degree of freedom in control and optimization of switching pattern as compared to other techniques. But at the same time its real time implementation is difficult for multilevel inverters with higher number of levels. HLCCAPOPWM and alternative hybrid modulation techniques are related with PDPWM and THD obtained is not much low but it can be further improved by taking appropriate modulation index. Thus various modulation techniques can be used directly or hybrid technique can be applied for hybrid multilevel inverter.

3.9 SUMMARY

The different modulation techniques are discussed in this chapter. It is observed that total harmonic distortion changes with inverter topology, output levels of multilevel inverter and modulation index. Some modulation techniques are easy to implement but as in hybrid modulation technique if it is implemented directly i.e by using low frequency and high frequency modulation with constant carrier frequency then THD is higher as compared to ISPWM, VFISPWM or optimized hybrid PWM. Similarly as the complexity of generation and implementation of modulation techniques is increased THD is likely to be decreases. Also some modulation techniques can be directly applied to multilevel inverters like NPC but modifications are required for implementing same technique to hybrid multilevel inverter.

The optimization in modulating signal as discussed in SFO-PWM only has the value to increase the available linear modulation region. While in PSC SFO PWM the zero sequence modification technique restricts its use to three phase three wire system, however it enables the modulation index to be increased by 15% before over modulation or pulse dropping occurs. Also the PSSUB- PWM is suitable for three-phase systems, as harmonics added are triplens and in three phase system triplens are missing. HLCCAPOPWM and alternative hybrid modulation techniques are related with PDPWM and THD obtained is not much low but it can be further improved by taking appropriate modulation index.

CHAPTER 4

SIMULATIONS RESULTS for MULTILEVEL INVERTER and HYBIRD MULTILEVEL INVERTER

In this chapter MATLAB simulations done for different cascaded multilevel inverters (CMLI) and hybrid multilevel inverters (HMLI) are described and analyzed. Simulations are carried out for 5 level, 7 level and 9 level output with respect to cascaded multilevel inverter. Different modulation techniques implemented are PD, POD, APOD and hybrid modulation technique. Modulation index is taken either 0.9 or 1 specified with respective output figures while frequency modulation index is 21. For better visualization figures are resolved, but simulations and THD measurement are done as per the values specified. Further sections describe MATLAB simulations for different MLI and HMLI.

4.1 SIMULATIONS FOR CASCADED MULTILEVEL INVERTER

As per the theory discussed in chapter 2 and chapter 3 simulations are carried out for different cascaded multilevel inverter and FFT analysis is done in MATLAB/SIMULINK to obtain THD.

4.1.1 FIVE LEVEL CASCADED MULTILEVEL INVERTER

As shown in Fig. 4.1 if two H bridges are cascaded then 5 level output is obtained. Though practically type of switches used do make difference in output but in simulations no major difference is observed.

4.1.1.1 Five Level Cascaded Multilevel Inverter with Staircase Technique

Fig. 4.1 shows block diagram structure in MATLAB/SIMULINK for 5 level cascaded MLI.

For all simulation results on Y-axis voltage in volts is taken and on X-axis time is taken in seconds.

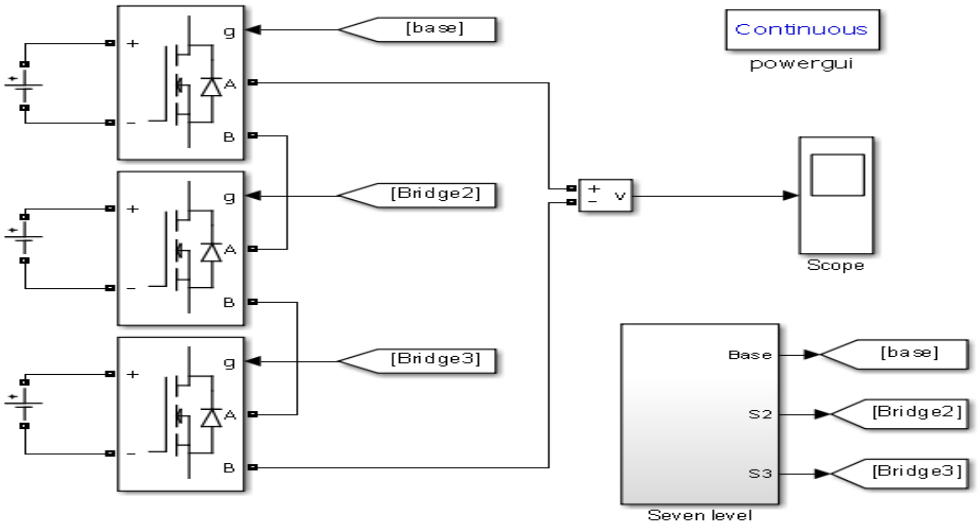


Fig. 4.1 Simulink block for cascaded multilevel inverter

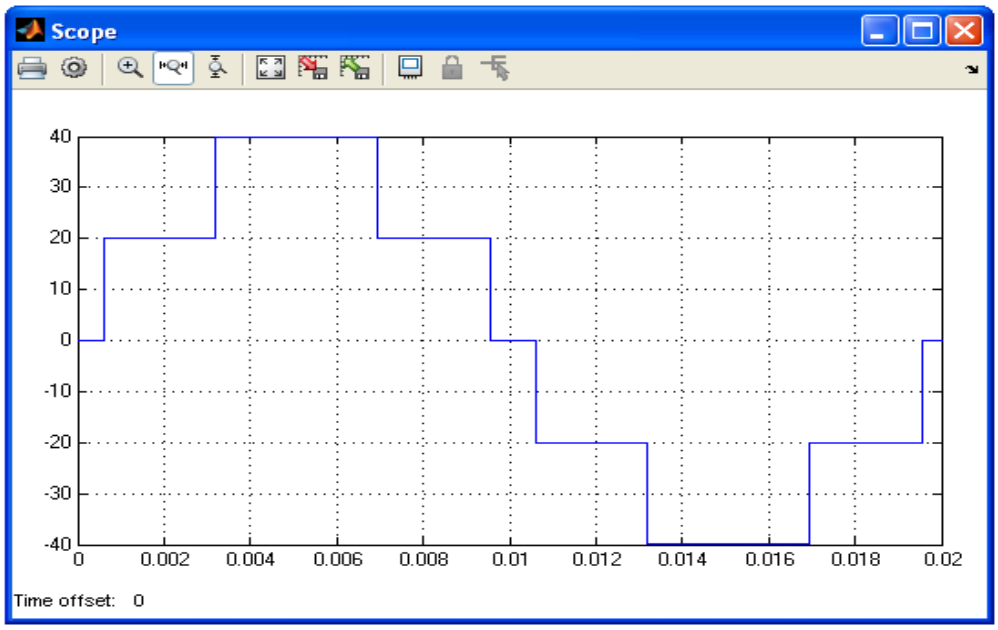


Fig. 4.2 Simulink output for five level cascaded multilevel inverter

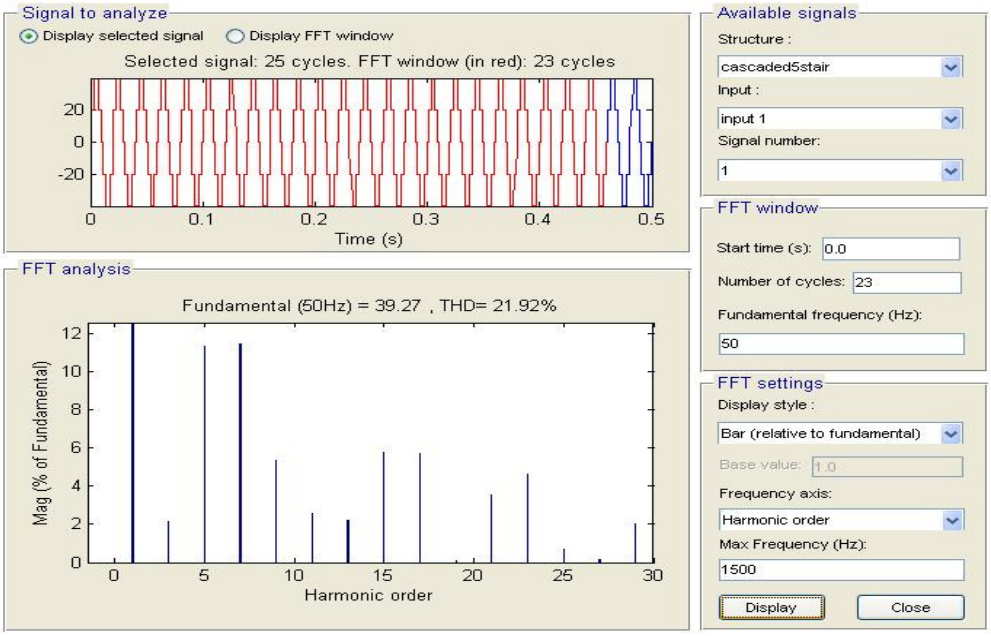


Fig. 4.3 FFT analysis and THD for five level cascaded multilevel inverter

In this simulation universal bridge simulink block is used in which MOSFET switch is chosen. Fig. 4.2 shows 5 level output voltage where V_{dc} is 20V for each bridge thus DC voltage is equal for both bridges. MOSFETs are switched at approximately 10^0 and 56^0 to obtain V_{dc} and $2V_{dc}$ as the output, accordingly rest of switching takes place. Switching angles can be obtained using different techniques such as selective harmonic elimination (SHE).

Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.3 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. FFT parameters remains same for all analysis unless and until specified.

4.1.1.2 Five Level Cascaded Multilevel Inverter with Phase Disposition Modulation Technique

Block diagram structure for 5 level cascaded MLI with PD modulation technique remains same as Fig. 4.1. Control block is changed as shown in Fig. 4.4 where 'g1'-'g2' combine to give 'A' and 'g5'-'g6' combine to give 'A1' in Fig. 4.1. Fig. 4.5 shows carrier and modulating signal for PD modulation technique for five level cascaded MLI. Modulation index is specified earlier. Fig. 4.6 shows 5 level output voltage where V_{dc} is 20V for each bridge. Thus DC voltage is equal for both bridges. Thus output can be changed with different modulation index for amplitude and frequency hence THD will change accordingly. Fig. 4.7 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. FFT parameters remains same for all analysis unless and until specified.

Similar outputs can be obtained for POD and APOD modulation technique.

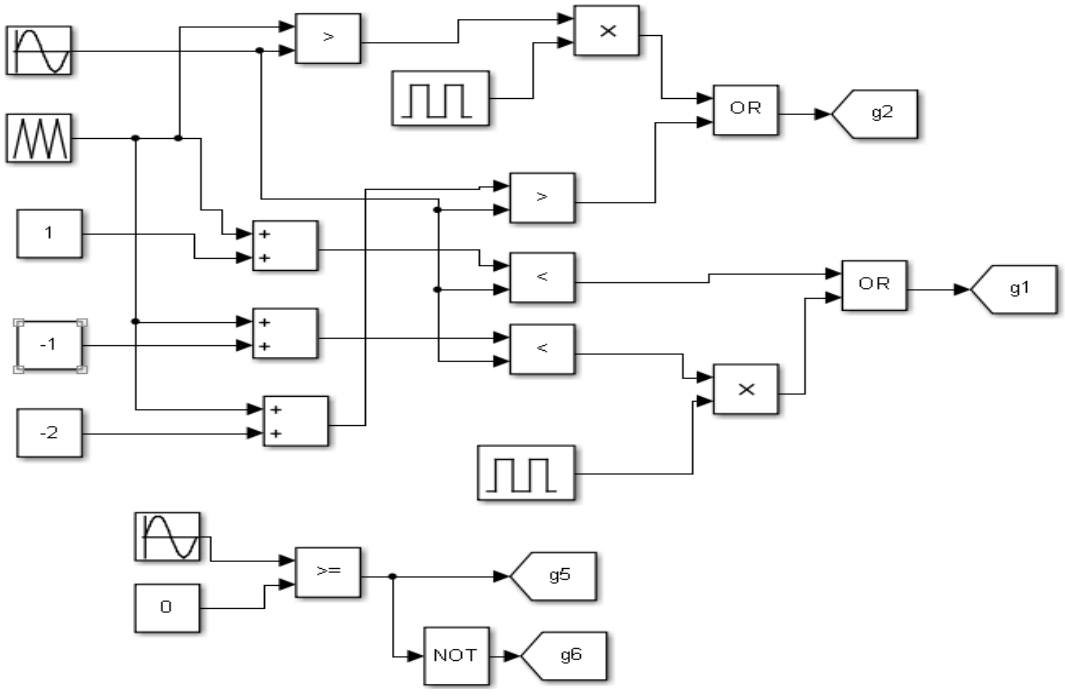


Fig. 4.4 Control block for five level cascaded MLI with PD technique

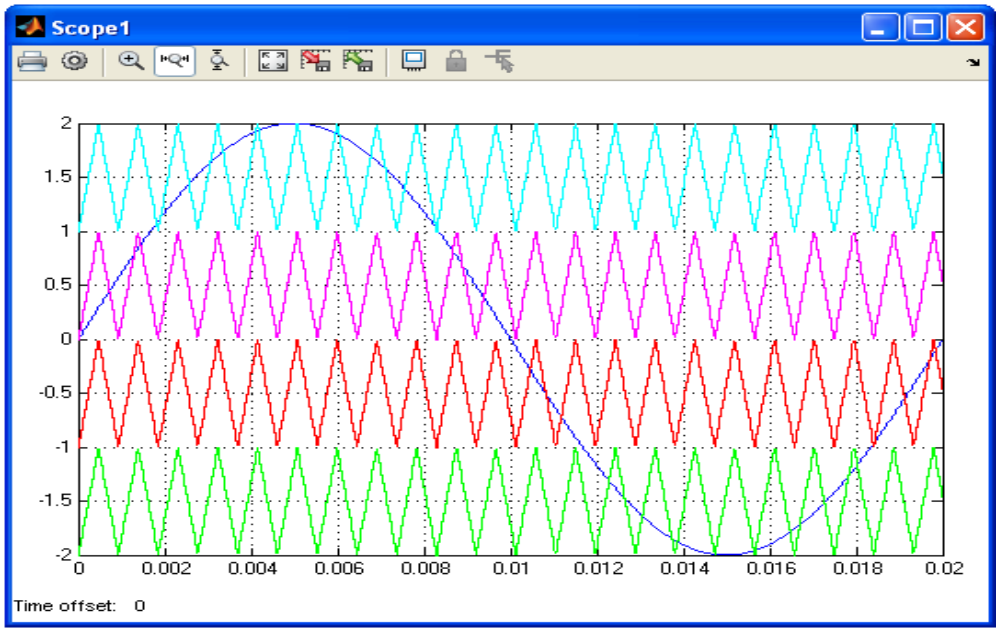


Fig. 4.5 Carrier and modulating signal for five level cascaded MLI with PD technique

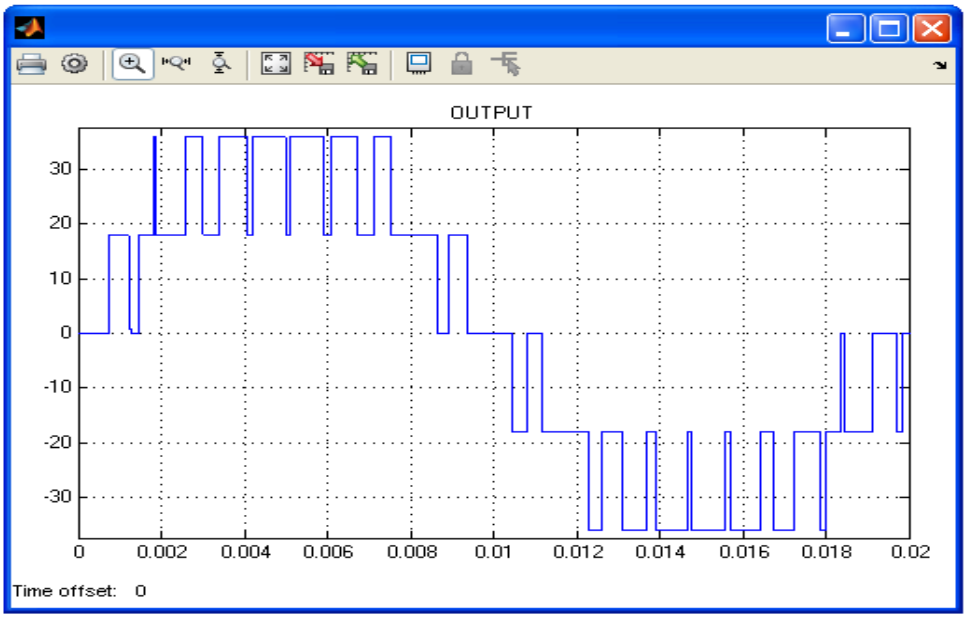


Fig. 4.6 Simulink output for five level cascaded multilevel inverter with PD technique

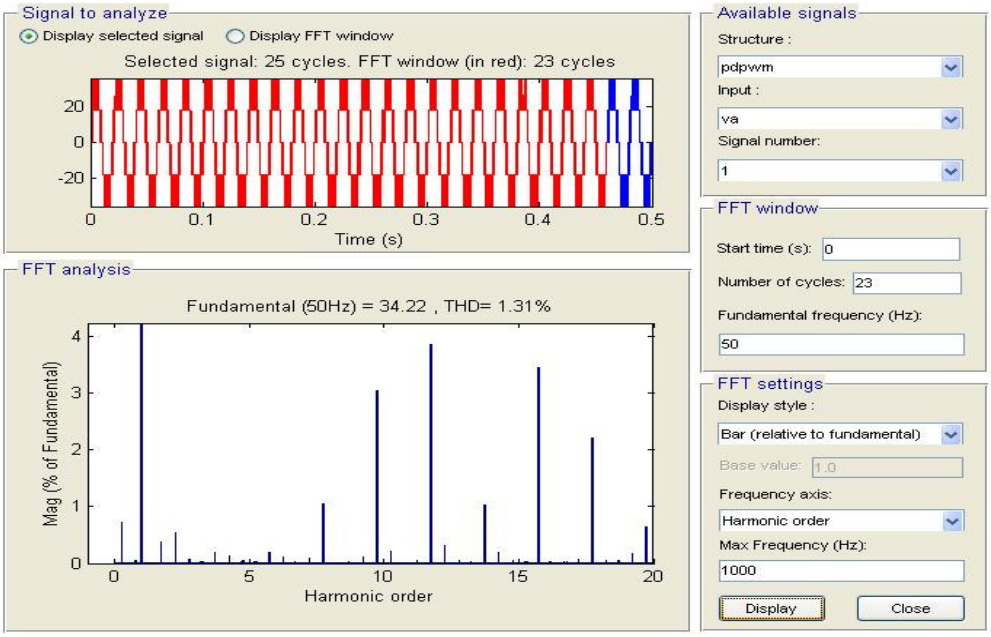


Fig. 4.7 FFT analysis and THD for five level cascaded multilevel inverter with PD technique

4.1.2 SEVEN LEVEL CASCADED MULTILEVEL INVERTER

Seven level output can be obtained using two or three H bridges by varying V_{dc} as per requirement.

4.1.2.1 Seven Level Cascaded Multilevel Inverter with Staircase Technique Using Three H Bridges

A) Using three bridges

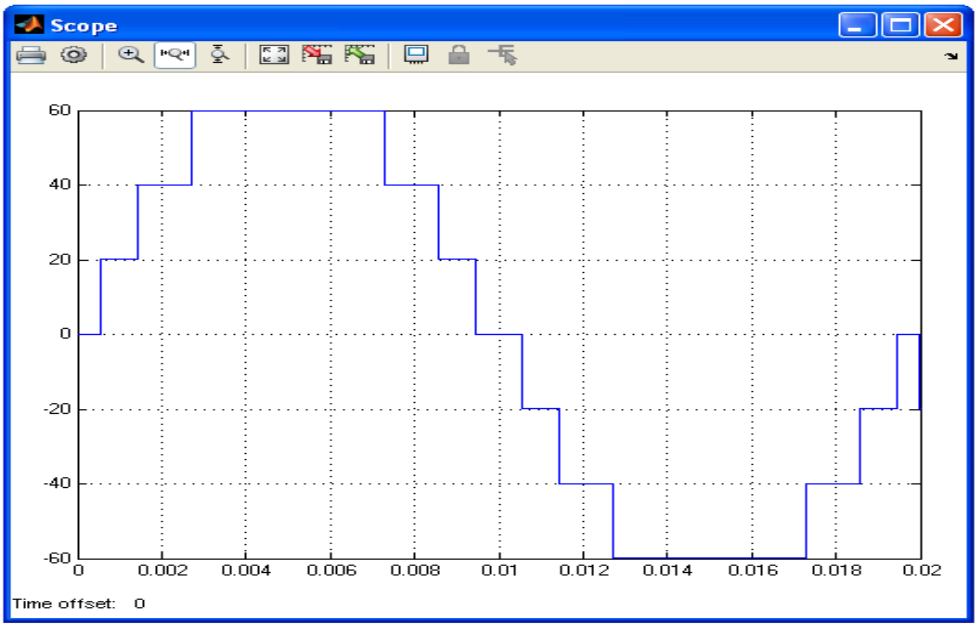


Fig. 4.8 Simulink output for seven level CMLI using three H bridges

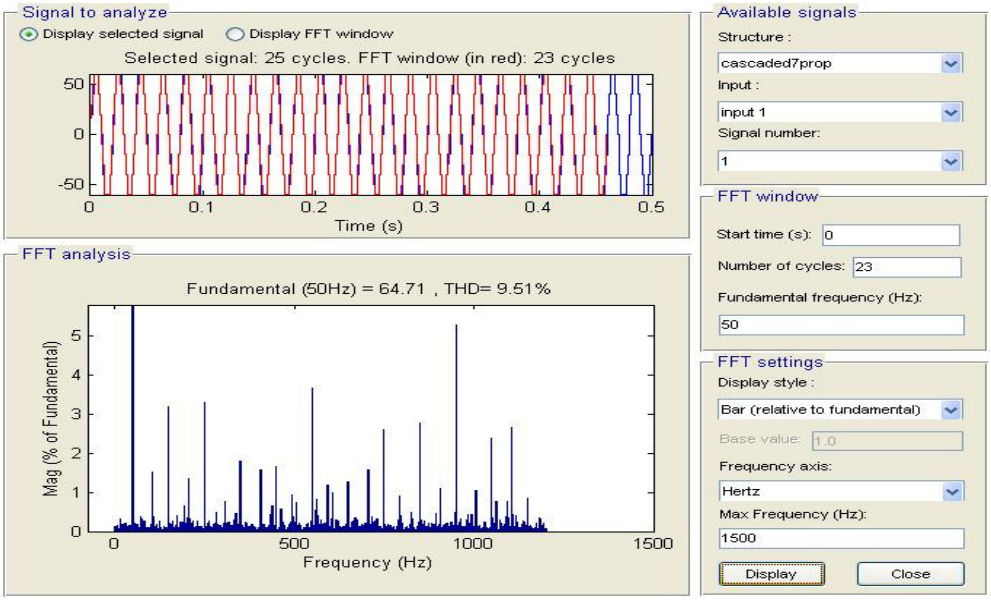


Fig. 4.9 FFT analysis and THD for seven level CMLI for specified angles

Block diagram structure for 7 level cascaded MLI with three H bridges is shown in Fig. 4.1. Switches are switched at approximately 10^0, 26^0 and 49^0 to obtain V_{dc}, $2V_{dc}$ and $3V_{dc}$ and accordingly rest of switching takes place. Fig. 4.8 shows 7 level output voltage where V_{dc} is 20V for each bridge thus DC voltage is equal for all bridges. Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.9 corresponds to FFT analysis giving THD at 23^{rd} cycle with 1500 Hz as maximum frequency.

B) Using two bridges

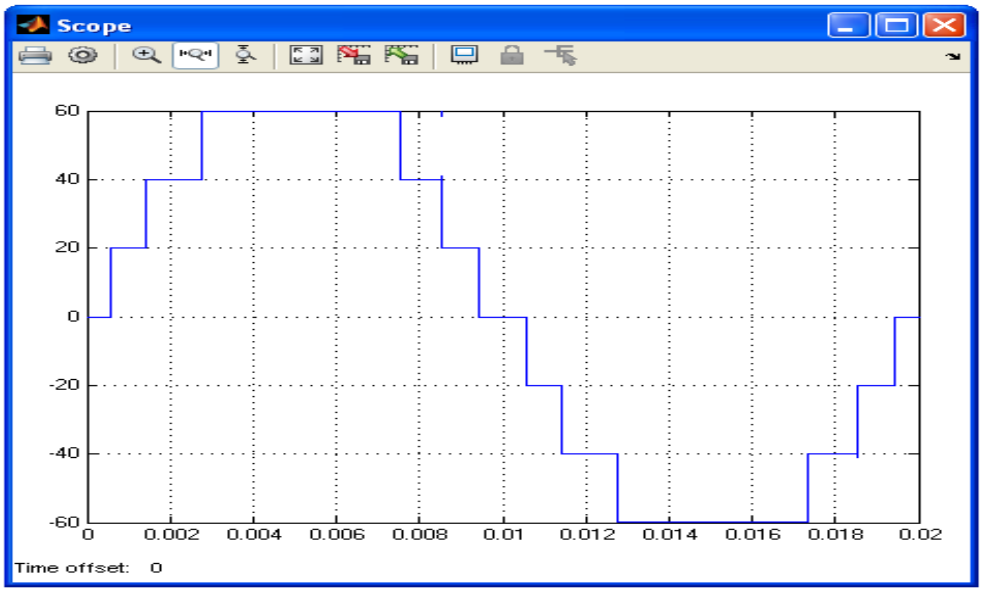


Fig. 4.10 Simulink output for 7 level CMLI using 2 H bridges

Seven level cascaded MLI with two H bridges can be obtained by removing one H bridge from Fig. 4.1 and changing DC voltages to V_{dc} and $2V_{dc}$. Switches are switched at approximately 10^0, 26^0 and 49^0 to obtain V_{dc}, $2V_{dc}$ and 3 V_{dc} and accordingly rest of switching takes place. Fig. 4.10 shows 7 level output voltage where V_{dc} is unequal for H bridges. Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.11 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

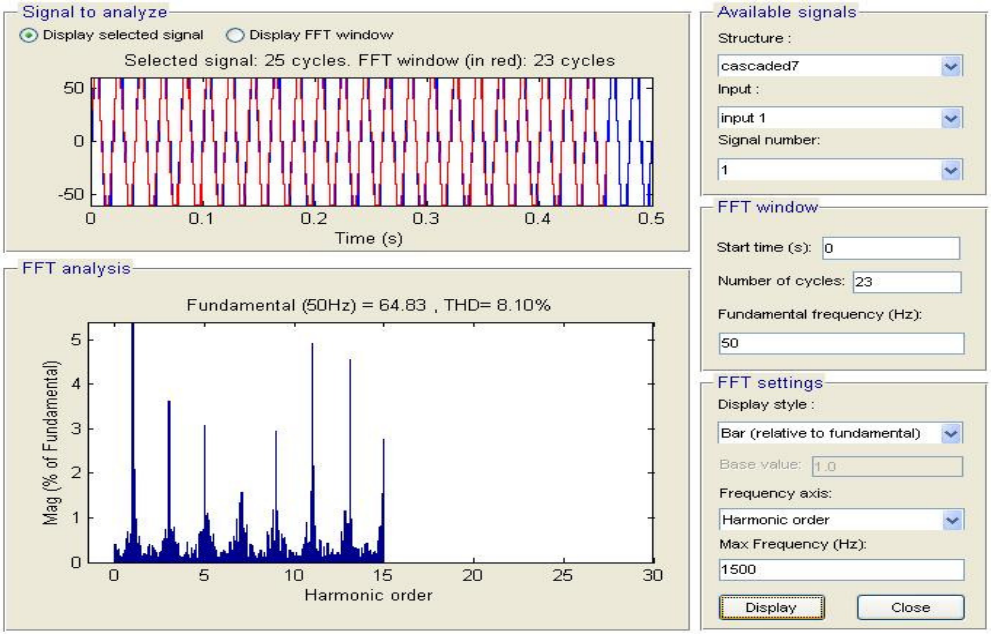


Fig. 4.11 FFT analysis and THD for 7 level CMLI for specified angles

4.1.2.2 Seven Level Cascaded Multilevel Inverter with Phase Disposition Modulation Technique

A) Using three bridges

Block diagram structure for 7 level cascaded MLI with PD modulation technique remains same as Fig. 4.1. Control block will consist of carrier and modulating signal for PD technique with number of carriers increased to six as output is having seven levels As shown in Fig. 4.5 number of carriers is increased while modulating signal is same. Modulation index is specified earlier. Fig. 4.12 shows 7 level output voltage where V_{dc} is 20V for each bridge, the DC voltage is equal for all bridges. Thus output can be changed with different modulation index for amplitude and frequency hence THD will change accordingly. Fig. 4.13 corresponds to FFT analysis giving THD at 23rd cycle with 1000 Hz as maximum frequency. FFT parameters remains same for all analysis unless and until specified.

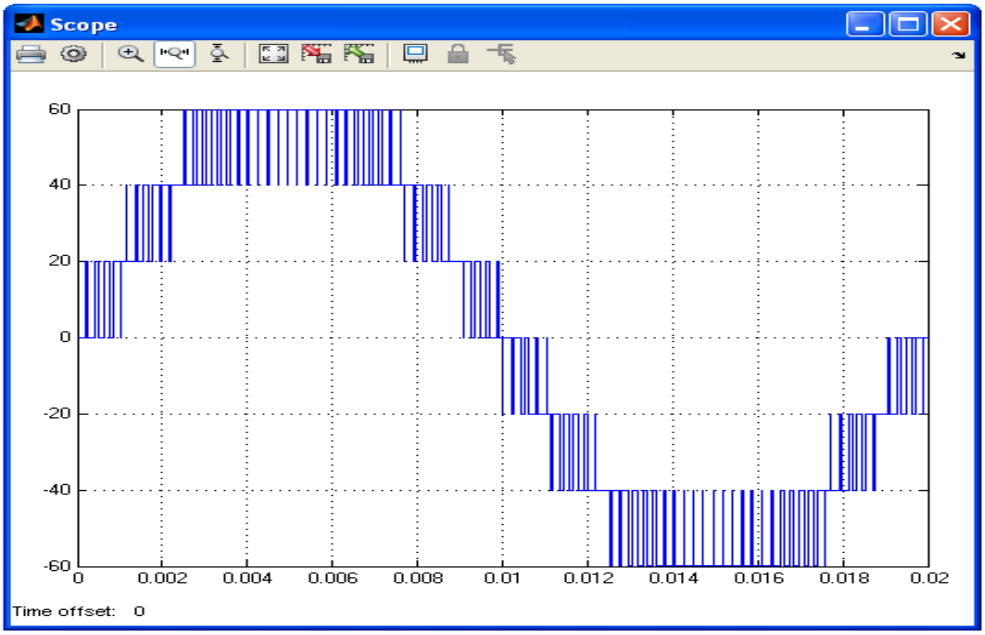


Fig. 4.12 Simulink output for 7 level CMLI with PD technique

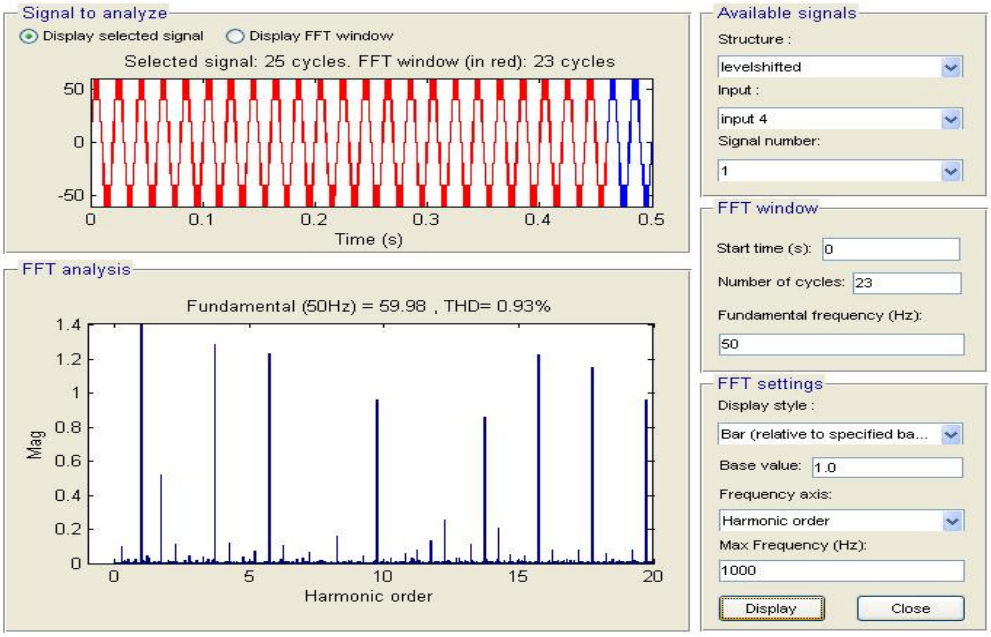


Fig. 4.13 FFT analysis and THD for seven level cascaded multilevel inverter with PD technique

Similar outputs can be obtained for POD and APOD modulation technique as shown in Fig. 4.14 and Fig. 4.15 respectively.

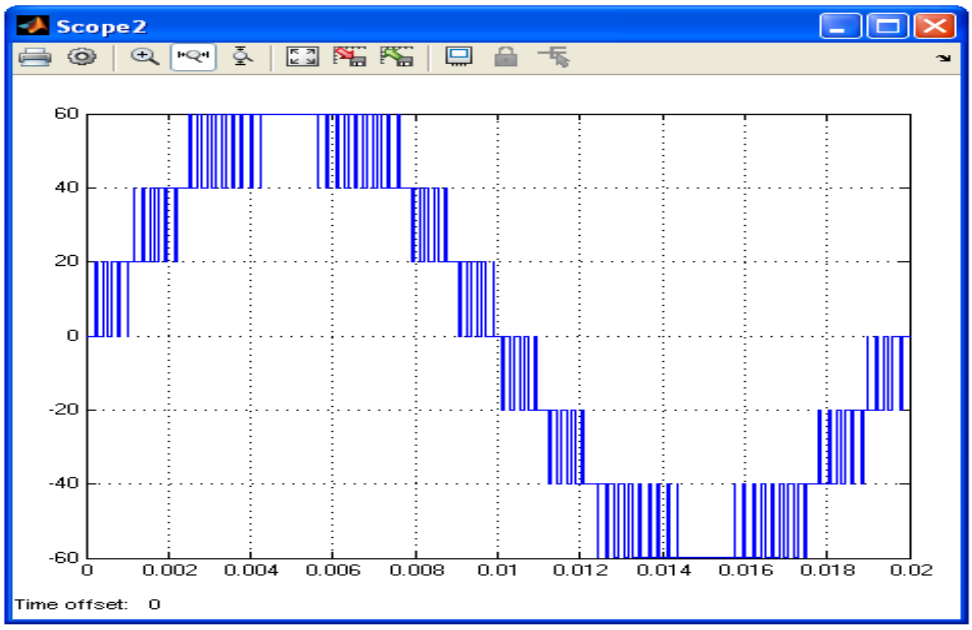


Fig. 4.14 Simulink output for 7 level CMLI with POD technique

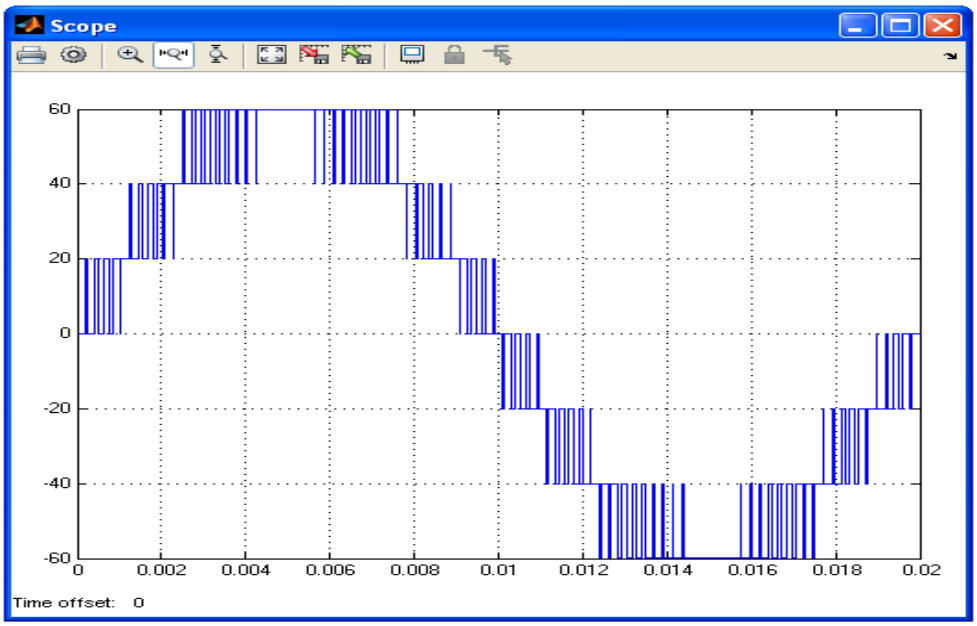


Fig. 4.15 Simulink output for 7 level CMLI with APOD technique

4.1.3 NINE LEVEL CASCADED MULTILEVEL INVERTER

Nine level output can be obtained by using two or four H bridges by varying V_{dc} as per requirement.

4.1.3.1 Nine Level Cascaded Multilevel Inverter with Staircase Technique Using Three H Bridges

A) Using four bridges

Switches are switched at approximately 7.5^0, 19.1^0, 33.5^0 and 51.6^0 to obtain V_{dc}, $2V_{dc}$, $3V_{dc}$ and $4V_{dc}$ and accordingly rest of switching takes place. Fig. 4.16 shows 9

level output voltage where V_{dc} is 20V for each bridge thus DC voltage is equal for all bridges. Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.17 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

Block diagram structure for 9 level CMLI with four H bridges can be obtained by adding one H bridge Fig. 4.1.

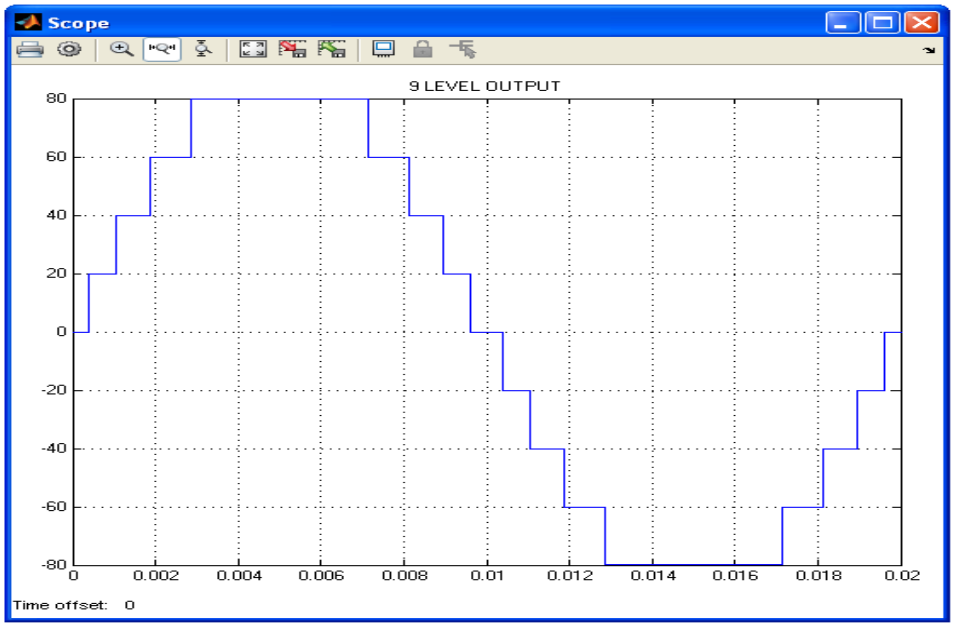


Fig. 4.16 Simulink output for 9 level CMLI for 4 H bridges

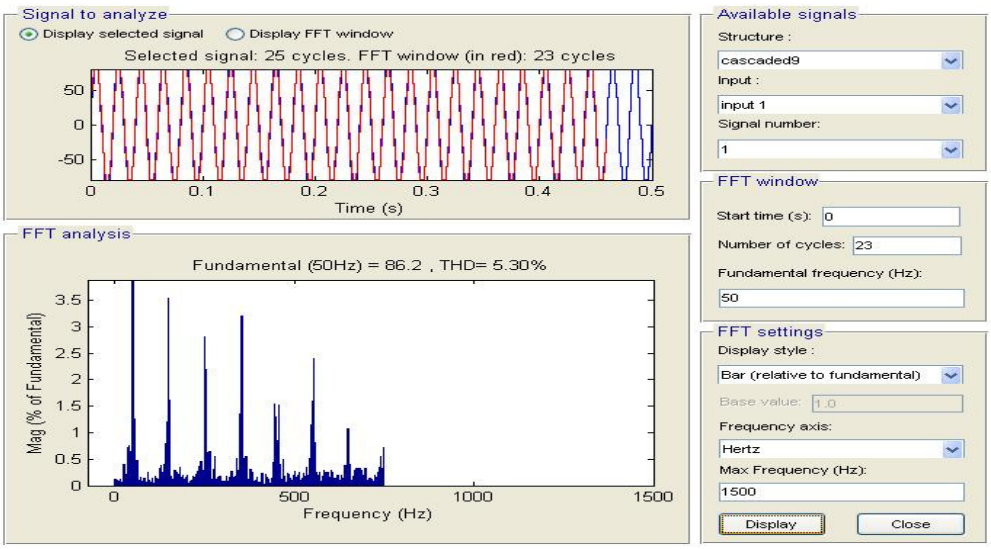


Fig. 4.17 FFT analysis and THD for 9 level CMLI for specified angles

B) Using two bridges

Nine level cascaded MLI with two H bridges can be obtained by removing one

H bridge from Fig. 4.1 and changing DC voltages to V_{dc} and $3V_{dc}$.

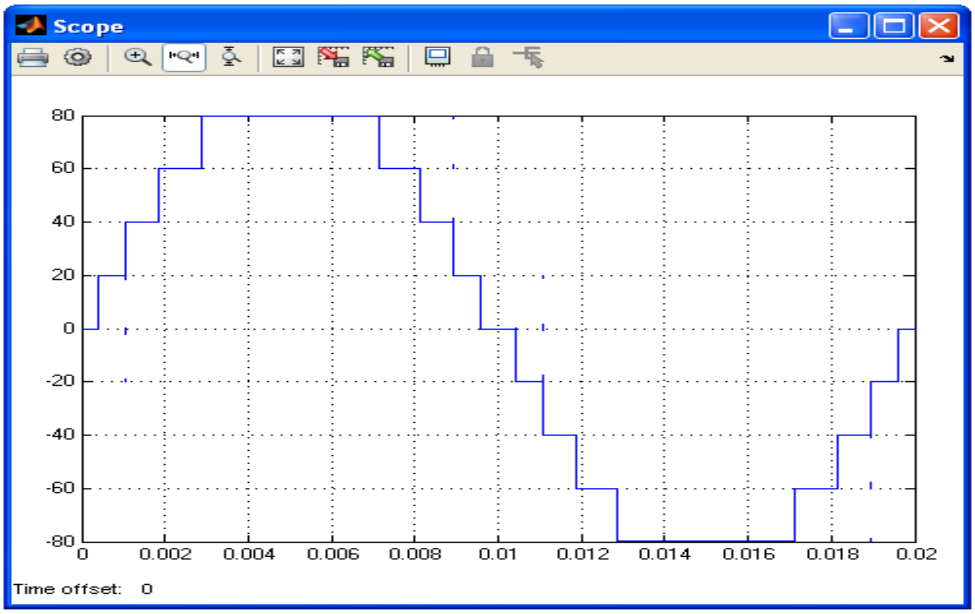


Fig. 4.18 Simulink output for nine level cascaded multilevel inverter for 2 H bridges

Switches are switched at approximately 7.5^0, 19.1^0, 33.5^0 and 51.6^0 to obtain 0, V_{dc}, $2V_{dc}$ and $3V_{dc}$ and accordingly rest of switching takes place. Fig. 4.18 shows 9 level output voltage where output levels are obtained by addition or subtraction of applied DC voltage i.e. 10V and 30V. Thus output can be optimized with different switching angles and accordingly THD will change. Fig. 4.19 corresponds to FFT analysis giving THD at 23^{rd} cycle with 1500 Hz as maximum frequency.

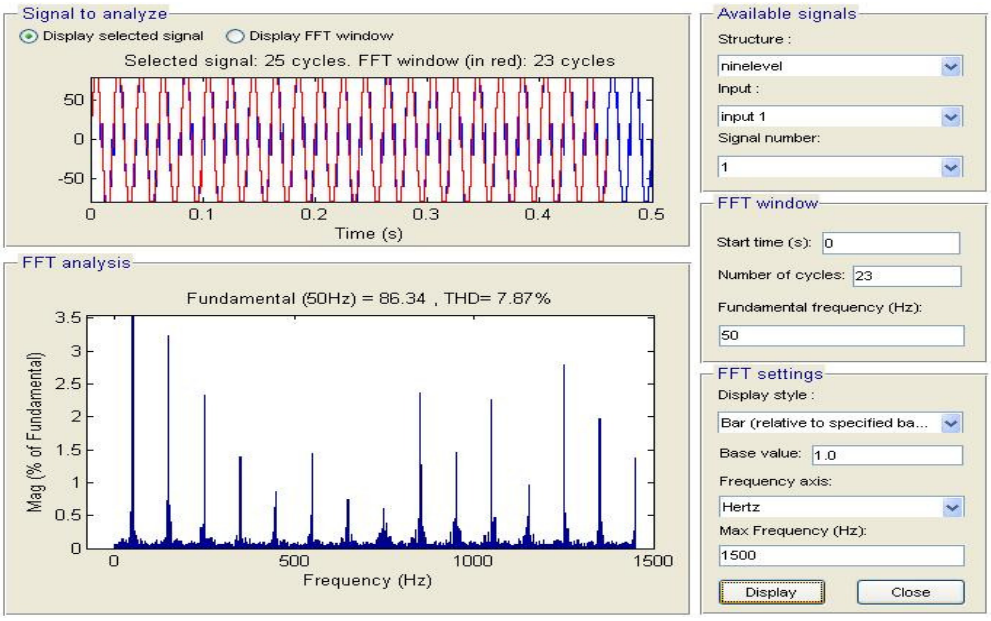


Fig. 4.19 FFT analysis and THD for 9 level CMLI for specified angles

4.2 SIMULATIONS FOR HYBRID MULTILEVEL INVERTER

As per the theory discussed in chapter 2 and chapter 3 simulations are carried out for different hybrid multilevel inverters and FFT analysis is done in MATLAB/SIMULINK to obtain THD.

4.2.1 ASYMMETRIC HYBRID MULTILEVEL INVERTER

As shown in Fig. 4.24 IGBT H bridge is cascaded with GTO H bridge thus giving asymmetric topology with respect to power devices, but in simulations no major difference is observed as compared to cascaded multilevel inverter with same type of power devices.

4.2.1.1 Single Phase Asymmetric Hybrid Multilevel Inverter with Hybrid Modulation Technique

A) Equal DC sources

Fig. 4.20 shows block diagram structure in MATLAB/SIMULINK for asymmetric hybrid multilevel inverter with equal DC sources. Fig. 4.21 is control block and Fig. 4.22 control signals for IGBT and GTO bridge. As per Fig. 4.22 it is observed that GTO H-bridge is switched at low frequency while IGBT bridge is switched at high frequency.

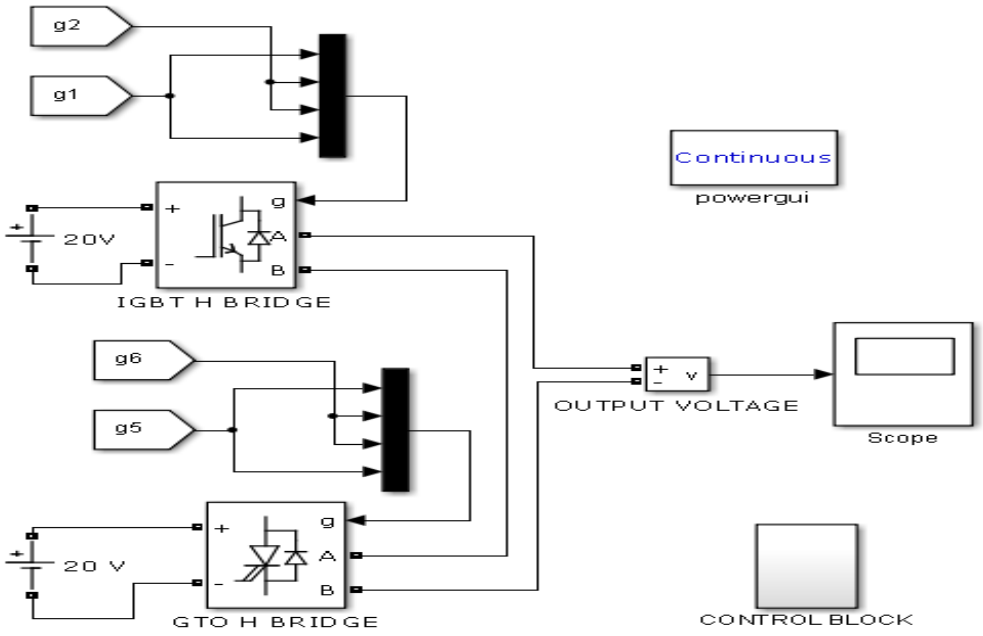


Fig. 4.20 Simulink block for single phase asymmetric hybrid multilevel inverter

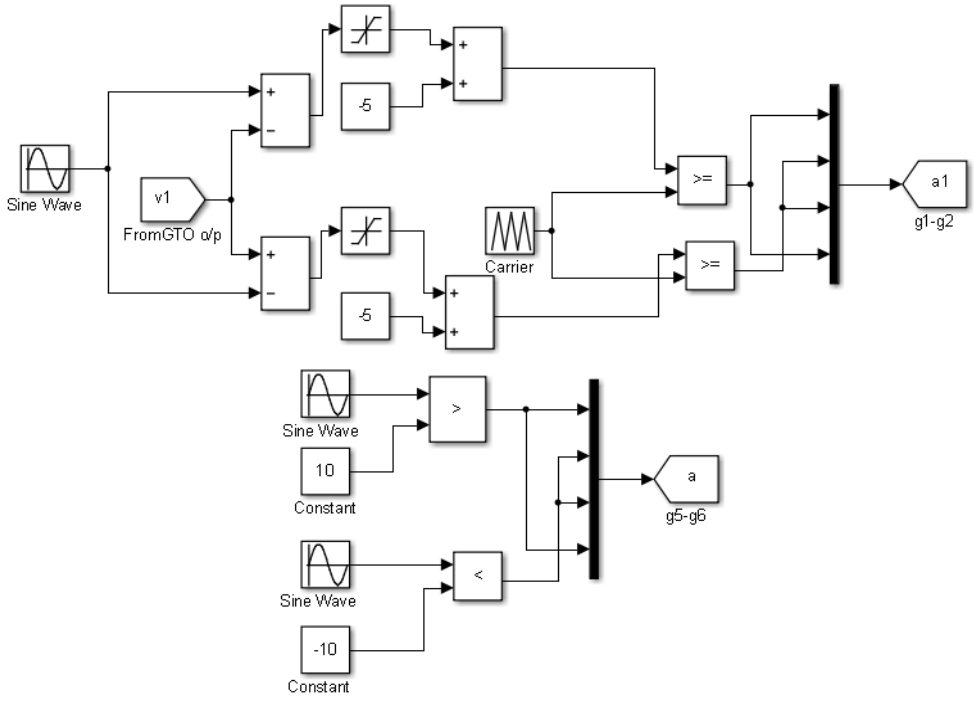


Fig. 4.21 Control block for single phase asymmetric hybrid multilevel inverter with hybrid modulation technique

As DC voltages sources are equal output is five level output as shown in Fig. 4.23. Fig. 4.24 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. FFT parameters remains same for all analysis unless and until specified.

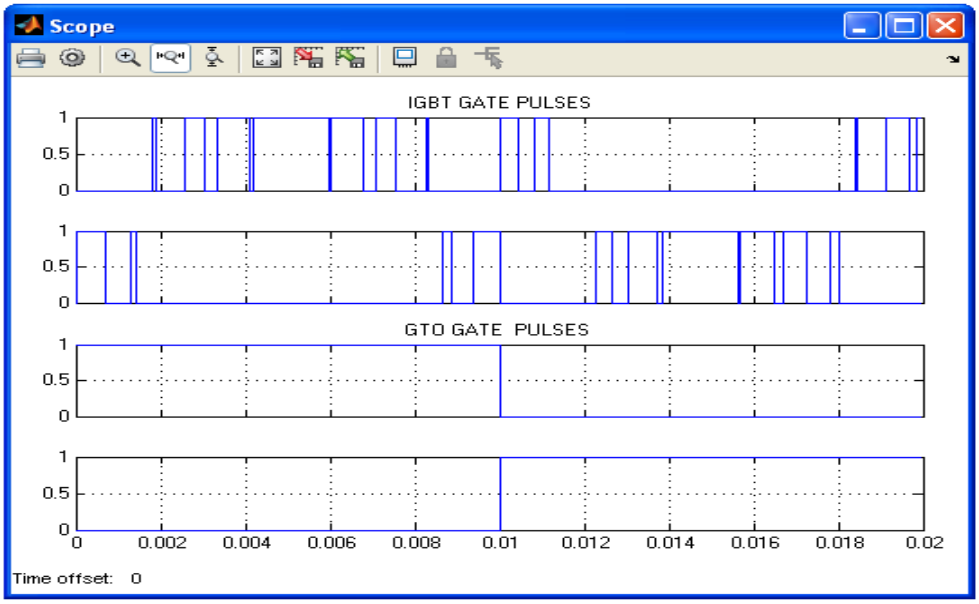


Fig. 4.22 Control signals for asymmetric hybrid multilevel inverter

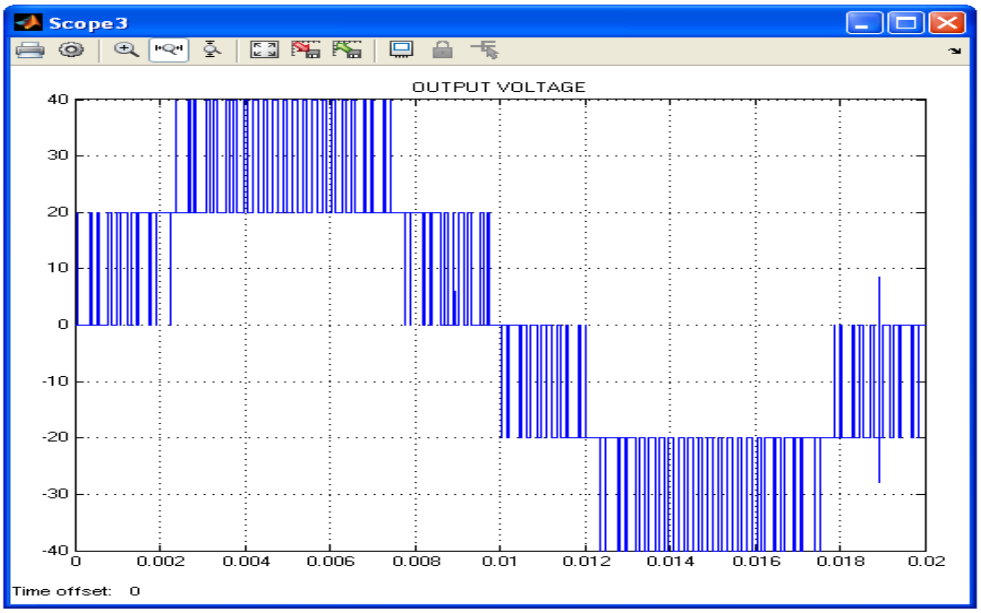


Fig. 4.23 Simulink output for single phase asymmetric multilevel inverter with hybrid modulation technique for equal DC sources

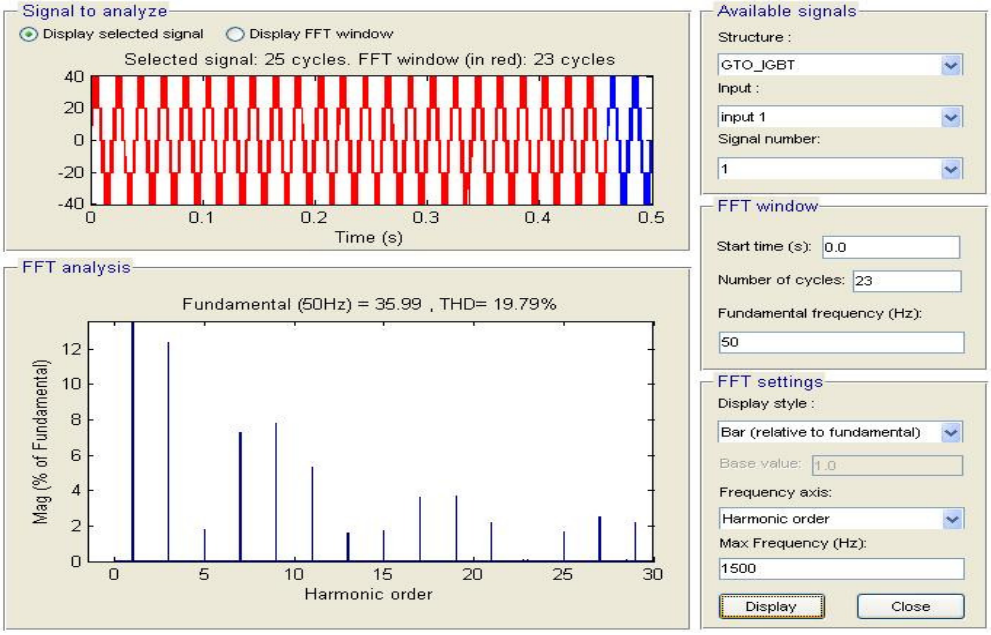


Fig. 4.24 FFT analysis and THD for asymmetric hybrid multilevel inverter with hybrid modulation technique for equal DC sources

B) Unequal DC sources

Asymmetric hybrid multilevel inverter with unequal DC sources is obtained by changing DC sources in Fig. 4.21 as 10V for IGBT H bridge and 20V for GTO H bridge. Control signals are same as shown in Fig. 4.22. As DC voltages sources are unequal output is seven level output as shown in Fig. 4.25. Fig. 4.26 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. FFT parameters remains same

for all analysis unless and until specified. It is observed that if DC voltage value is increased like 100V or more THD remains unchanged in simulation

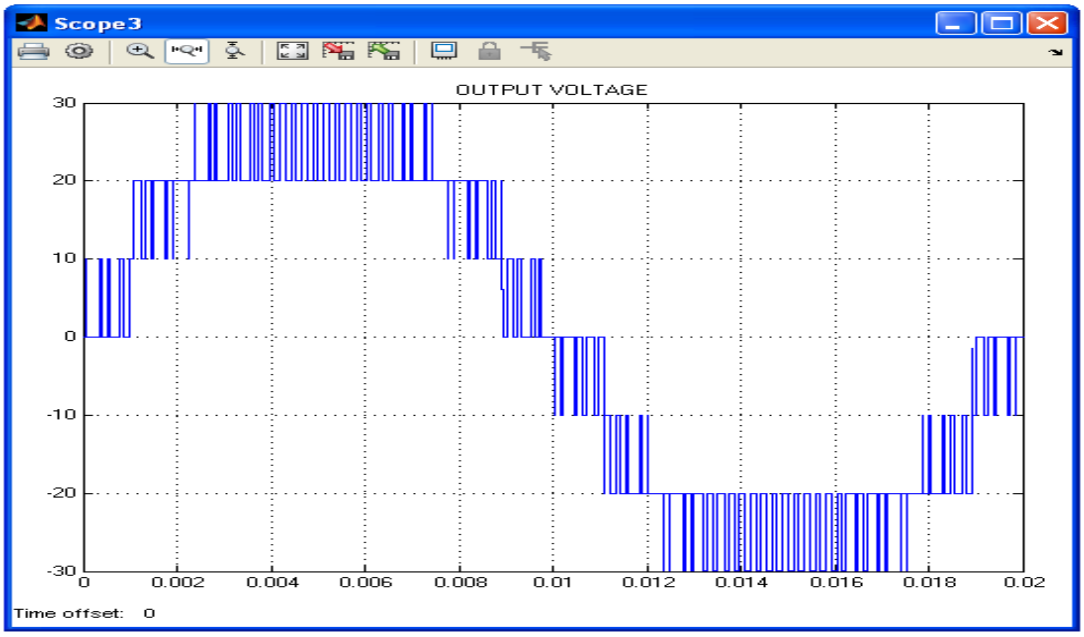


Fig. 4.25 Simulink output for single phase asymmetric multilevel inverter with hybrid modulation technique for unequal DC sources.

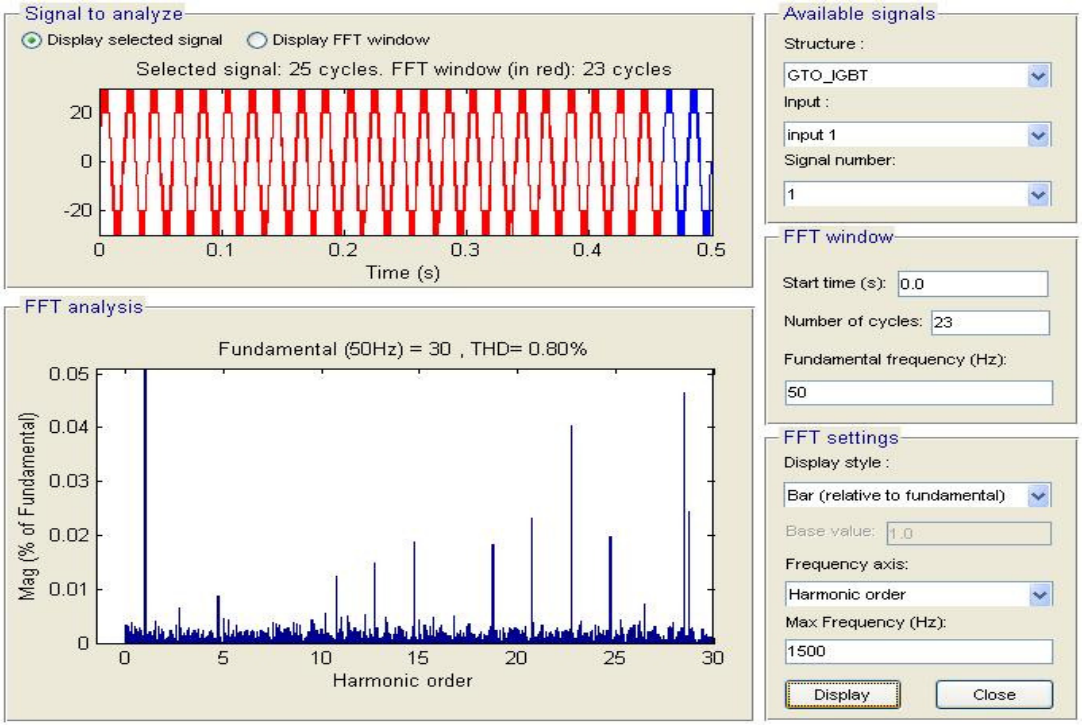


Fig. 4.26 FFT analysis and THD for asymmetric hybrid multilevel inverter with hybrid modulation technique for unequal DC sources

4.2.1.2 Single Phase Asymmetric Hybrid Multilevel Inverter with Phase Disposition Modulation Technique

A) Equal DC sources

Fig. 4.27 shows the output for single phase asymmetric hybrid multilevel inverter with phase disposition modulation technique and equal DC sources which is equal to 20V. Thus five level output is obtained. While Fig. 4.28 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

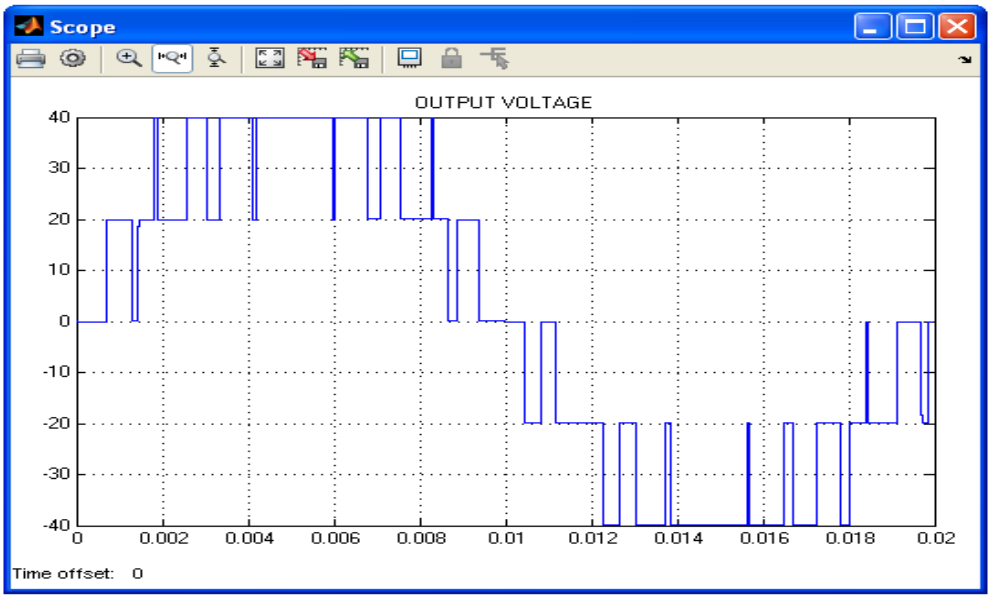


Fig. 4.27 Simulink output for single phase asymmetric multilevel inverter with PD technique for equal voltages

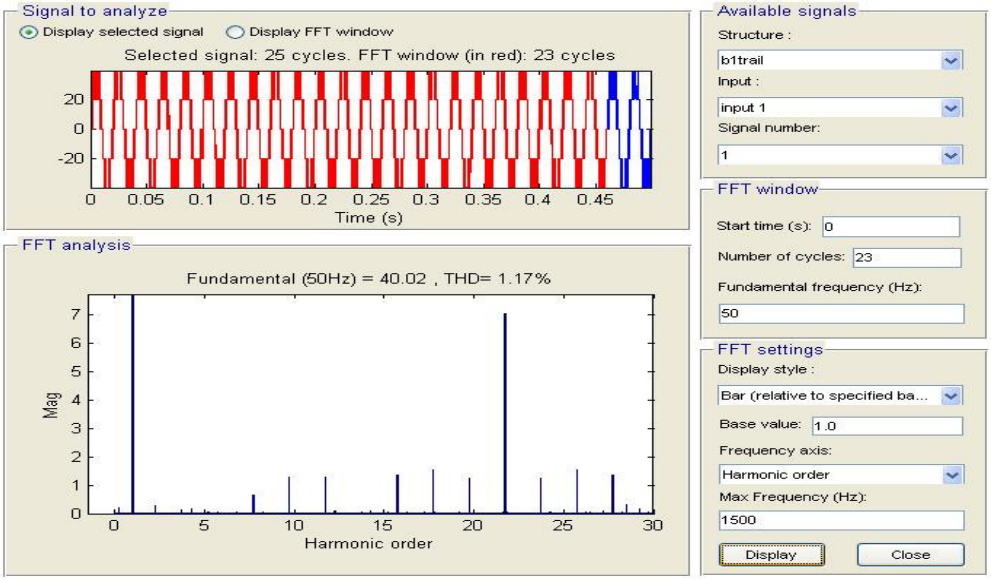


Fig. 4.28 FFT analysis and THD for asymmetric hybrid multilevel inverter with PD modulation technique for equal DC sources

4.2.1.3 Three Phase Asymmetric Hybrid Multilevel Inverter with Hybrid Modulation Technique

A) Equal DC sources

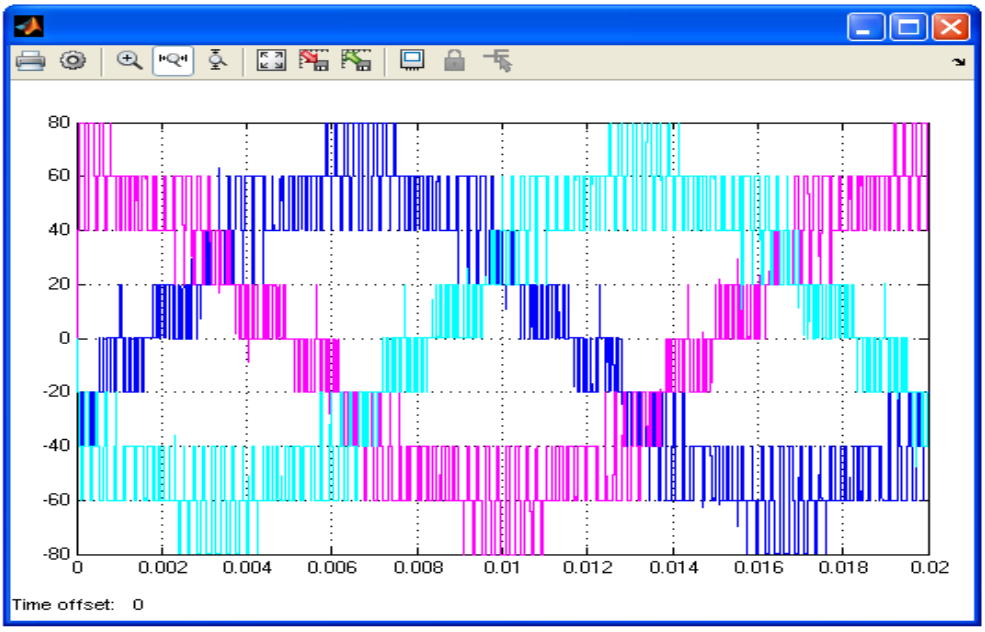


Fig. 4.29 Simulink output for three phase asymmetric hybrid multilevel inverter hybrid modulation technique with equal voltages

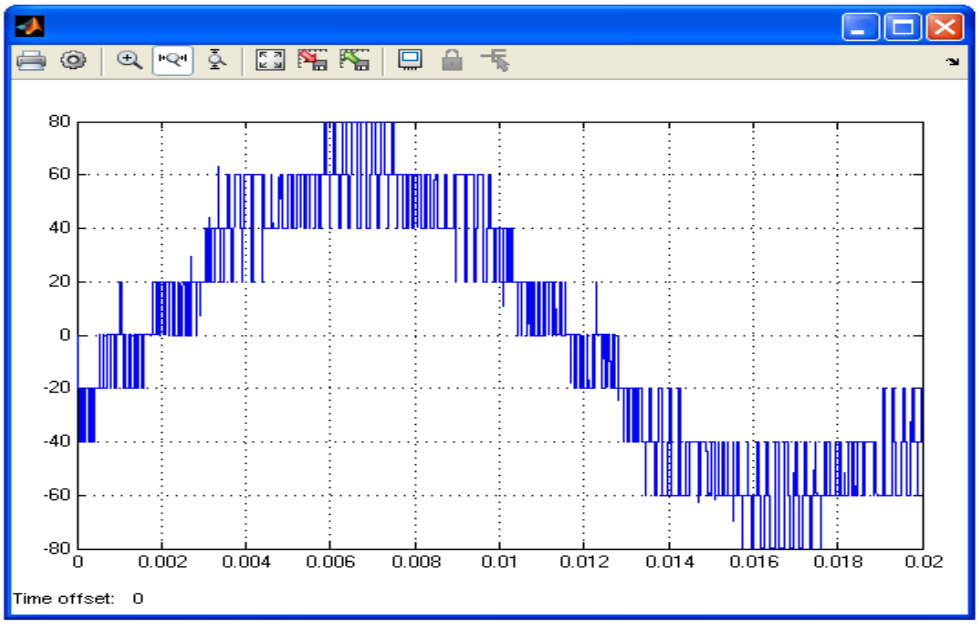


Fig. 4.30 One phase output from three phase asymmetric hybrid multilevel inverter hybrid modulation technique with equal voltages

Fig. 4.29 shows the output for three phase asymmetric hybrid multilevel inverter with hybrid modulation technique and equal DC sources where voltage is 20V. In three phase control signals are phase shifted by 120^0. Fig. 4.30 shows nine level output for single leg of three phase asymmetric hybrid multilevel inverter. While Fig.4.31

corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

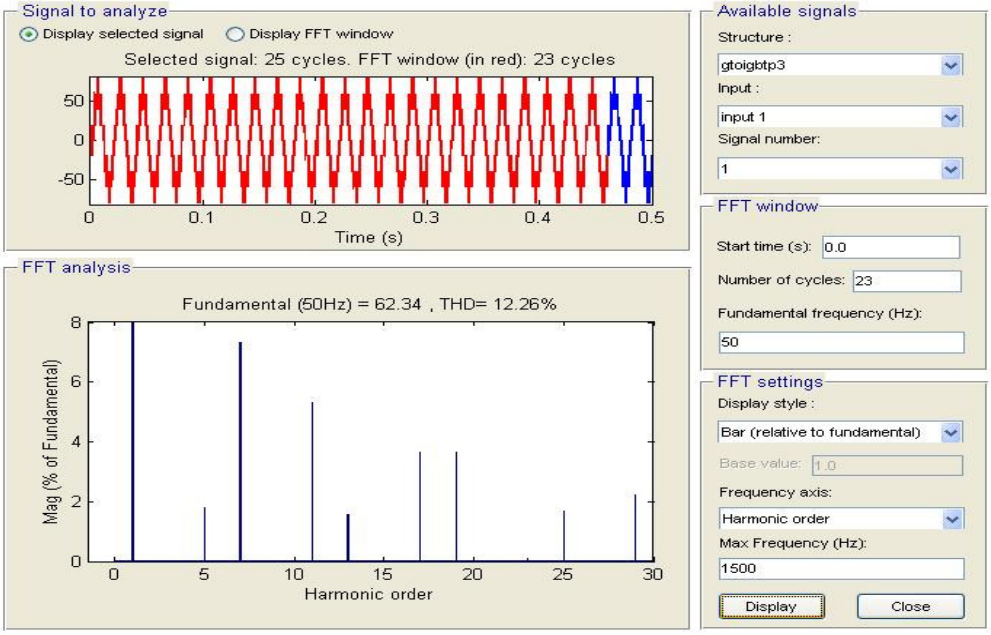


Fig. 4.31 FFT analysis and THD for three phase asymmetric hybrid multilevel inverter with hybrid modulation technique for equal DC sources

B) Unequal DC sources

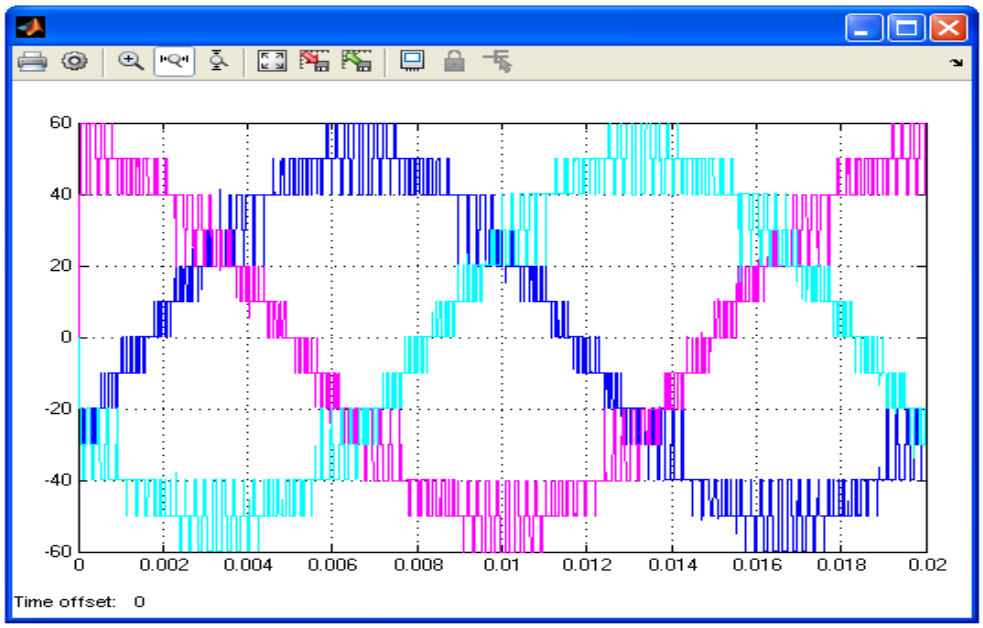


Fig. 4.32 Simulink output for three phase asymmetric hybrid multilevel inverter hybrid modulation technique with unequal DC sources

Three phase asymmetric hybrid multilevel inverter with unequal DC sources with hybrid modulation technique output is shown in Fig. 4.32 with DC sources as 10V for

IGBT bridges and 20V for GTO bridges. Control signals are phase shifted by 120^0. As DC voltages sources are unequal output is thirteen level as shown in Fig. 4.33. Fig. 4.34 corresponds to FFT analysis giving THD at 23^{rd} cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

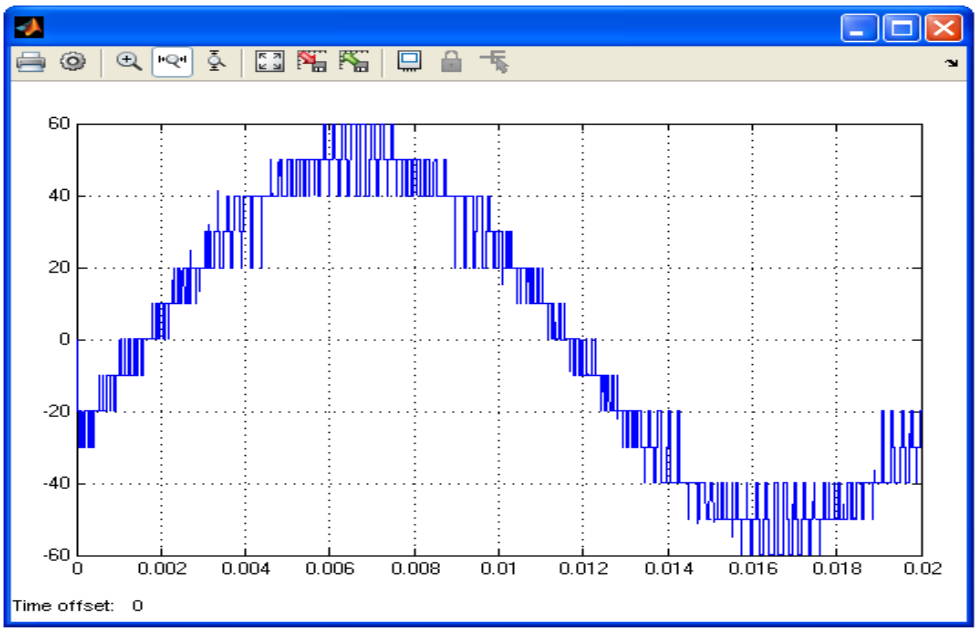


Fig. 4.33 One phase output from three phase asymmetric hybrid multilevel inverter hybrid modulation technique with unequal DC sources

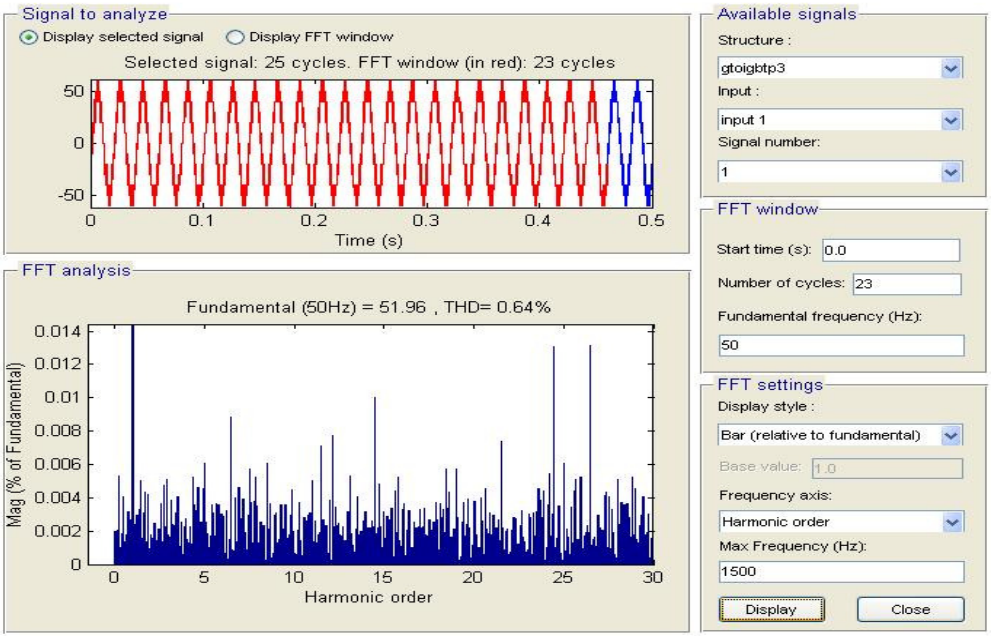


Fig. 4.34 FFT analysis and THD for three phase asymmetric hybrid multilevel inverter with hybrid modulation technique for unequal DC sources

4.2.2 SYMMETRICAL HYBRID MULTILEVEL INVERTER

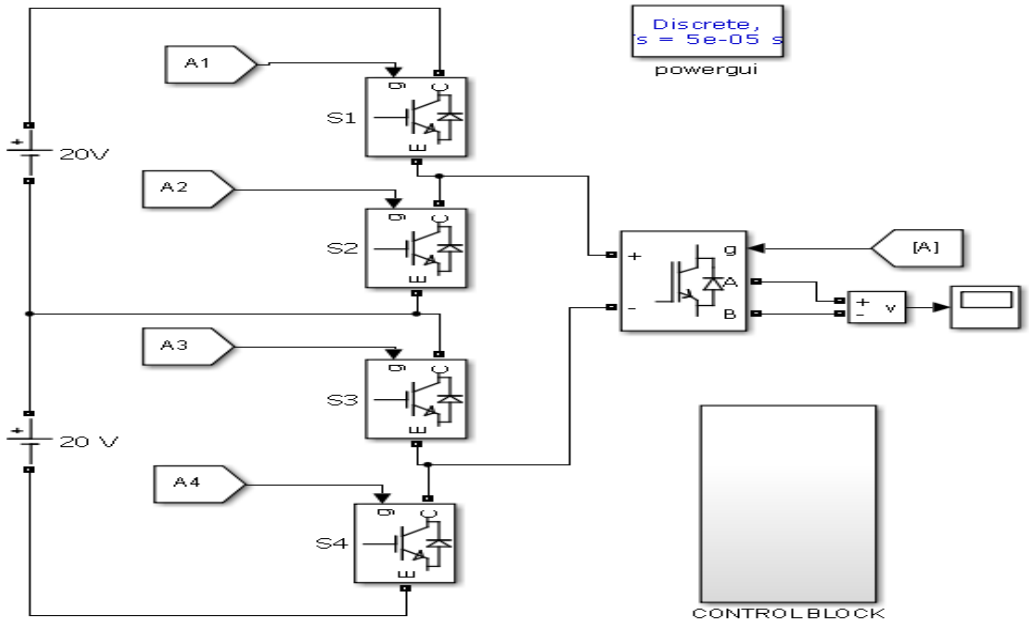


Fig. 4.35 Simulink block for five level symmetric hybrid multilevel inverter

Block diagram structure for symmetrical hybrid multilevel inverter is shown in Fig. 4.35.DC voltage sources are equal. As per switching pattern discussed in chapter 2 simulations are done.

4.2.2.1 Symmetrical Hybrid Multilevel Inverter with Staircase Technique

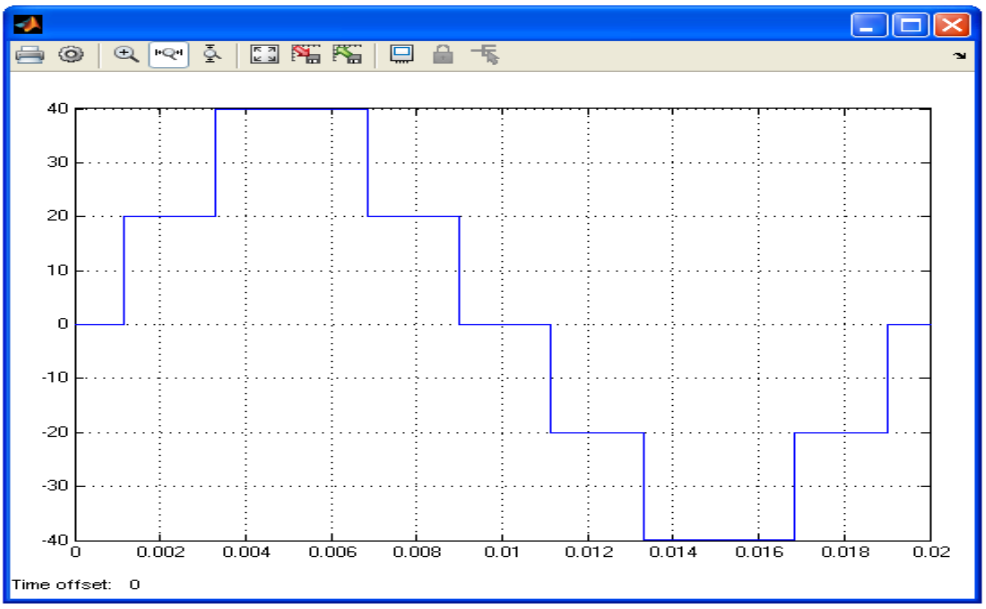


Fig. 4.36 Simulink output for five level symmetric multilevel inverter

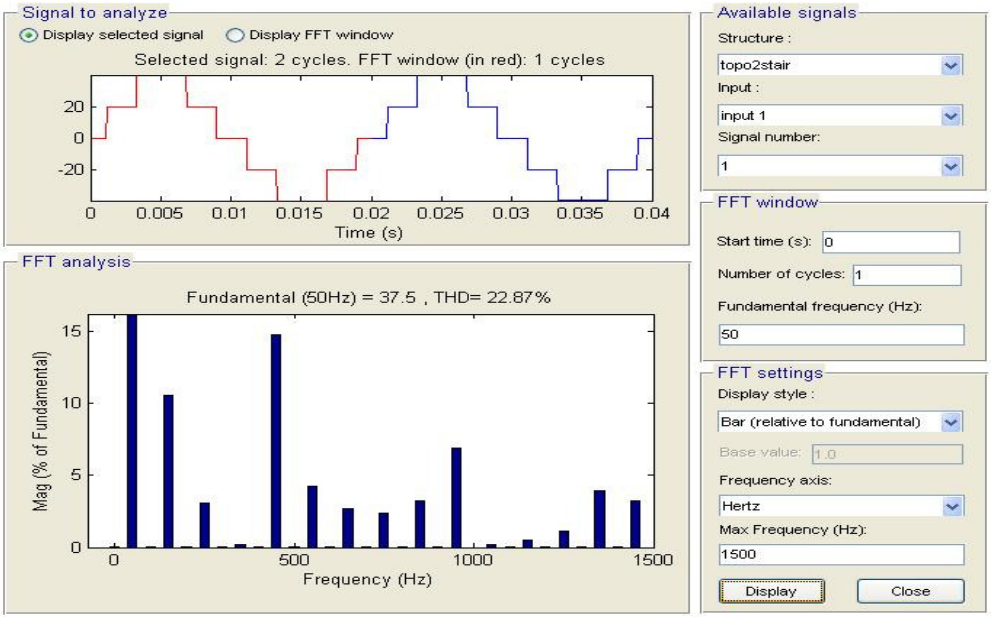


Fig. 4.37 FFT analysis and THD for single phase symmetrical hybrid multilevel inverter with staircase technique

In symmetrical hybrid multilevel inverter switches are switched at approximately 20^0 and 58^0 to obtain 5 level output as shown in Fig. 4.36. To optimize output with different switching angles can be applied and accordingly THD changes. Fig. 4.37 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

4.2.2.2 Single Phase Symmetrical Hybrid Multilevel Inverter with Phase Shift Modulation Technique

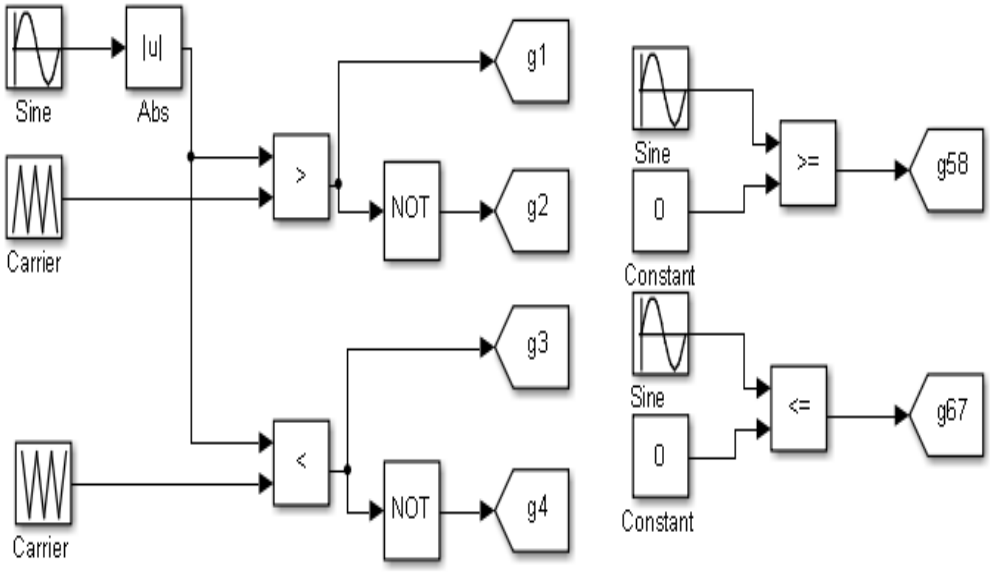


Fig. 4.38 Control block for single phase symmetrical hybrid multilevel inverter with phase shift modulation technique

Fig. 4.38 control block for single phase symmetrical hybrid multilevel inverter with phase shift modulation technique. Fig. 4.39 shows carrier and modulating signal for PS technique for single phase symmetrical hybrid multilevel inverter.

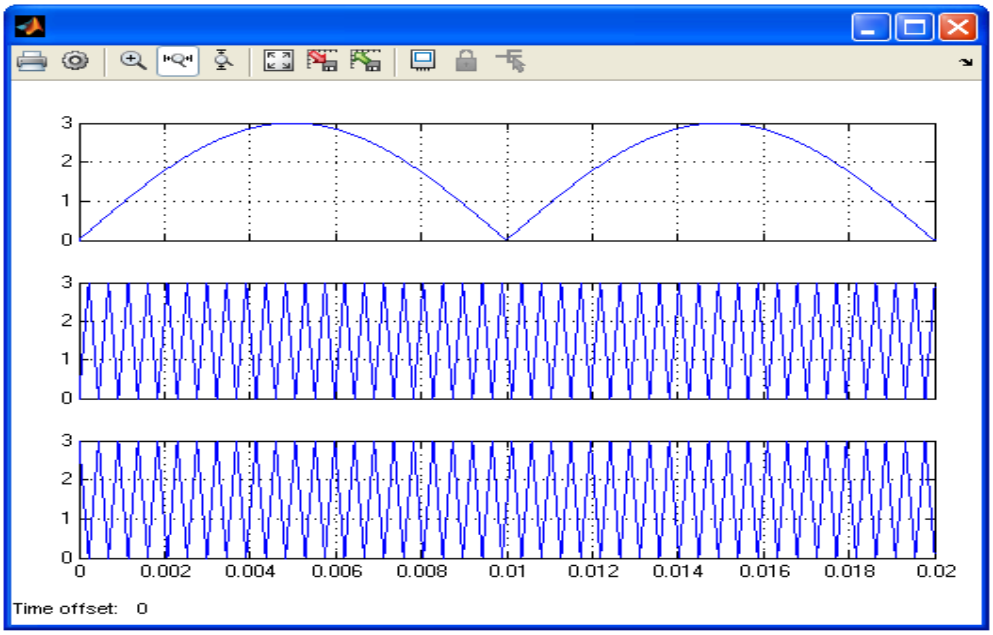


Fig. 4.39 Carrier and modulating signal for symmetrical hybrid MLI with PS technique

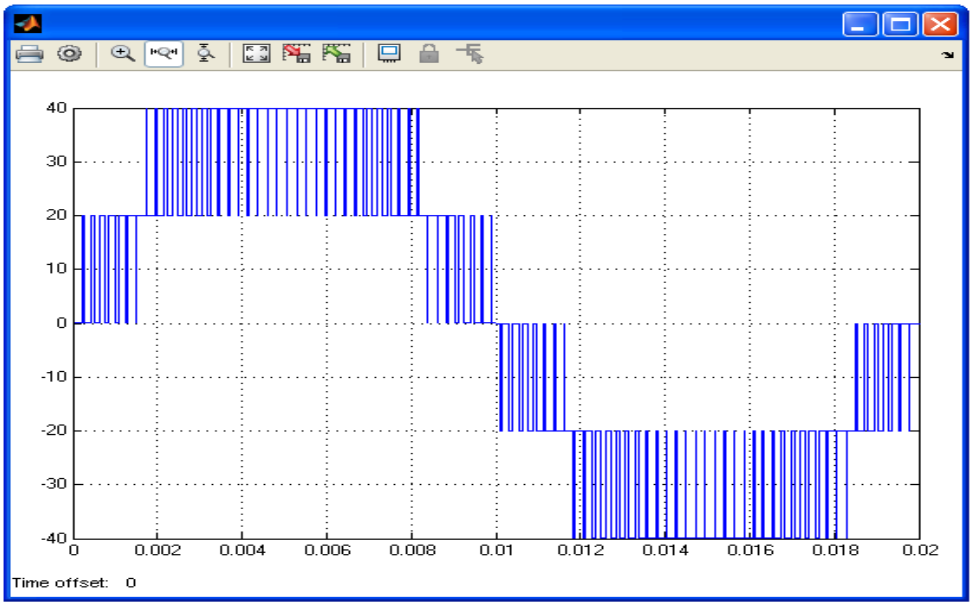


Fig. 4.40 Single phase output for symmetrical multilevel inverter for PS modulation

Fig. 4.40 shows 5 level output voltage where each source is 20V and phase shift modulation technique is applied. Frequency modulation index is approximately 43. Thus output can be changed with different modulation index for amplitude and frequency

hence THD will change accordingly. Fig. 4.41 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

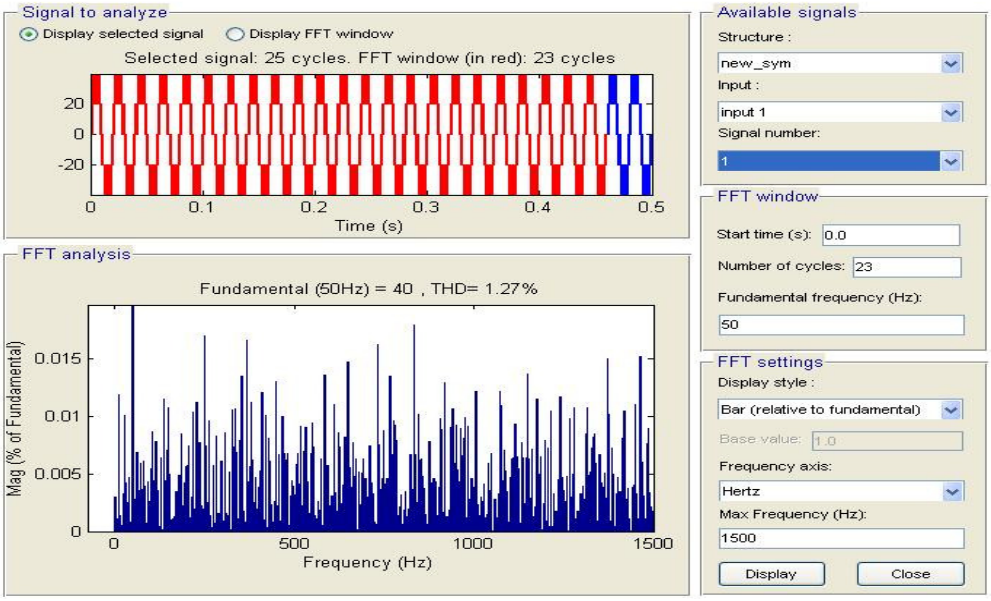


Fig. 4.41 FFT analysis and THD for single phase symmetrical hybrid multilevel inverter with PS modulation

4.2.2.3 Three Phase Symmetrical Hybrid Multilevel Inverter with Phase Shift Modulation Technique

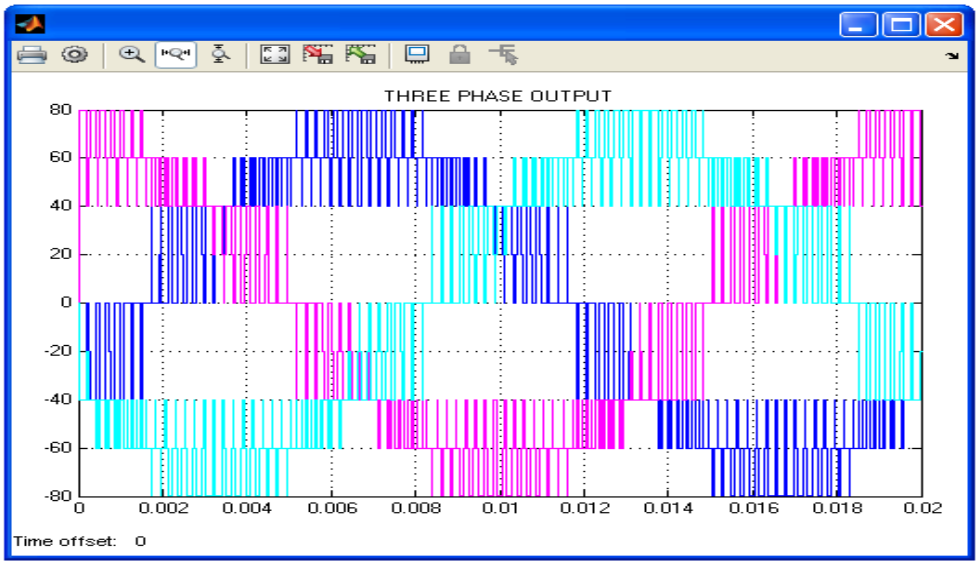


Fig. 4.42 Three phase output for symmetric multilevel inverter for PS modulation

Output for three phase symmetric hybrid multilevel inverter is shown in Fig. 4.42 with DC sources as 20V. Control signals are phase shifted by 120^0. Fig. 4.43 shows nine level output for single leg of three phase symmetric hybrid multilevel inverter. Fig. 4.44

corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

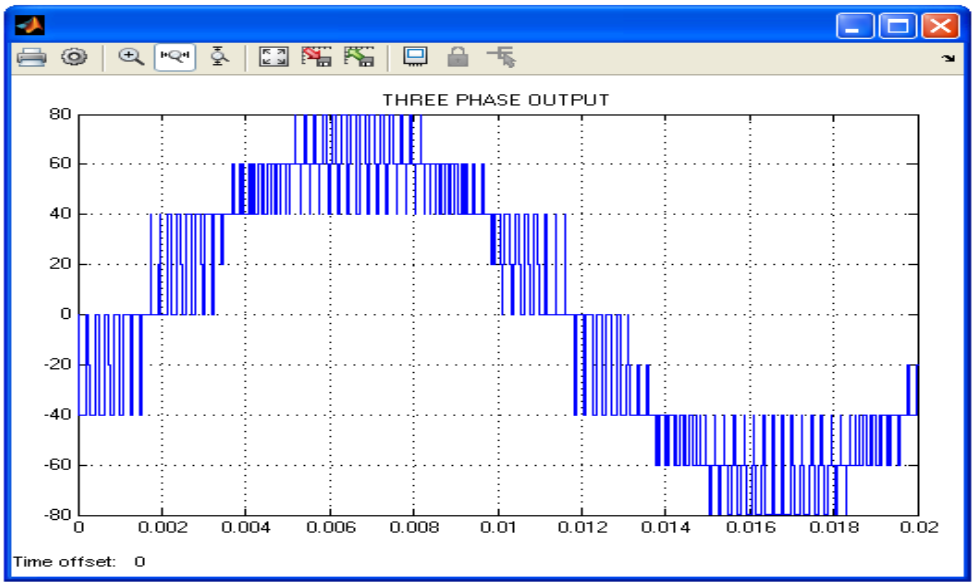


Fig. 4.43 One phase output from three phase symmetric hybrid multilevel inverter PS modulation technique

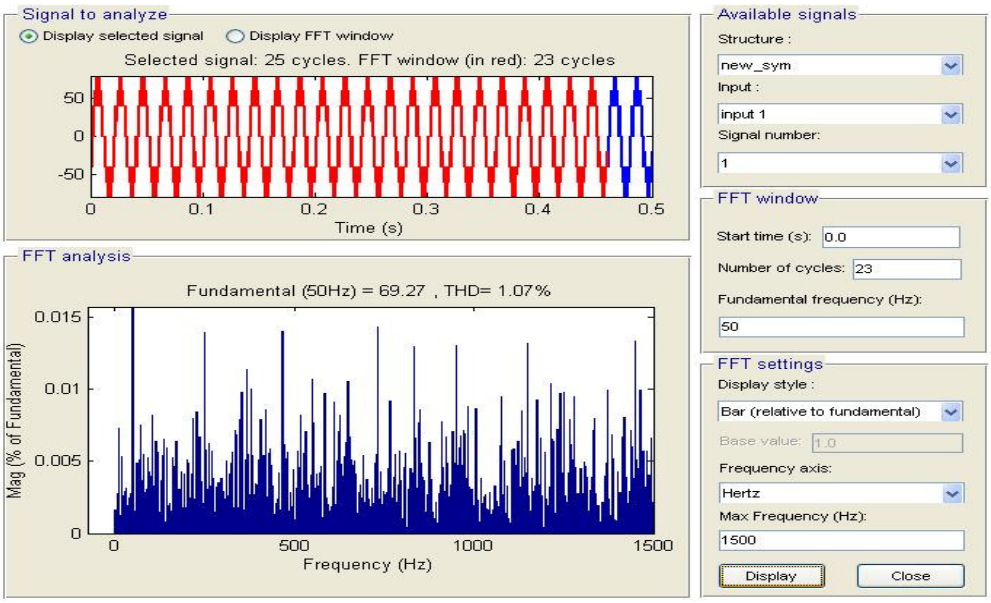


Fig. 4.44 FFT analysis and THD for three phase symmetric hybrid multilevel inverter with PS modulation technique

4.2.3 HALF BRIDGE MODULES BASED HYBRID MULTILEVEL INVERTER

Block diagram structure for single phase half bridge module based hybrid multilevel inverter is shown in Fig. 4.45. DC voltage sources are equal. In this topology half bridges are connected as shown and as per connection output is asymmetric four level output with positive levels greater than negative levels. Hence as shown in Fig.4.45

constant is added to obtain symmetric output across zero level [Fig. 4.4].

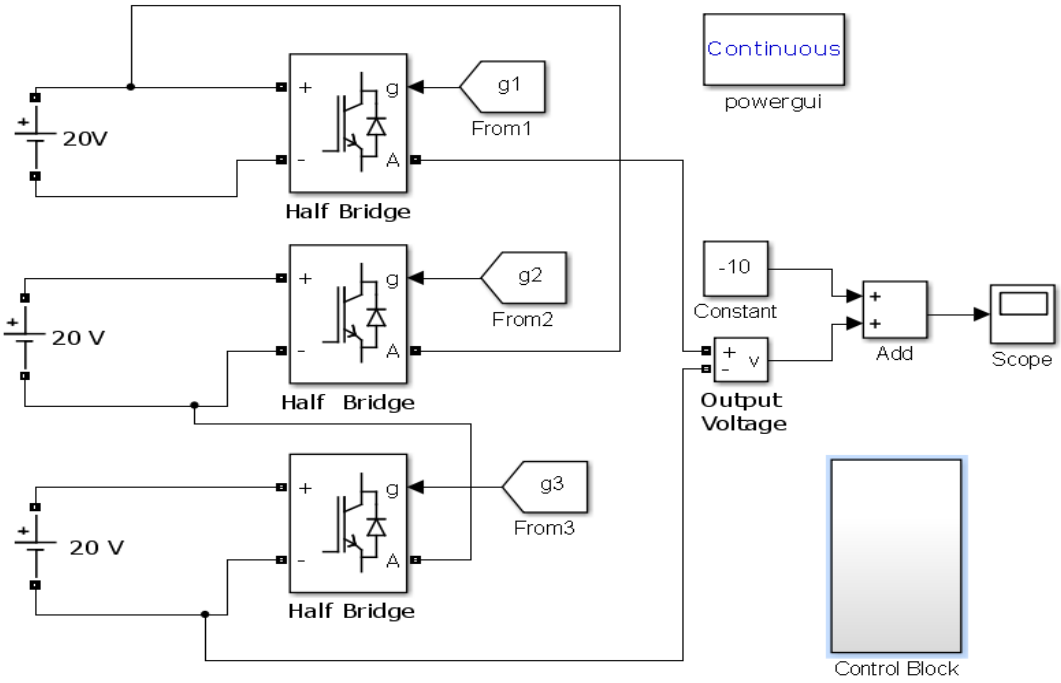


Fig. 4.45 Simulink block for half bridge module based hybrid multilevel inverter

4.2.3.1 Single Phase Half Bridge Modules Based Hybrid Multilevel Inverter with Phase Disposition Modulation Technique

Fig. 4.46 shows carrier and modulating signal for PD technique for single phase half bridge modules based hybrid multilevel inverter.

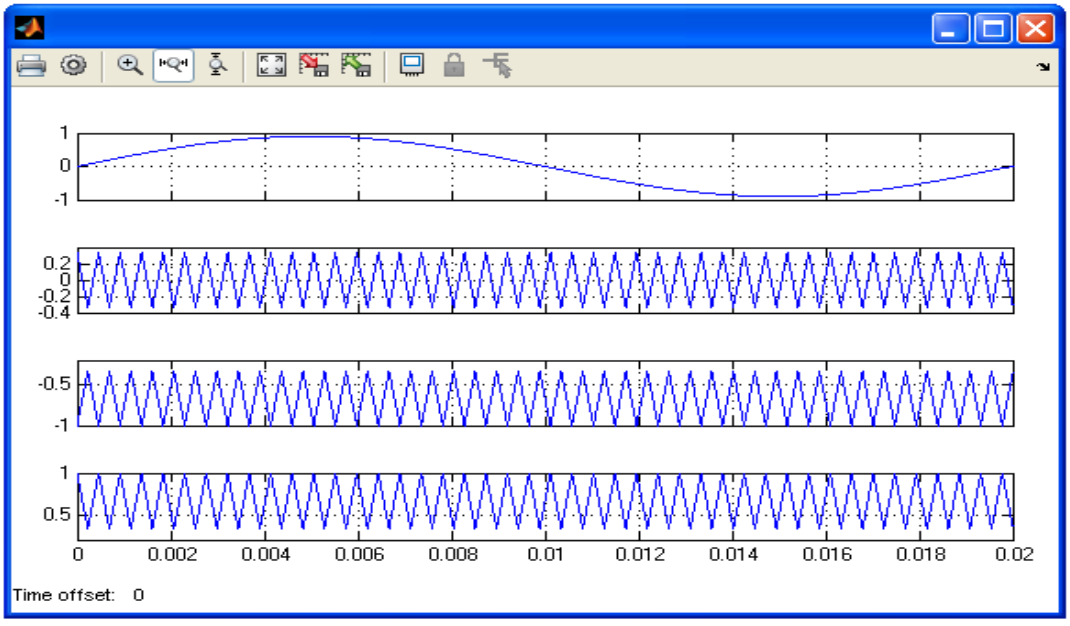


Fig. 4.46 Carrier and modulating signal for half bridge module based hybrid MLI with PD technique

Fig. 4.47 shows 4 level output voltage where each source is 20V and phase disposition modulation technique is applied. Frequency modulation index is approximately 43. Thus output can be changed with different modulation index for amplitude and frequency hence THD will change accordingly. Fig. 4.48 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

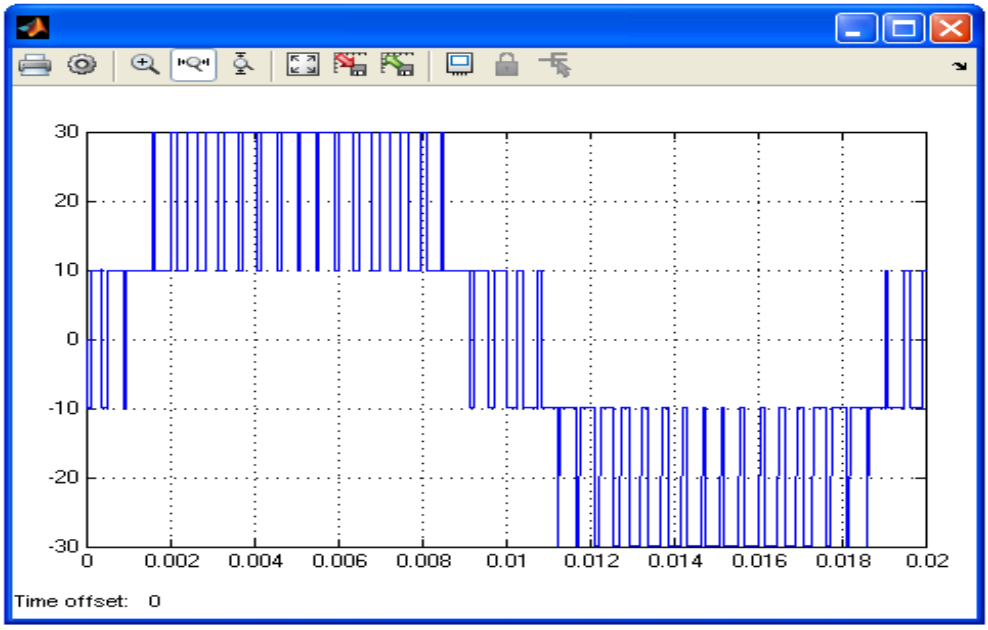


Fig. 4.47 Single phase output for half bridge modules based hybrid multilevel inverter for PD modulation

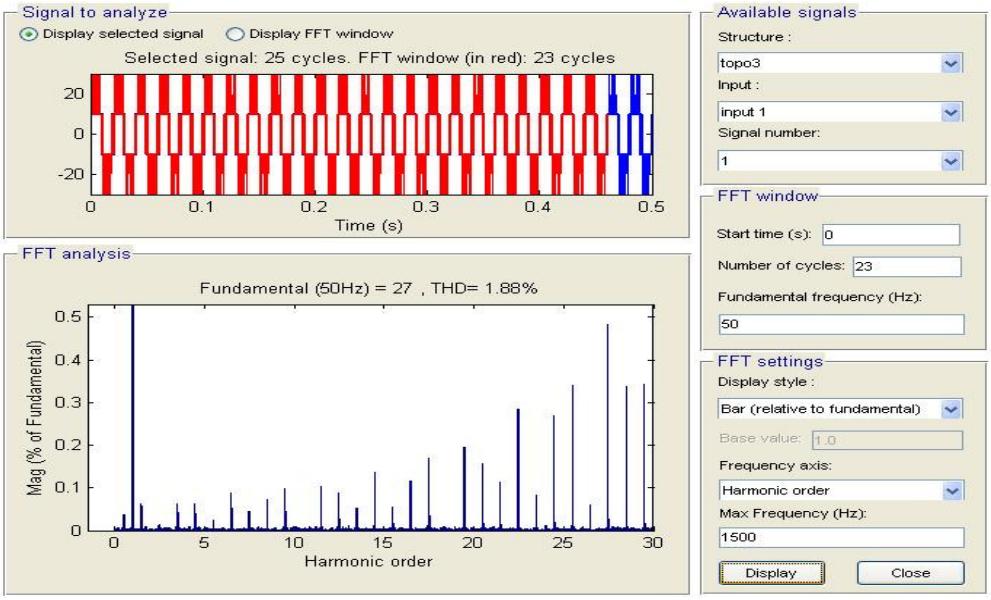


Fig. 4.48 FFT analysis and THD for single phase half bridge module based hybrid multilevel inverter with PD modulation

4.2.3.2 Three Phase Half Bridge Module Based Hybrid Multilevel Inverter with Phase Disposition Modulation Technique

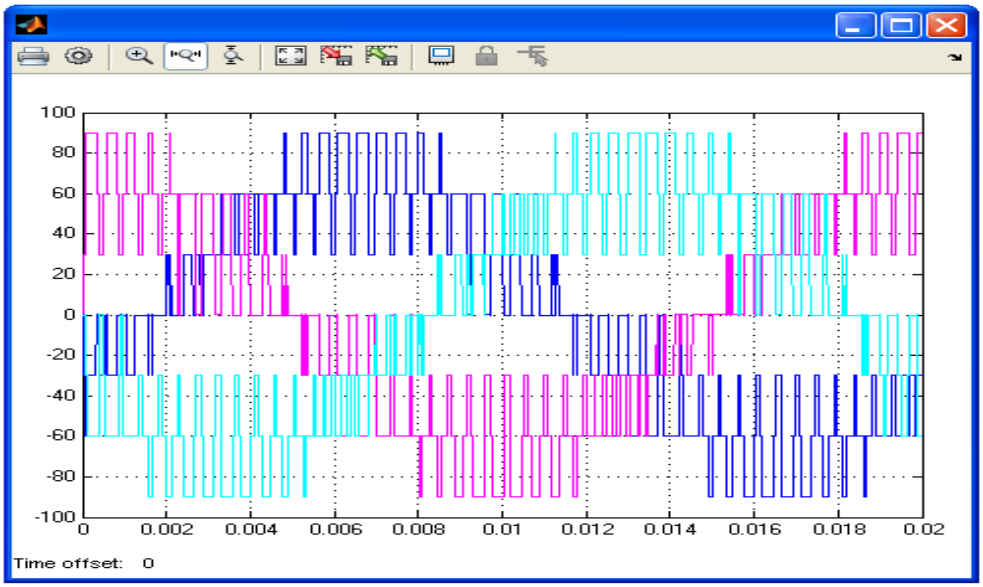


Fig. 4.49 Three phase output for half bridge module based multilevel inverter for PD modulation

Output for three phase half bridge module based hybrid multilevel inverter is shown in Fig. 4.49 with DC sources as 30V. Control signals are phase shifted by 120^0.

Fig. 4.50 shows seven level output for single leg of three phase symmetric hybrid multilevel inverter. Fig. 4.51 corresponds to FFT analysis giving THD at 23^{rd} cycle with 1500 Hz as maximum frequency. Other parameters remain same as above.

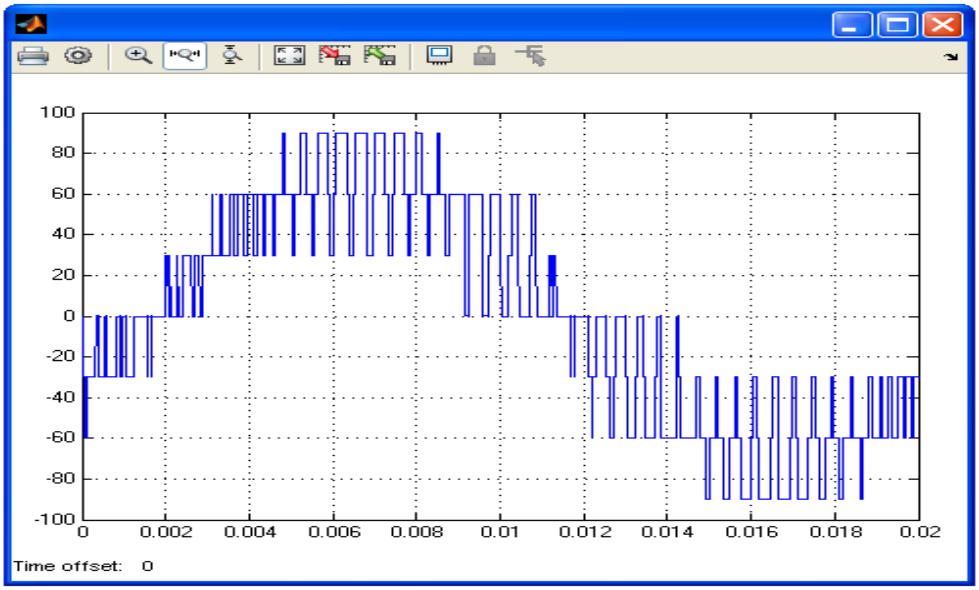


Fig. 4.50 One phase output from three phase half bridge module based hybrid multilevel inverter PD modulation technique

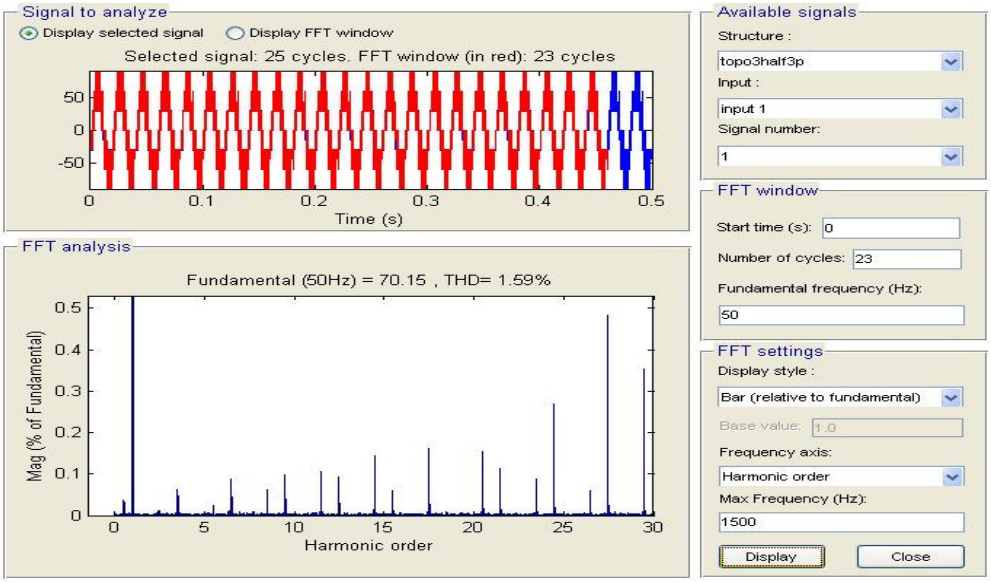


Fig. 4.51 FFT analysis and THD for three phase half bridge module based hybrid multilevel inverter with PD modulation technique

Table 4.1 MATLAB simulation summary

Topology	Phase	Modulation Technique	Output Levels	THD %
Cascaded multilevel inverter	1	--	5	21.92
	1	PD	5	1.31
	1	--	7	9.51
	1	PD	7	0.93
	1	--	9	5.3
Asymmetric hybrid multilevel inverter	1	HYBRID	5	0.8
	1	PD	5	1.17
	3	HYBRID	9	0.64
Symmetrical hybrid multilevel inverter	1	PS	5	1.27
	3	PS	9	1.07
Half bridge modules based hybrid multilevel inverter	1	PD	4	1.88
	3	PD	7	1.59

4.3 SUMMARY

Different MATLAB simulations are done for cascaded multilevel inverter and hybrid multilevel inverter. Comparison is done on basis of THD. Results are summarized in Table 4.1. It is observed that for particular modulation index THD does not vary much with change in modulation technique. Number of stages, number of switches, number of sources, number of capacitors, overall cost etc. are the selection criteria for given application.

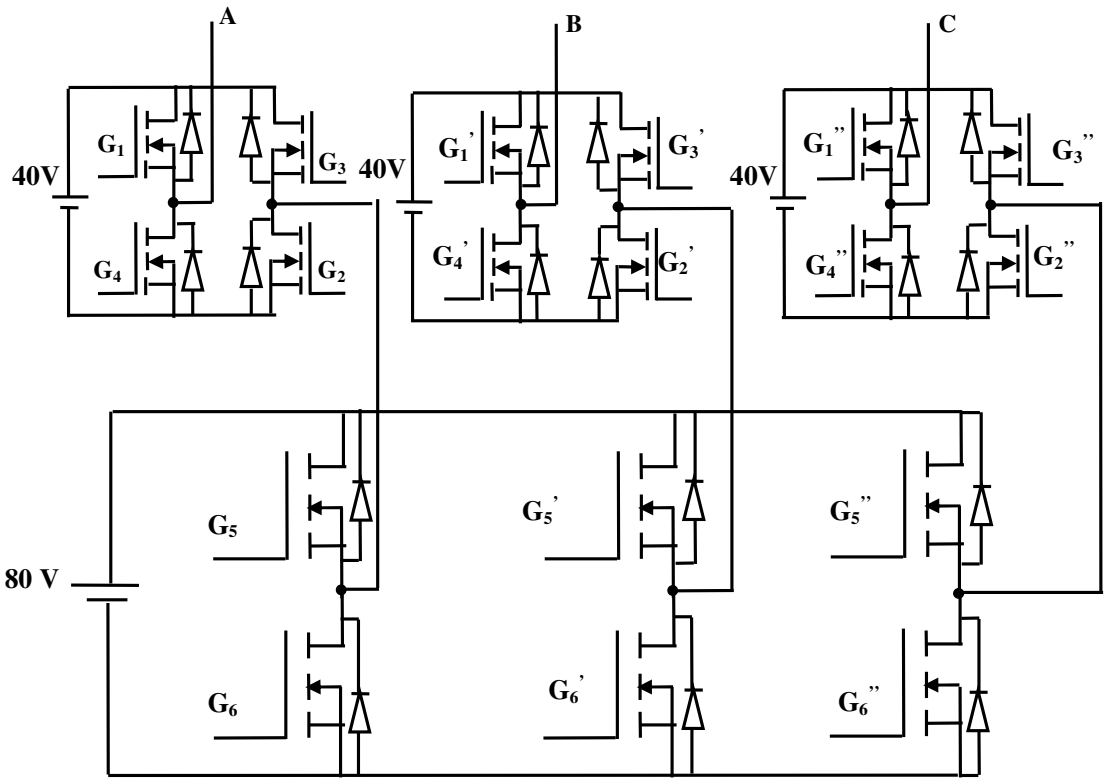
CHAPTER 5

SIMULATIONS RESULTS for SELECTED HYBIRD MULTILEVEL INVERTER

Circuit topology selected for the hardware implementation is as shown below. Circuit selection was done from many available HMLI topologies at the time of registration. As per norms registered topology cannot be changed hence it was implemented but hardware was done for the proposed topology only.

In this chapter MATLAB simulations done for selected configuration of hybrid multilevel inverter are described and analyzed. Simulations are carried out for single phase and three phase. Different modulation techniques implemented are PD, POD, APOD, PS, inverted sine and hybrid modulation technique which are described in chapter 3. Modulation index is taken either 0.9 or 1 specified with respective output figures while frequency modulation index is 21. For better visualization figures are resolved, but simulations and THD measurement are done as per the values specified and not for the resolved one.

Further sections describe MATLAB simulations for selected configuration of single phase and three phase HMLI.



Schematic for power circuit

5.1 SIMULATIONS FOR SINGLE PHASE HYBRID MULTILEVEL INVERTER

Fig. 5.1 is simulation block for selected single phase HMLI for which simulations are done in MATLAB and hardware is also implemented which is described in further chapters. Simulations are done for different modulation techniques. Working principle for this HMLI is explained in chapter 2. Solver ode23tb is used as suggested by MATLAB Help.

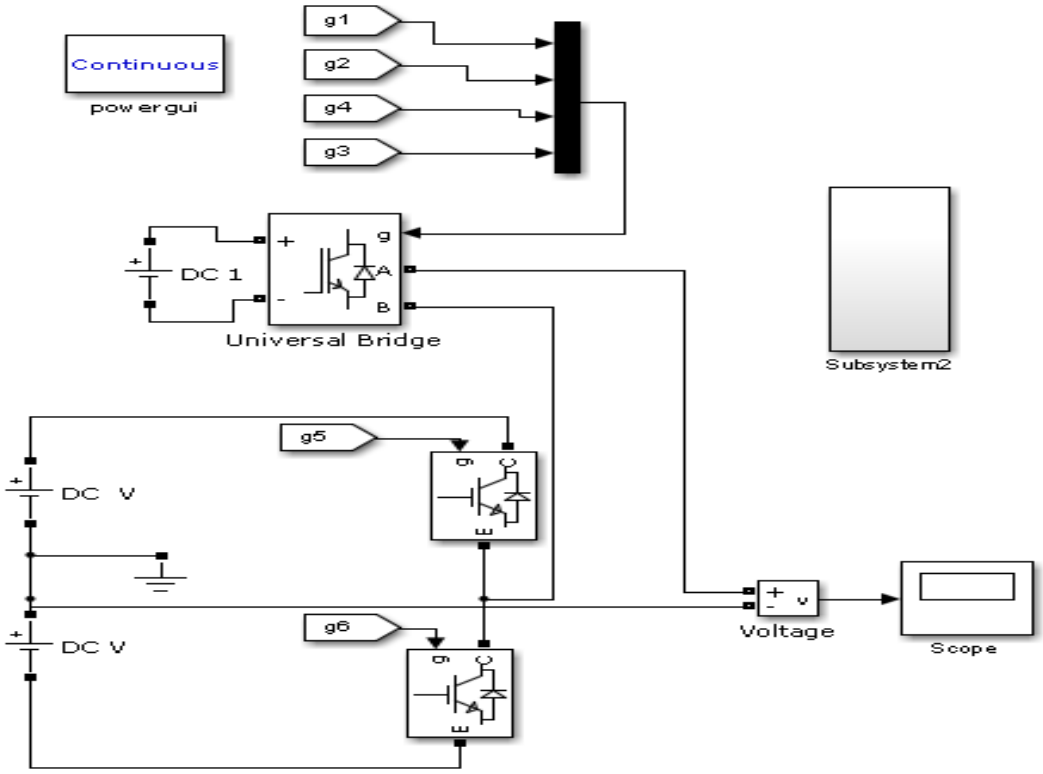


Fig. 5.1 Simulink block for single phase HMLI

5.1.1 SIMULATIONS FOR HMLI WITH PD MODULATION TECHNIQUE

Fig. 5.2 shows the output for single phase HMLI with phase disposition modulation technique and equal DC sources which are equal to 20V. Thus five level output is obtained. While Fig. 5.3 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as mentioned in previous chapter.

For all simulation results on Y-axis voltage in volts is taken and on X-axis time is taken in seconds.

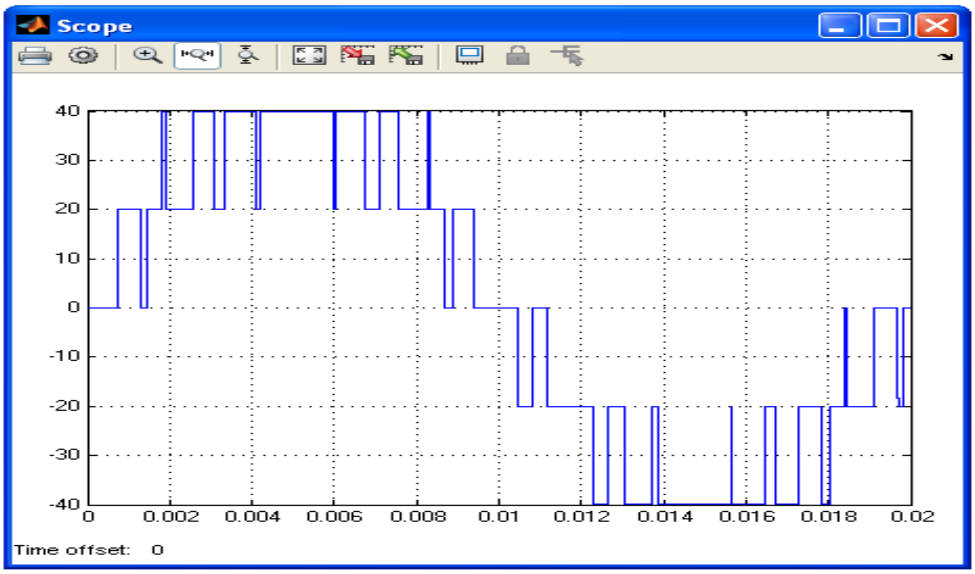


Fig. 5.2 Simulink output for single phase HMLI with PD modulation technique

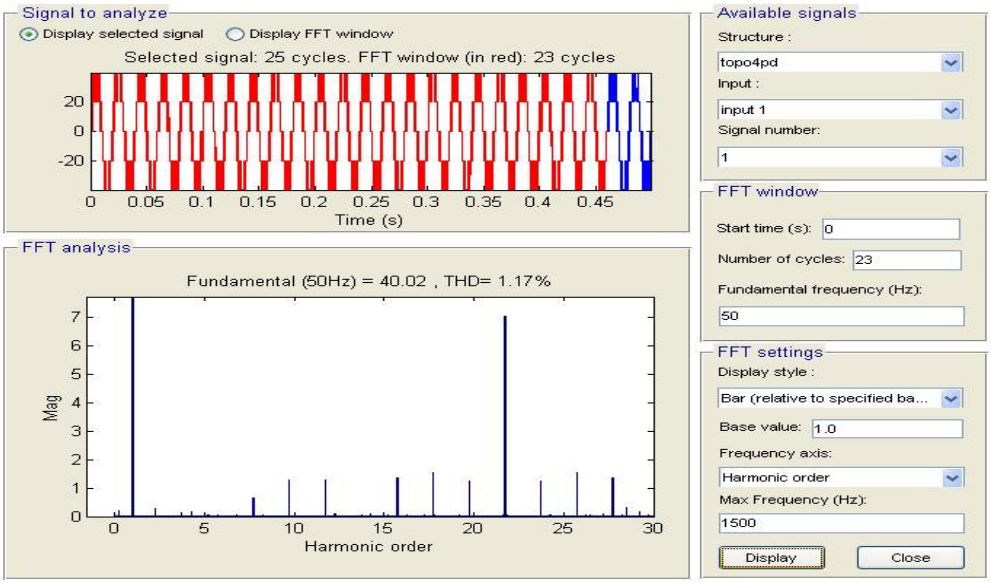


Fig. 5.3 FFT analysis and THD for single phase HMLI with PD modulation technique

5.1.2 SIMULATIONS FOR HMLI WITH POD MODULATION TECHNIQUE

Fig. 5.4 shows the output for single phase HMLI with phase opposition disposition modulation technique and equal DC sources which are equal to 20V. Thus five level output is obtained. While Fig. 5.5 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as mentioned in previous chapter.

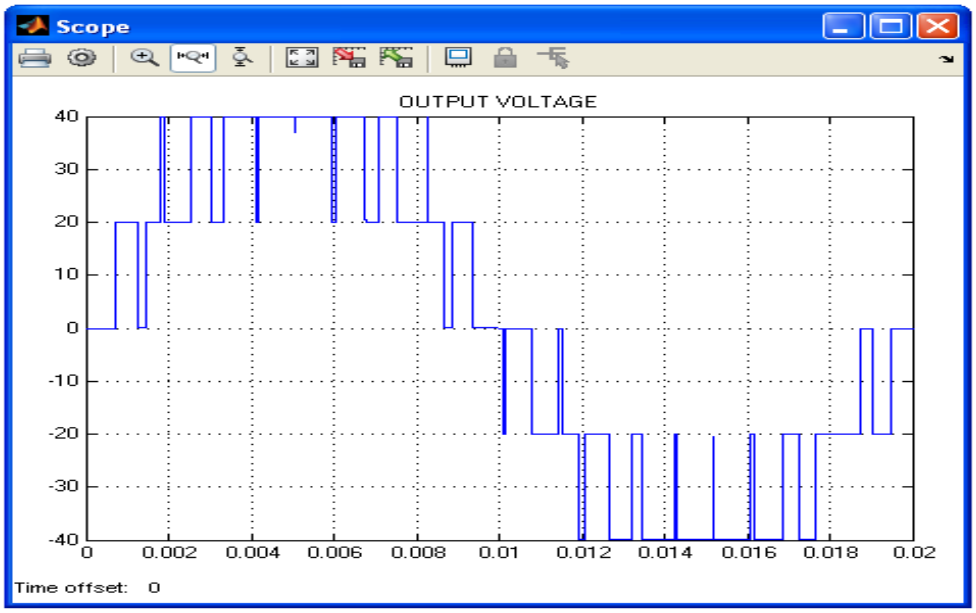


Fig. 5.4 Simulink output for single phase HMLI with POD modulation technique

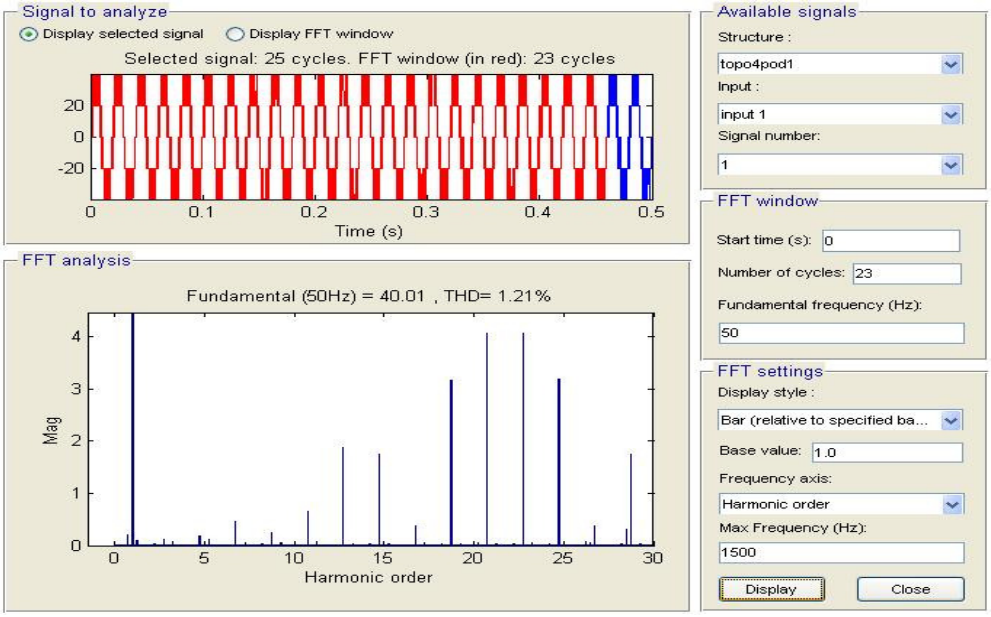


Fig. 5.5 FFT analysis and THD for single phase HMLI with POD modulation technique

5.1.3 SIMULATIONS FOR HMLI WITH APOD MODULATION TECHNIQUE

Fig. 5.6 shows the output for single phase HMLI with alternative phase opposition disposition modulation technique and equal DC sources which are equal to 20V. Thus five level output is obtained. While Fig. 5.7 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as mentioned in previous chapter.

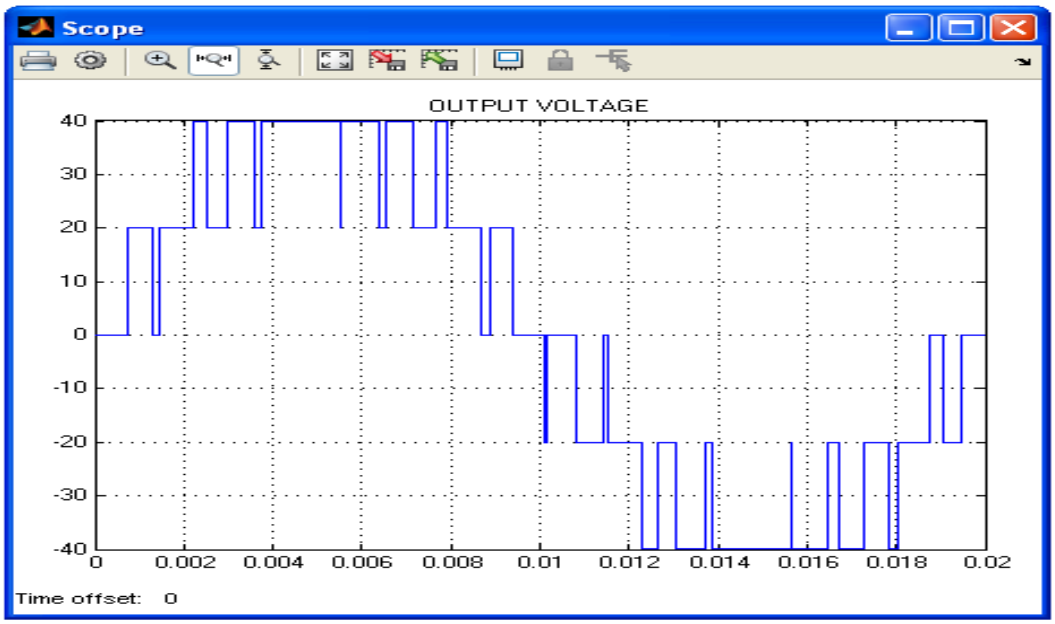


Fig. 5.6 Simulink output for single phase HMLI with APOD modulation technique

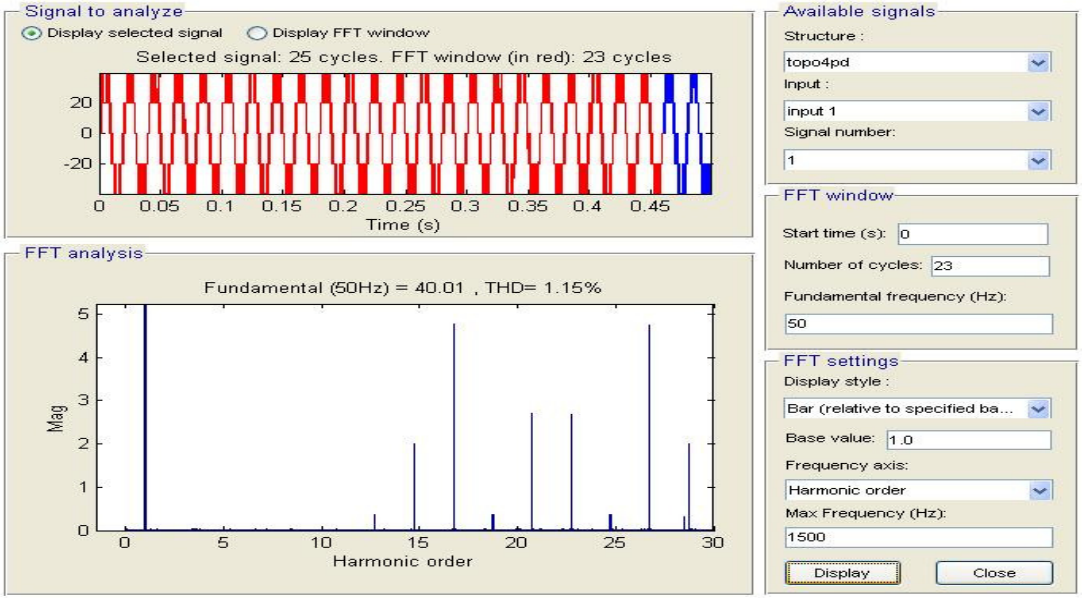


Fig. 5.7 FFT analysis and THD for single phase HMLI with APOD modulation technique

5.1.4 SIMULATIONS FOR HMLI WITH PS MODULATION TECHNIQUE

Fig. 5.8 shows the output for single phase HMLI with phase shifted modulation technique and equal DC sources which are equal to 20V. Thus five level output is obtained. While Fig. 5.9 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency.

Other parameters remain same as mentioned in previous chapter.

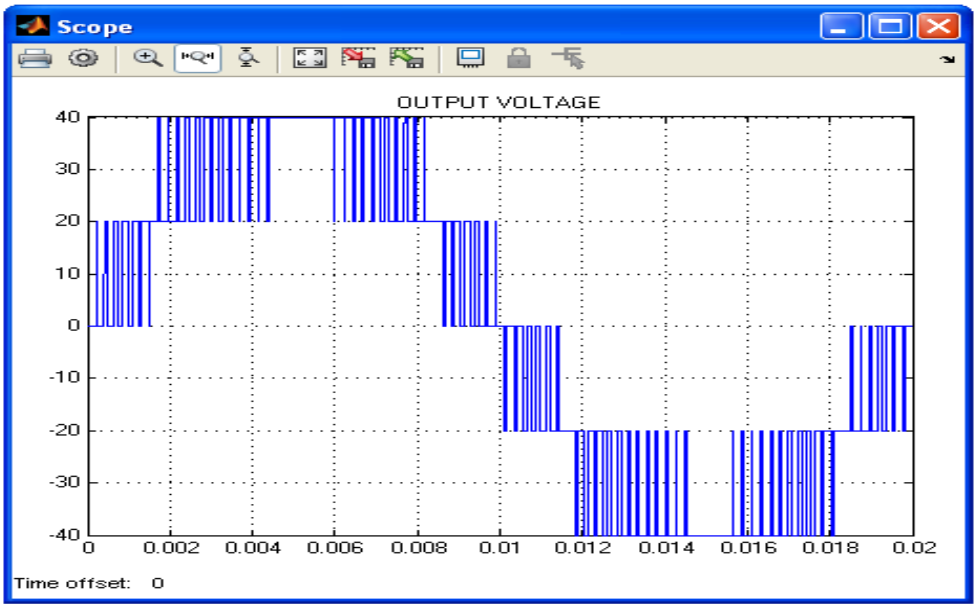


Fig. 5.8 Simulink output for single phase HMLI with PS modulation technique

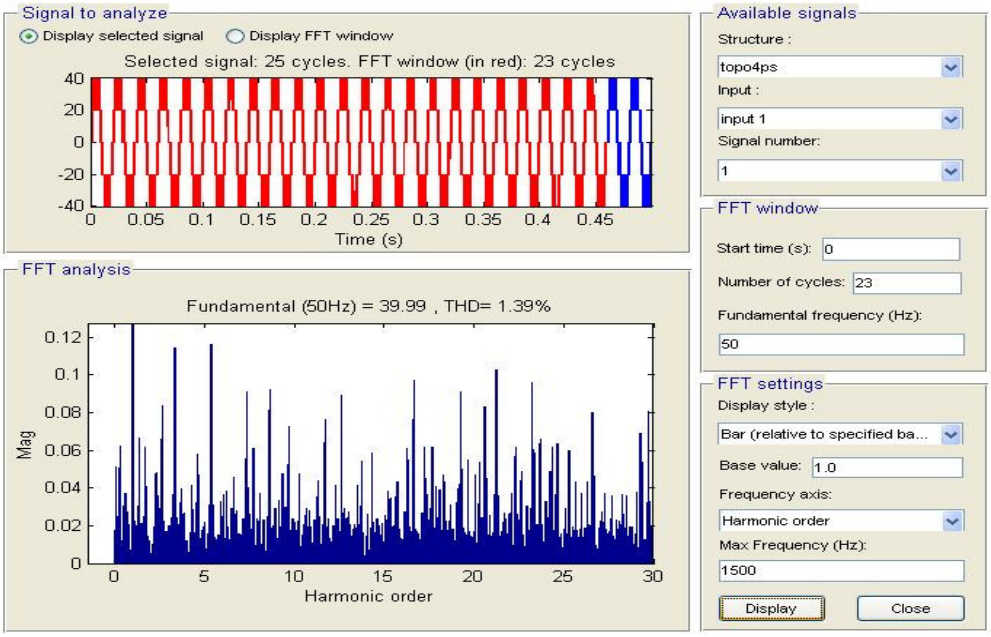


Fig. 5.9 FFT analysis and THD for single phase HMLI with PS modulation technique

5.1.5 SIMULATIONS FOR HMLI WITH HYBRID MODULATION TECHNIQUE

Fig. 5.10 shows the output for single phase HMLI with hybrid modulation technique and equal DC sources which are equal to 20V. Thus five level output is obtained. While Fig. 5.11 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as previous chapter.

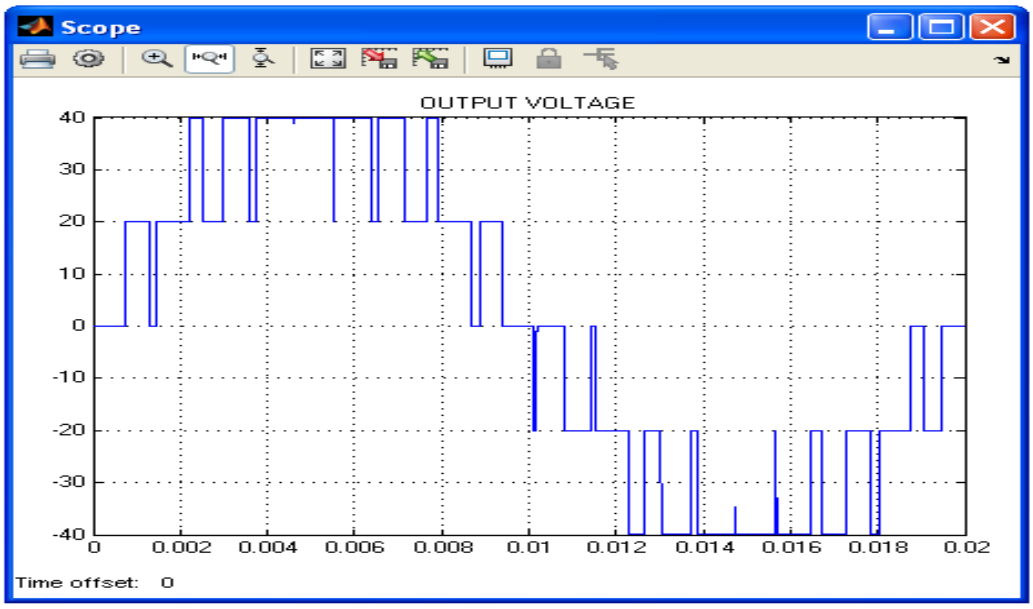


Fig. 5.10 Simulink output for single phase HMLI with hybrid modulation technique

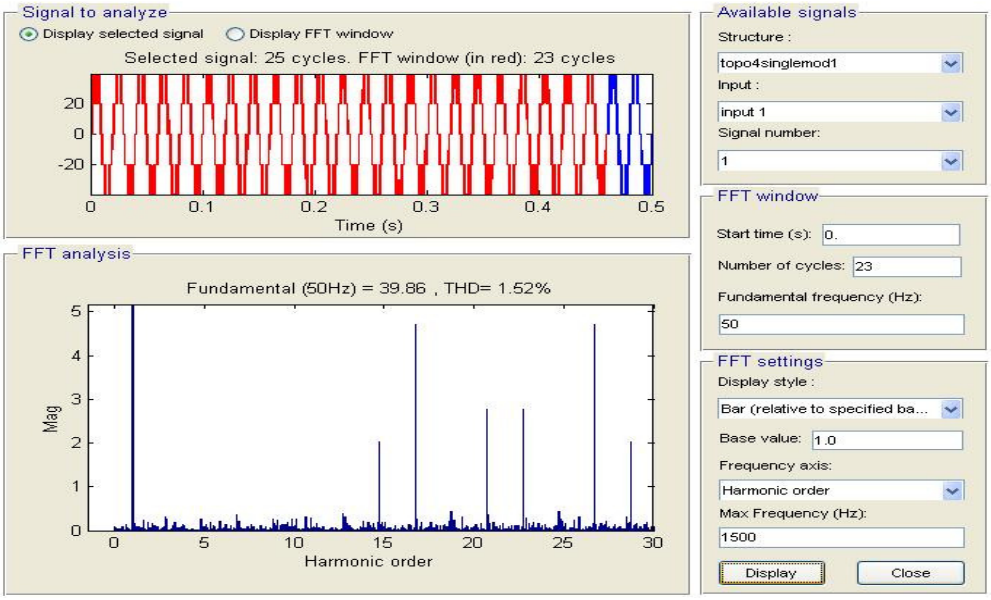


Fig. 5.11 FFT analysis and THD for single phase HMLI with hybrid modulation technique

5.1.6 SIMULATIONS FOR HMLI WITH THIRD HARMONIC INJECTION MODULATION TECHNIQUE

Fig. 5.12 shows control block for single phase HMLI with third harmonic injection modulation technique. Fig. 5.13 shows the output for single phase HMLI with third harmonic injection modulation technique and equal DC sources which is equal to 20V. Thus five level output is obtained. While Fig. 5.14 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. As explained in chapter

3 this modulation technique is applicable for three phase system due to addition of third harmonic in each reference hence THD obtained is high for single phase HMLI.

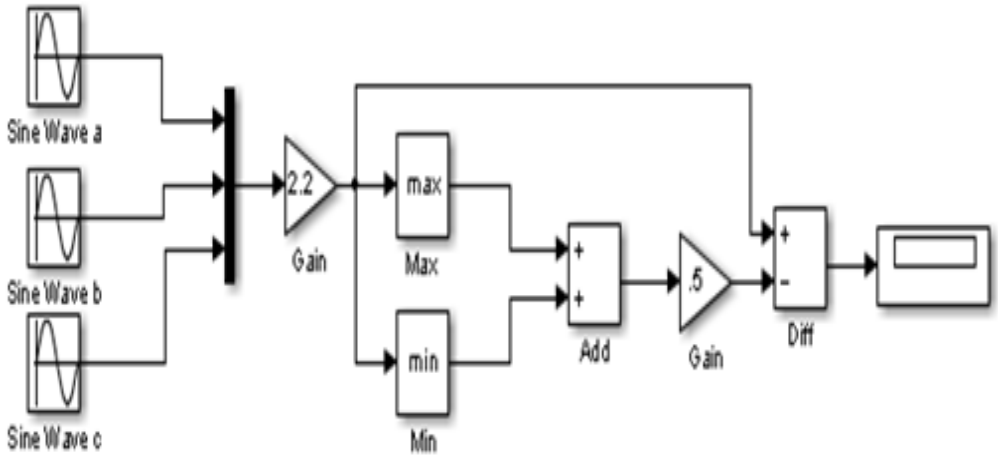


Fig. 5.12 Control block for HMLI with third harmonic injection modulation technique

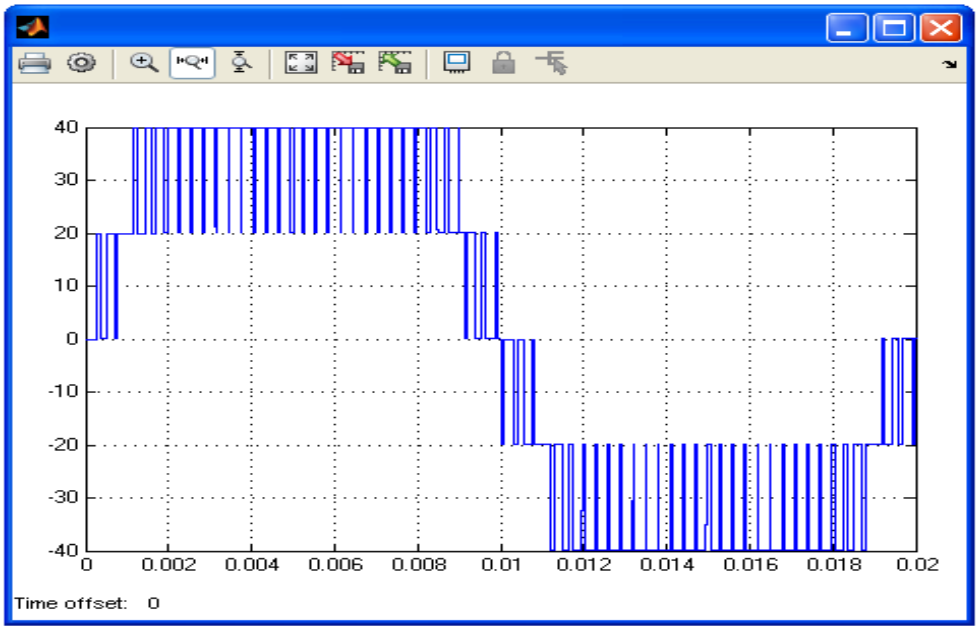


Fig. 5.13 Simulink output for single phase HMLI with third harmonic injection modulation technique

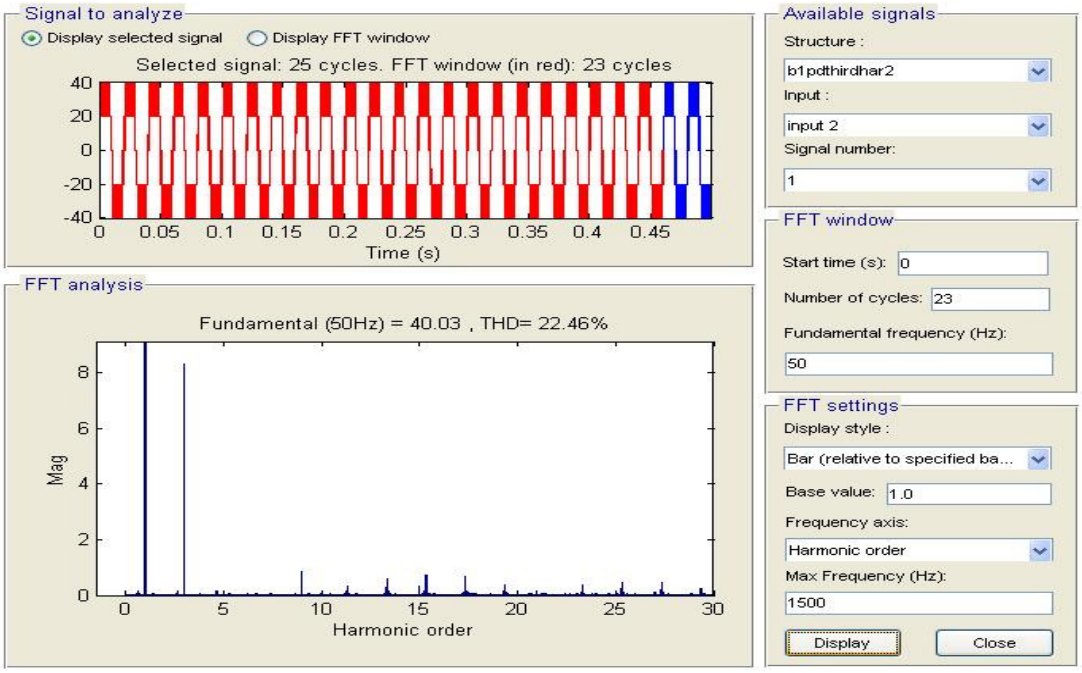


Fig. 5.14 FFT analysis and THD for single phase HMLI with third harmonic injection modulation technique

5.1.7 SIMULATIONS FOR HMLI WITH ISPWM TECHNIQUE

Fig. 5.15 shows the control block for single phase HMLI with ISPWM technique.

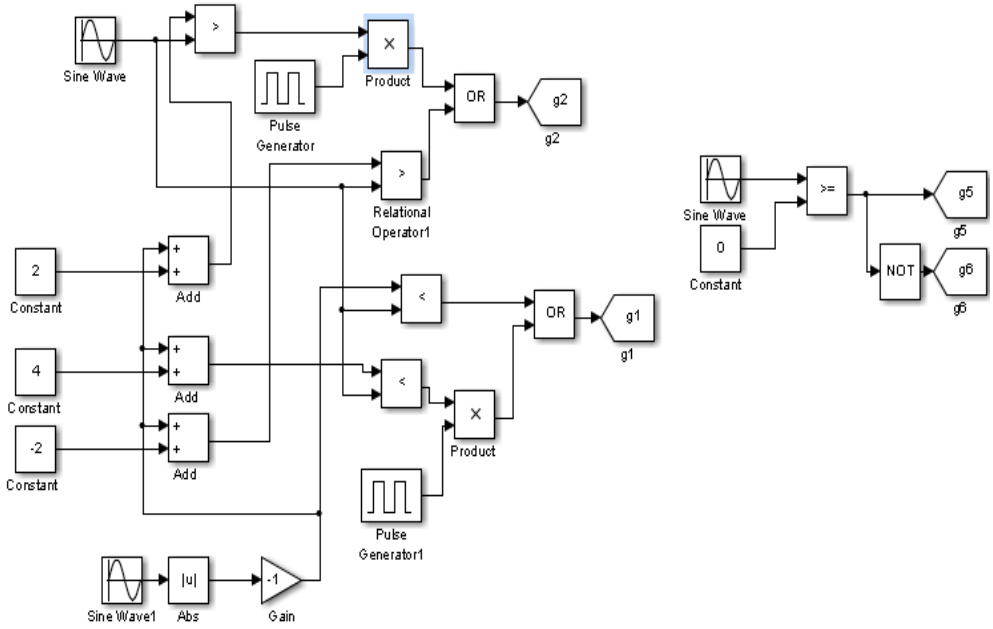


Fig. 5.15 Control block for HMLI with ISPWM technique

Fig. 5.16 shows the output for single phase HMLI with ISPWM technique and equal DC sources which is equal to 20V. Thus five level output is obtained. While Fig. 5.17 corresponds to FFT analysis giving THD at 1st cycle with 1500 Hz as maximum

frequency. It was observed that for increased number of cycles THD remains unchanged. For ISPWM carrier frequency is 1 kHz. Output is not half wave symmetrical thus even harmonics are also present hence THD is more.

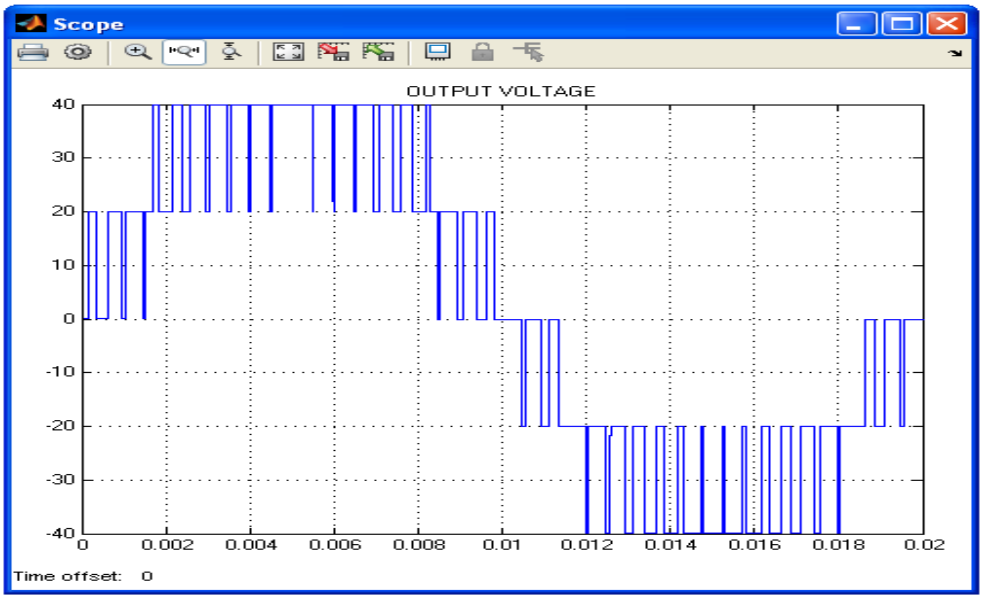


Fig. 5.16 Simulink output for single phase HMLI with inverted sine modulation technique

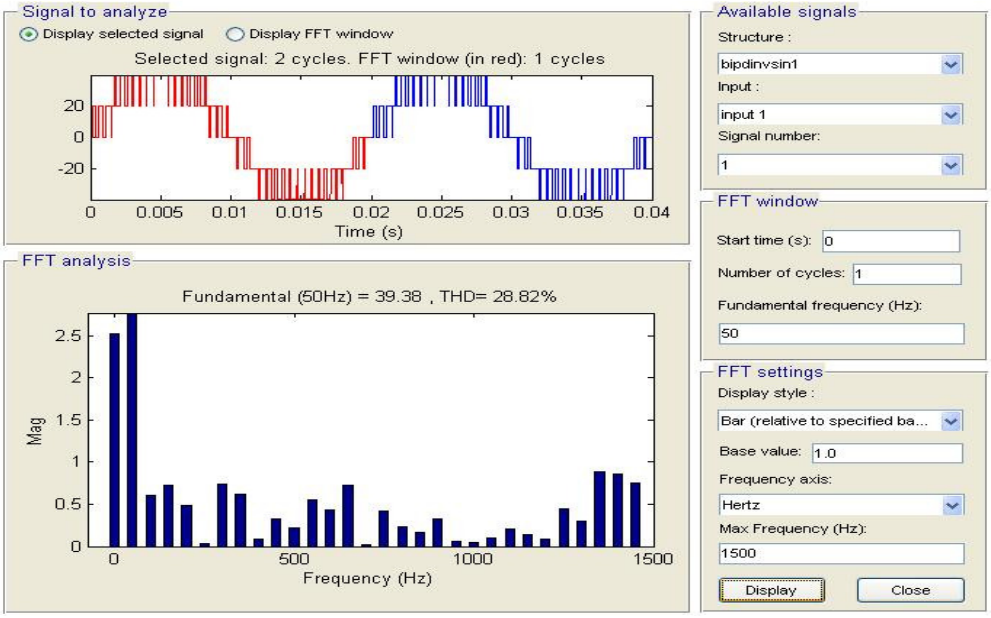


Fig. 5.17 FFT analysis and THD for single phase HMLI with inverted sine modulation technique

5.2 SIMULATIONS FOR THREE PHASE HYBRID MULTILEVEL INVERTER

Fig. 5.18 is simulation block for selected three phase HMLI for which simulations are done in MATLAB and hardware is also implemented which is described

in further chapters. Simulations are done for different modulation techniques. Working principle for this HMLI is explained in chapter 2.

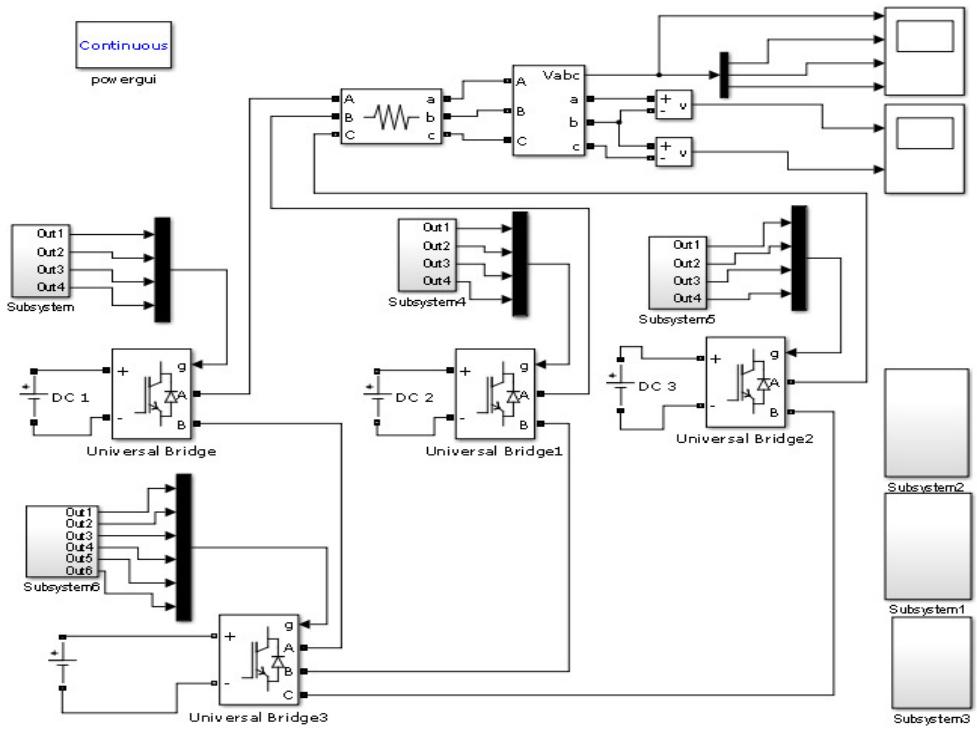


Fig. 5.18 Simulink block for three phase HMLI

5.2.1 SIMULATIONS FOR THREE PHASE HMLI WITH PD MODULATION TECHNIQUE

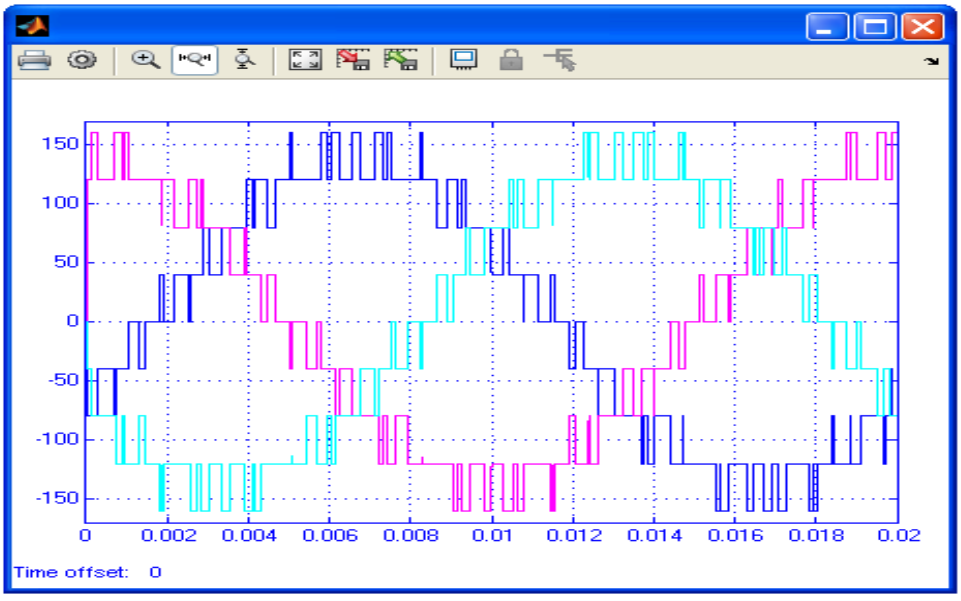


Fig. 5.19 Simulink output for three phase HMLI with PD modulation technique

Fig. 5.19 shows the output for three phase HMLI with phase disposition modulation technique.

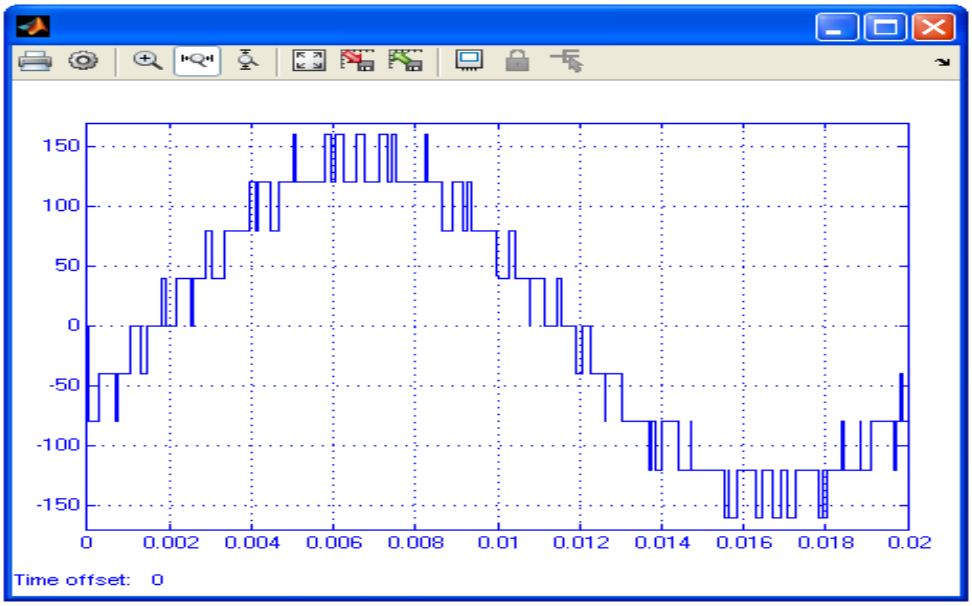


Fig. 5.20 One phase output from three phase HMLI PD modulation technique

DC source is 80V for three phase inverter and 40V for single phase 3 H bridges. Thus nine level output is obtained. While Fig. 5.21 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as previous chapter.

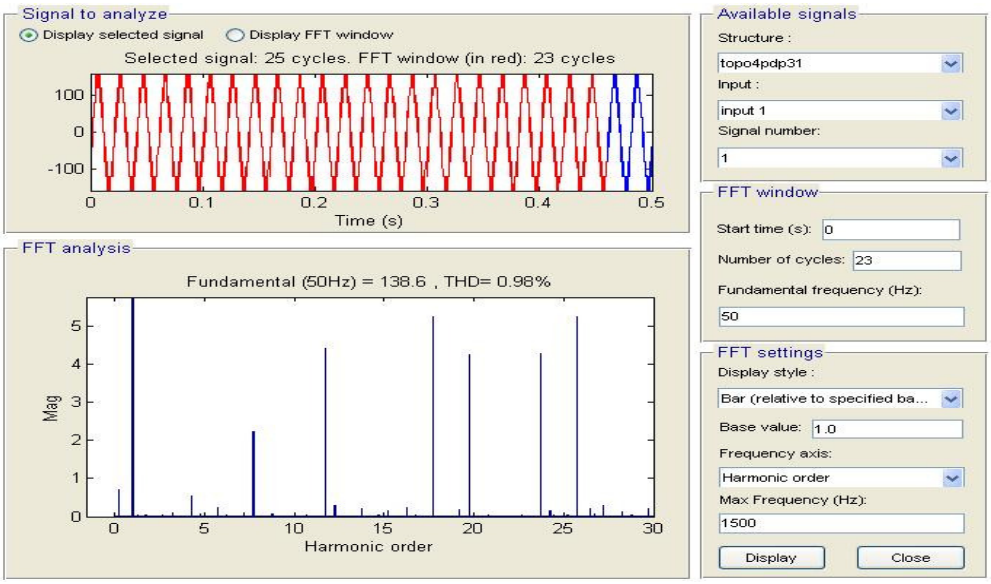


Fig. 5.21 FFT analysis and THD for HMLI with PD modulation technique

5.2.2 SIMULATIONS FOR THREE PHASE HMLI WITH POD MODULATION TECHNIQUE

Fig. 5.22 shows the output for three phase HMLI with phase opposition disposition modulation technique.

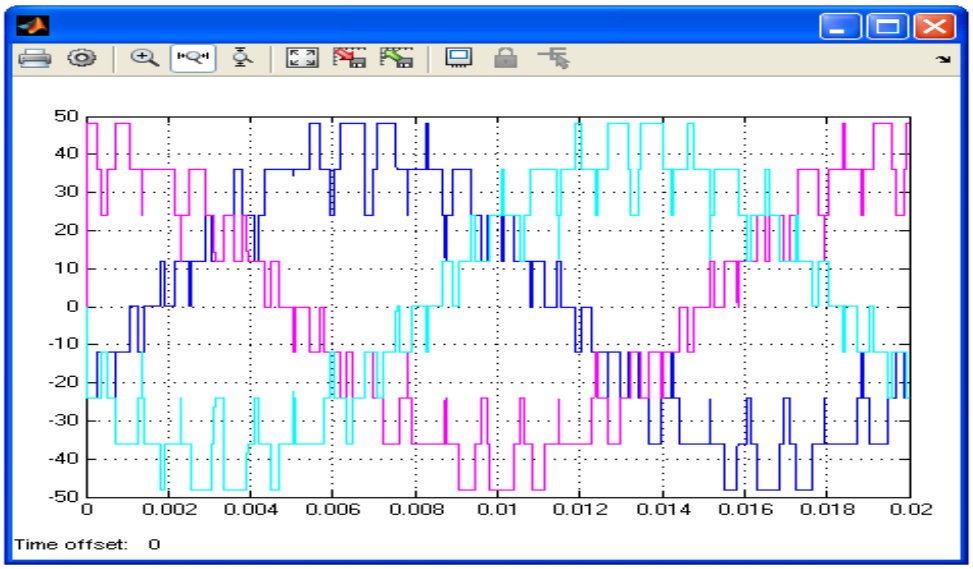


Fig. 5.22 Simulink output for three phase HMLI with POD modulation technique

DC source is 24V for three phase inverter and 12V for single phase 3 H bridges. Thus nine level output is obtained. While Fig. 5.24 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as previous chapter.

Fig. 5.23 One phase output from three phase HMLI POD modulation technique

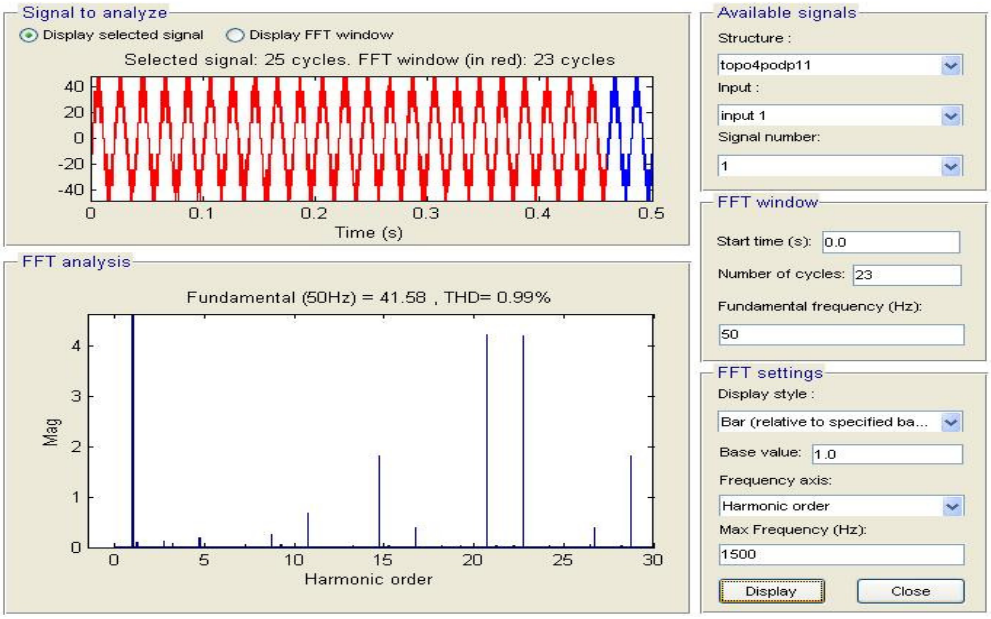


Fig. 5.24 FFT analysis and THD for HMLI with POD modulation technique

5.2.3 SIMULATIONS FOR THREE PHASE HMLI WITH APOD MODULATION TECHNIQUE

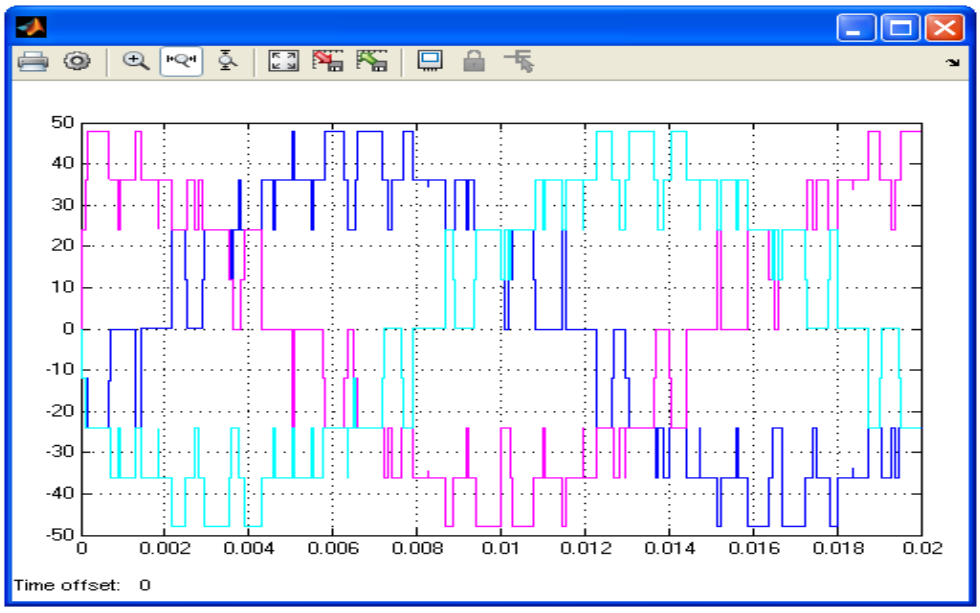


Fig. 5.25 Simulink output for three phase HMLI with APOD modulation technique

Fig. 5.25 shows the output for three phase HMLI with alternative phase opposition disposition modulation technique. DC source is 24V for three phase inverter and 12V for single phase 3 H bridges. Thus nine level output is obtained. While Fig. 5.27 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as previous chapter.

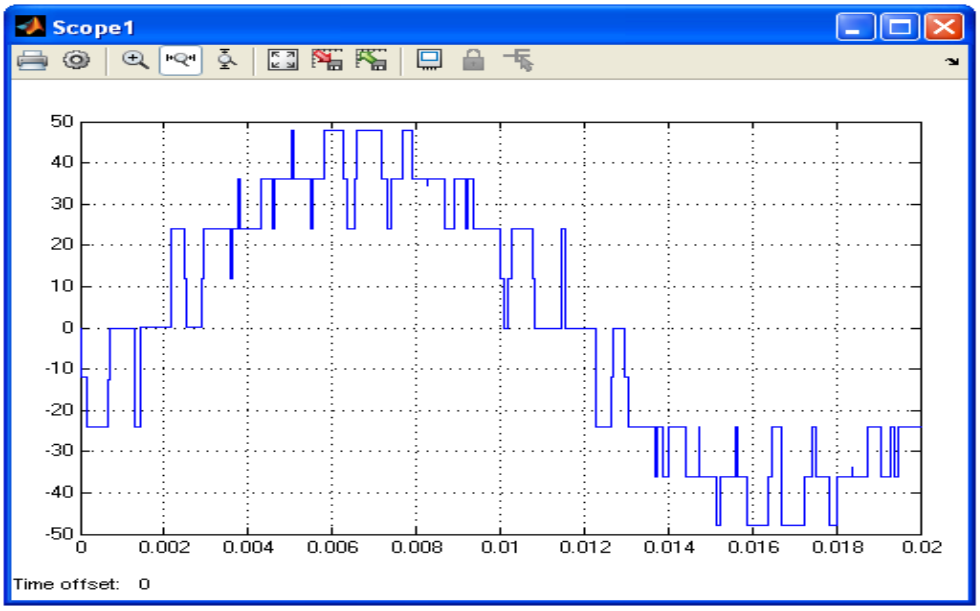


Fig. 5.26 One phase output from three phase HMLI APOD modulation technique

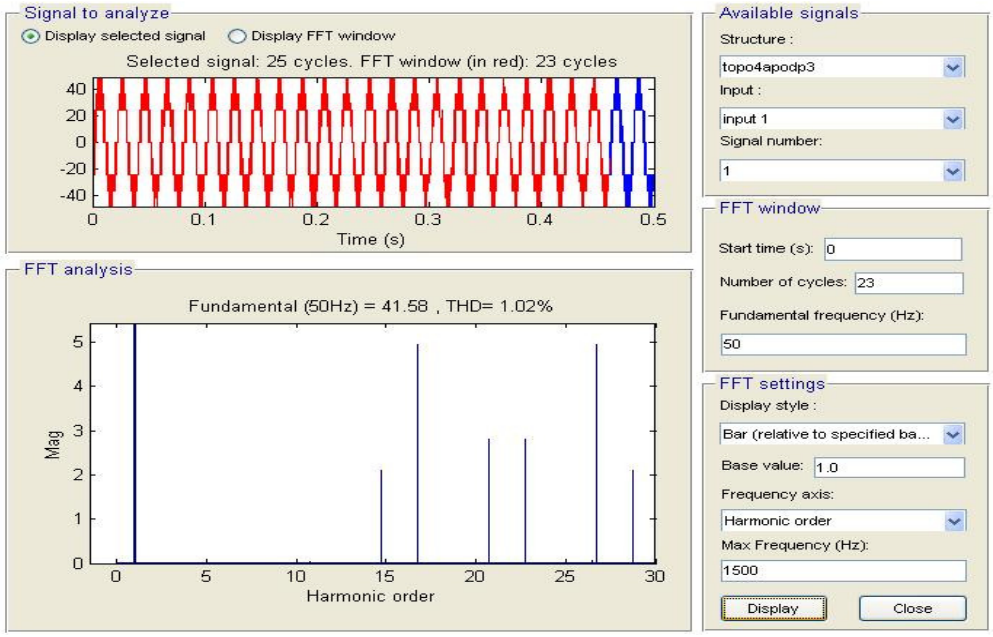


Fig. 5.27 FFT analysis and THD for HMLI with APOD modulation technique

5.2.4 SIMULATIONS FOR THREE PHASE HMLI WITH PS MODULATION TECHNIQUE

Fig. 5.28 shows the output for three phase HMLI with phase shifted modulation technique. DC source is 40 V for three phase inverter and 20 V for single phase 3 H bridges. Thus nine level output is obtained. While Fig. 5.30 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as previous chapter.

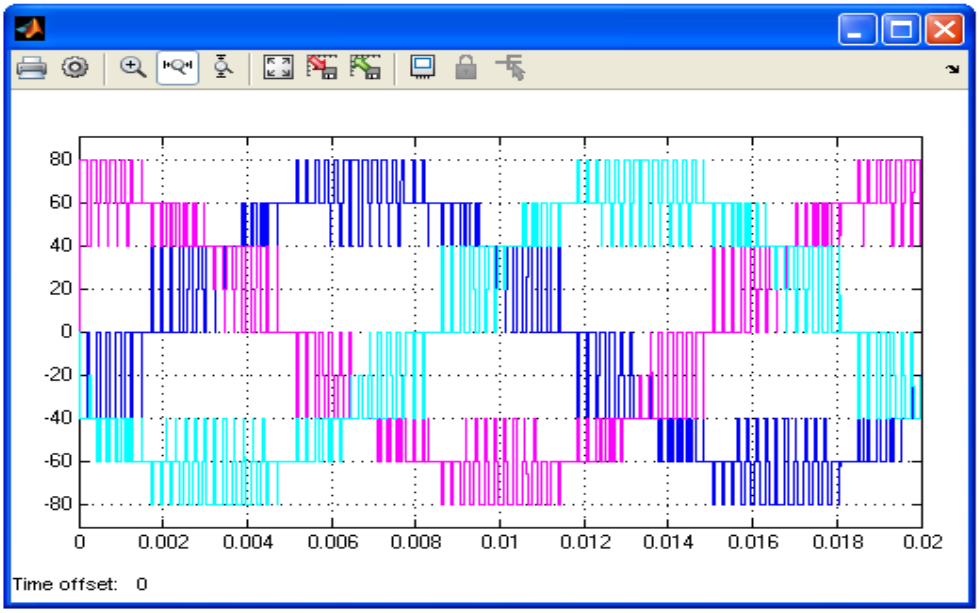


Fig. 5.28 Simulink output for three phase HMLI with PS modulation technique

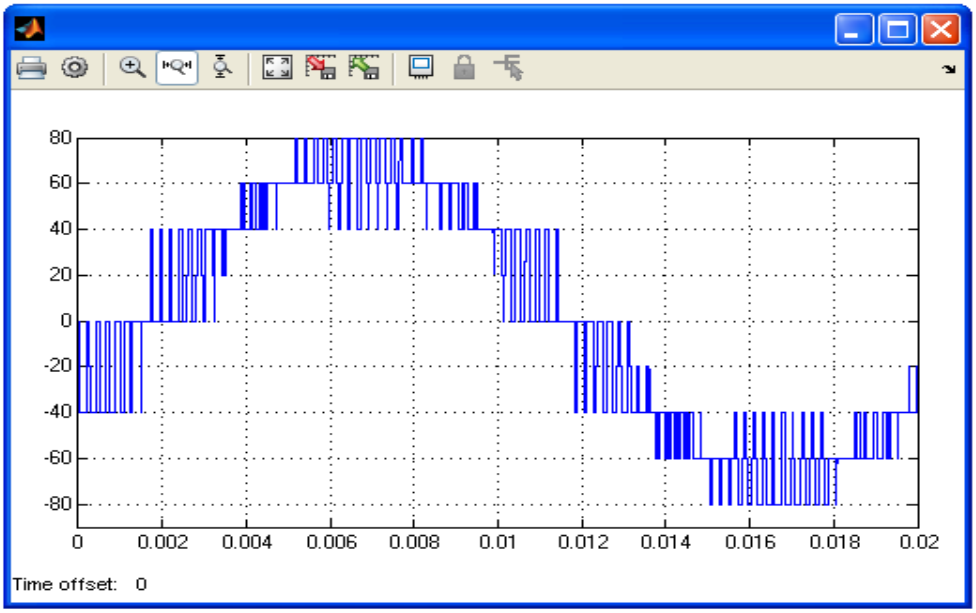


Fig. 5.29 One phase output from three phase HMLI PS modulation technique

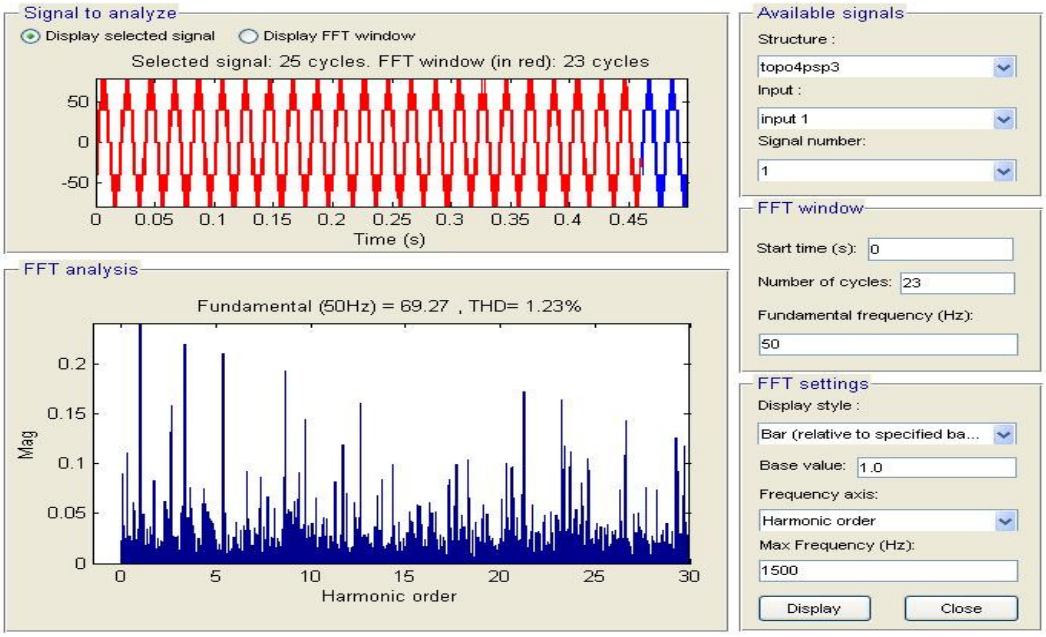


Fig. 5.30 FFT analysis and THD for HMLI with PS modulation technique

5.2.5 SIMULATIONS FOR THREE PHASE HMLI WITH HYBRID MODULATION TECHNIQUE

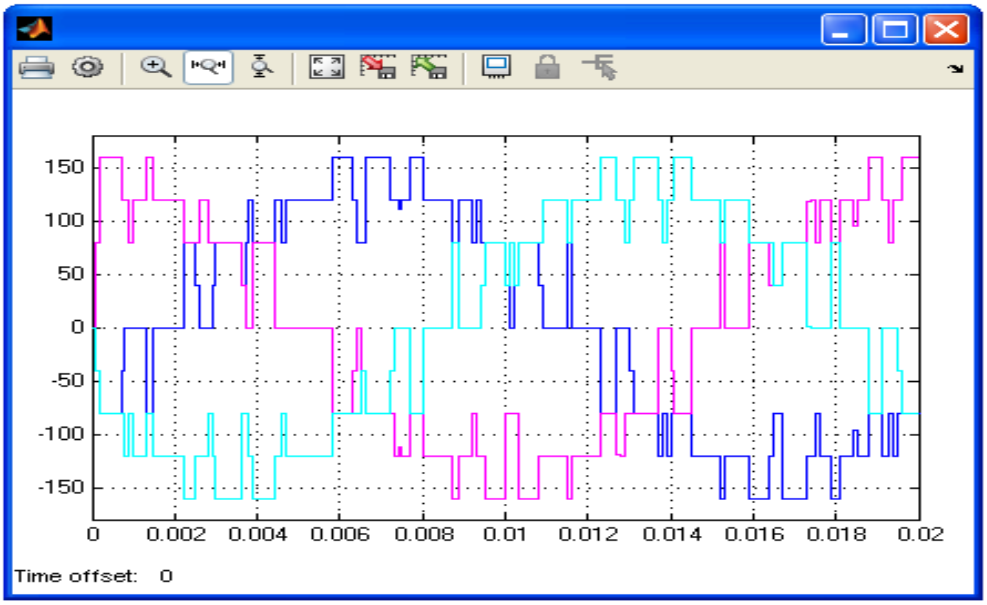


Fig. 5.31 Simulink output for three phase HMLI with hybrid modulation technique

Fig. 5.29 shows the output for three phase HMLI with hybrid modulation technique. DC source is 80 V for three phase inverter and 40 V for single phase 3 H bridges. Thus nine level output is obtained. While Fig. 5.31 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as previous chapter.

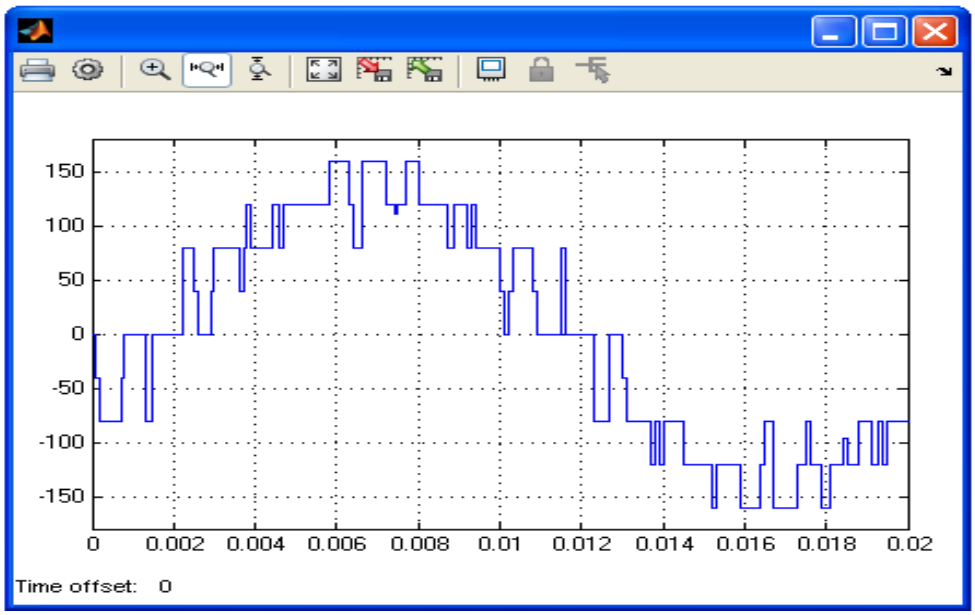


Fig. 5.32 One phase output from three phase HMLI hybrid modulation technique

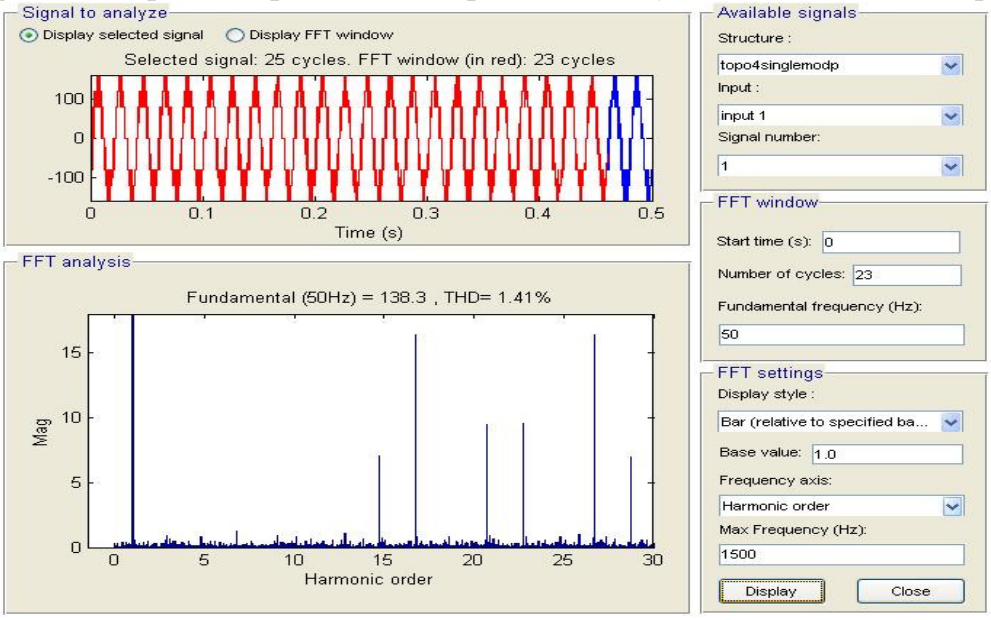


Fig. 5.33 FFT analysis and THD for HMLI with hybrid modulation technique

5.2.6 SIMULATIONS FOR HMLI WITH THIRD HARMONIC INJECTION MODULATION TECHNIQUE

Fig. 5.32 shows the output for three phase HMLI with phase shifted modulation technique. DC source is 80 V for three phase inverter and 40 V for single phase 3 H bridges. Thus nine level output is obtained. While Fig. 5.34 corresponds to FFT analysis giving THD at 23rd cycle with 1500 Hz as maximum frequency. Other parameters remain same as previous chapter.

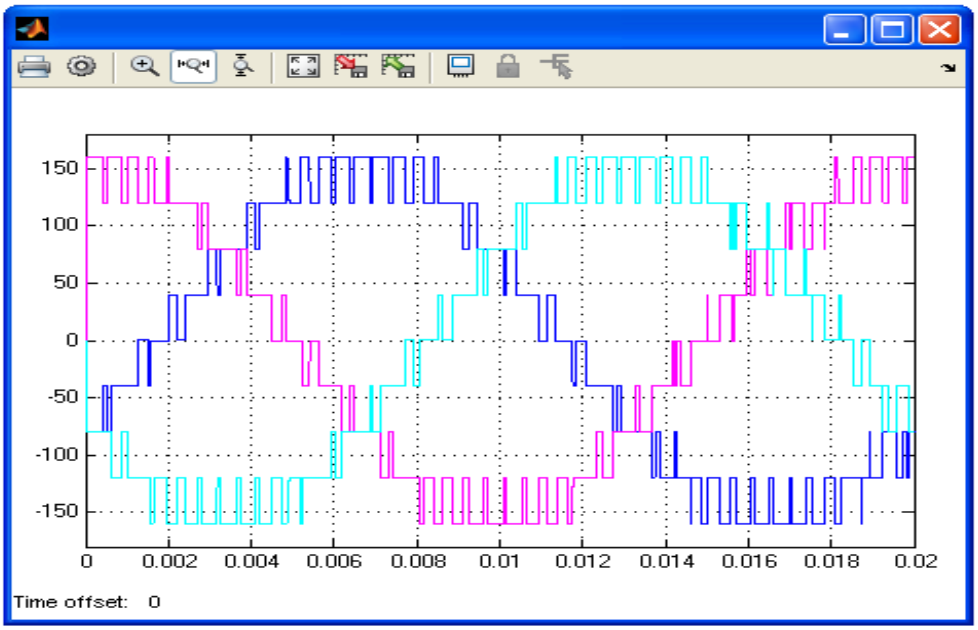


Fig. 5.34 Simulink output for three phase HMLI with third harmonic injection modulation technique

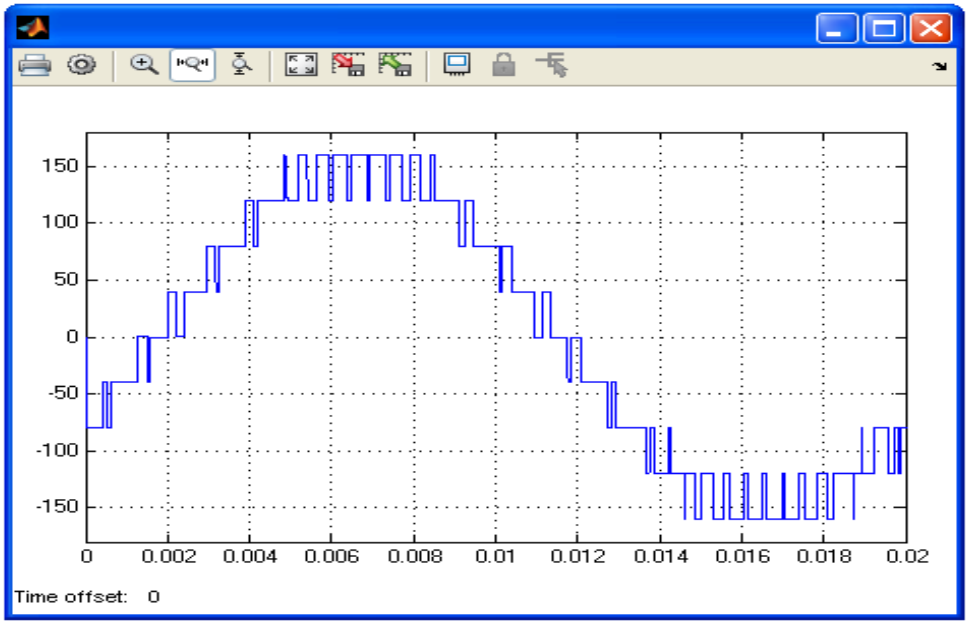


Fig. 5.35 One phase output from three phase HMLI third harmonic injection modulation technique

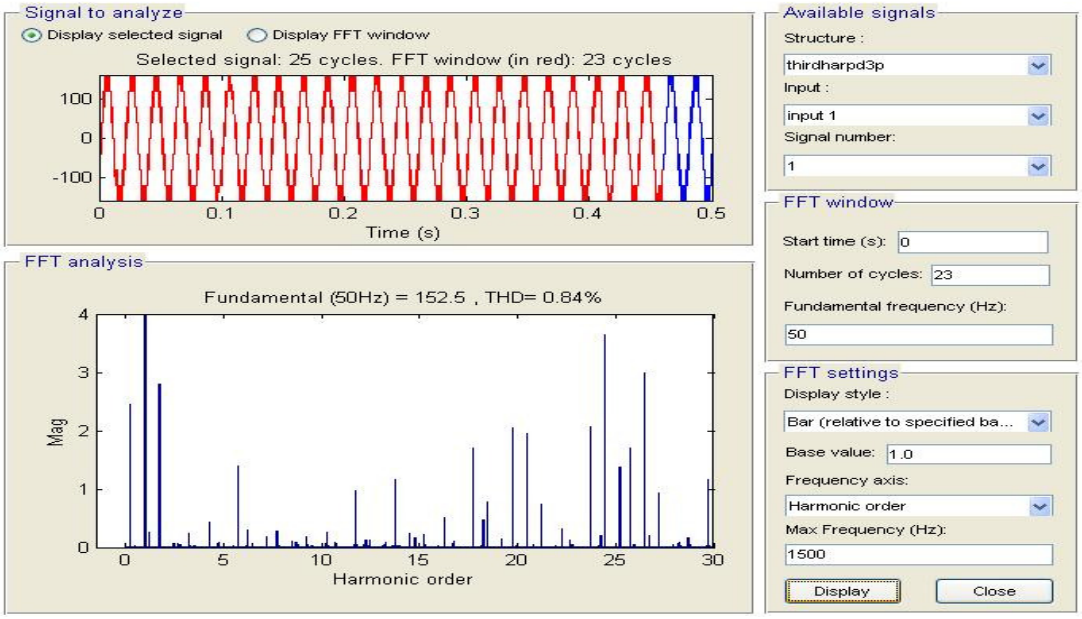


Fig. 5.36 FFT analysis and THD for HMLI with third harmonic injection modulation technique

Table 5.1 MATLAB simulation summary for HMLI

Phase	Modulation Technique	Output Levels	THD
Single	PD	5	1.17
	POD	5	1.21
	APOD	5	1.15
	PS	5	1.39
	HYBRID	5	1.52
	THIRD HARMONIC INJECTION	5	22.46
	ISPWM	5	28.82
Three	PD	9	0.98
	POD	9	.99
	APOD	9	1.02
	PS	9	1.23
	HYBRID	9	1.41
	THIRD HARMONIC INJECTION	9	0.84

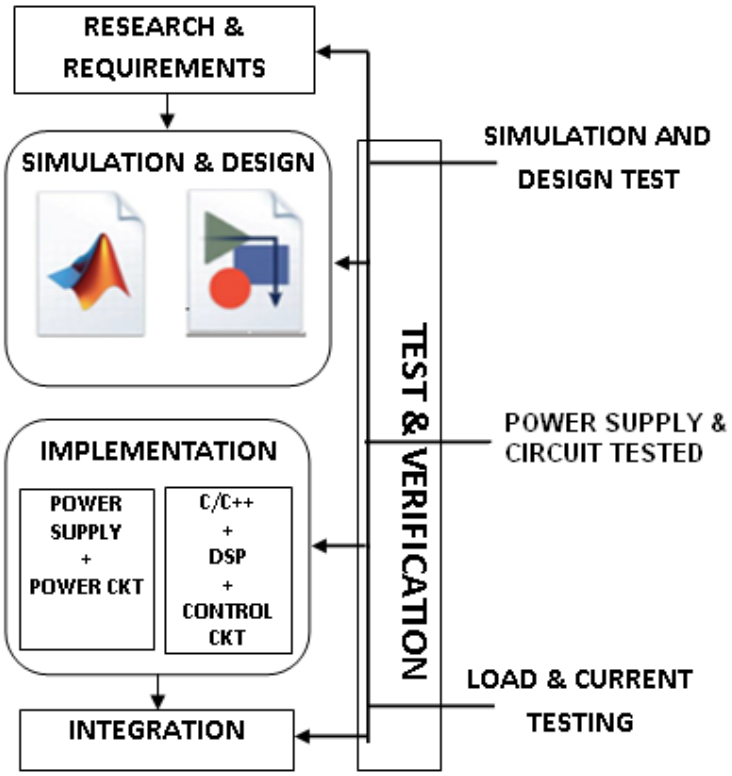
5.3 SUMMARY

Different MATLAB simulations are done for selected hybrid multilevel inverter. Comparison is done on basis of THD. Results are summarized in Table 5.1. It is observed that for particular modulation index THD does not vary much with change in modulation technique. Number of stages, number of switches, number of sources, number of capacitors, overall cost etc. are the selection criteria for given application.

CHAPTER 6

CONTROL SIGNAL GENERATION

Following block diagram shows the procedure for the simulation, control signal generation and implementation.



Block diagram for simulation, control signal generation and implementation

- Simulink model generated and optimal THD is obtained.
- Building of Simulink model with CCS3.3, code generated is loaded to Emulator xds510usb, control signal generation from DSP28335.
- Control signals obtained applied to buffer, opto isolation and driver circuits.
- Control signals generated are given to power circuit.
- Power circuit results are observed on DSO.

This chapter dicusses the processor used for gating signals applied to switches in power circuit. As discussed earlier 18 switches are there in 3 phase Hybrid Multilevel Inverter controlled separately with different modulation techniques as per requirement. Thus processor chosen should provide minimum 18 separate pulses at the output. Though complimentary pulses can be used but to avoid leg short circuiting and intentional delay separate pulses are used in this topology.

Analog control can be used but for implementation of various modulation techniques digital control is suggested. Control signals can be obtained using different high level languages like C/C++ programming. But as per advancement in technology control signals can directly be obtained using MATLAB SIMULINK Blocks with Code Composer Studio and Emulator. All these interfaces are discussed in detail.

This chapter describes steps involved in generation and application of control signals to power circuit.

6.1 DIGITAL SIGNAL PROCESSOR

Fig. 6.1 depicts EPB 28335. The EPB28335 is a stand-alone card allowing developers to evaluate the TMS320F28335 digital signal processor (DSP) to determine if it meets their application requirements. Furthermore, the module is an excellent platform to develop and run software for the TMS320F28335 processor. The EPB28335 is shipped with a TMS320F28335 DSP. The EPB28335 allows full speed verification of F28335 code. To simplify code development and reduce debugging time, a C2000 Code Composer Studio driver is provided. In addition, an onboard JTAG connector provides interface to emulators, with assembly language and ‘C’ high level language debug. Following features of EPB28335 and TMS320F28335 DSP can be summarized in brief [1-3].

- Fast, 150 MHz clock/instruction cycle.
- High speed A/D converter, 12.5 MHz max sample rate, 16 channels, 12-bits.
- 80-ns conversion rate (12.5 MHz)
- A/D includes two parallel sample and hold circuits.
- Nominally a 32-bit machine.
- 34 K words (16-bit) of on-chip static random access memory (RAM).
- 256 K words (16-bit) of flash read only memory (ROM).
- 6 high resolution (150 picosecond) pulse width modulators. Can readily be used to implement D/A converters.

- Possesses a rich set of peripheral interface devices
- 6 high resolution pulse width modulator outputs
- Three 32-bit timers
- Serial port peripherals
- On chip 32-bit floating point unit
- 68K bytes on-chip RAM
- 512K bytes on-chip Flash memory
- On board 1M bytes (64kx16) off-chip SRAM memory
- 9-volt only operation with supplied AC adapter
- On board Power-On LED indication
- Connector for Watchdog timer output
- 20 Pin (10x2 header) Connector for 16 GPIO lines
- DB25 Connector for 8 Digital Input and 8 Digital Output interface with +5V compatibility
- Error + Trip +5V compatible connector for Inverter control module
- On board USB Connector for UART-A interface with LED indication
- On board USB for Flashing
- On board DB9 connector for UART-A interface
- On board LED indication for Transmit and Receive data at UART-A
- On board 3 pin header for UART-B interface
- On board DB9 connector for CAN-A interface (Loop back mode possible)
- On board 4 pin header for CAN-B interface (Loop back mode possible)
- On board DB9 connector for 6 channel capture interface
- On board DB25 connector for 12 channel PWM interface
- On board DB15 connector for 8 Channel On-Chip ADC-A interface (with 3V protection using Op-Amps with unity gain output)
- On board DB15 connector for 8 Channel On-Chip ADC-B interface (with 3V protection using Op-Amps with unity gain output)
- On board Potentiometer to test On-Chip ADC
- On board DB9 connector for 4 channel SPI based External DAC interface
- On board I2C based Off-Chip EEPROM interface
- On board I2C based Off-Chip RTC interface

- On board Reset Switch with LED indication
- On board Switch for Run/Program mode switching
- On board Switch for boot mode selection
- On board IEEE 1149.1 JTAG emulation connector (7x2 pins) with LED indication
- Test points for All the PWM channels
- Test points for All the ADC channels
- Test points for Power signals
- On board LED at GPIO Pin as GPIO Test point
- 88 configurable general purpose I/O (GPIO) pins

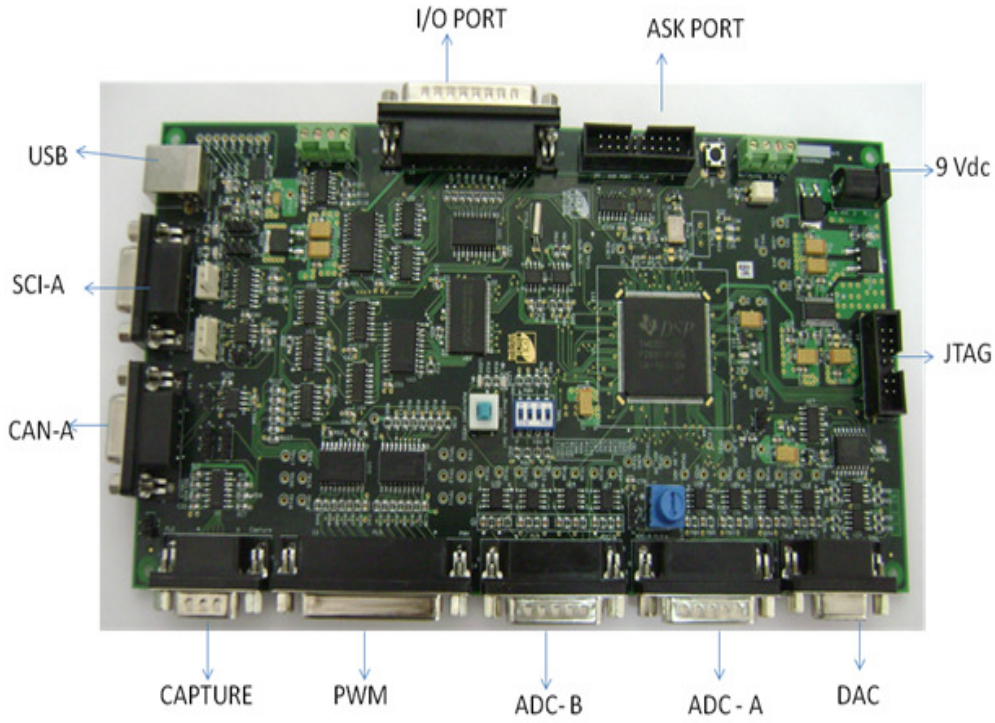


Fig. 6.1 EPB 28335 with peripherals

On the 2833x/2823x devices, the GPIO signals are assigned to 32-bit ports. The GPIO control and data registers have been moved from peripheral frame 2 (16-bit access only) to peripheral frame 1, which allows for 32-bit as well as 16-bit operations on the registers. The GPIO MUX logic has been redesigned to allow for a higher level of peripheral multiplexing. The 2833x/2823x GPIO MUX can multiplex up to three independent peripheral signals into a signal GPIO pin, in addition to providing individual pin toggling I/O capability. There are two MUX registers for each GPIO port. For each of the GPIO pins one can enable or disable an internal pullup resistor through software.

Thus features utilised are GPIO and I/O ports for 18 control signals. JTAG for interfacing emulator with DSP.

6.2 FLOW OF CONTROL SIGNALS

As discussed control signals are obtained in following steps:

Step 1 : Open CCSSTUDIO Setup as shown in Fig. 6.2.

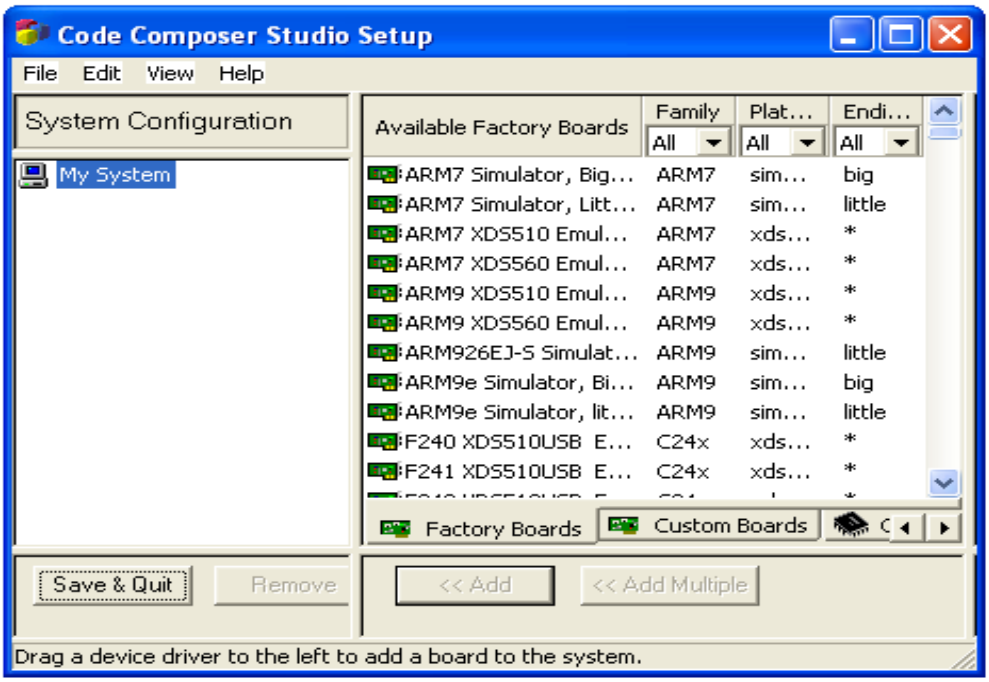


Fig. 6.2 CCS setup

Step 2: Select family, platform and add to system Do the settings as shown in Fig. 6.3.

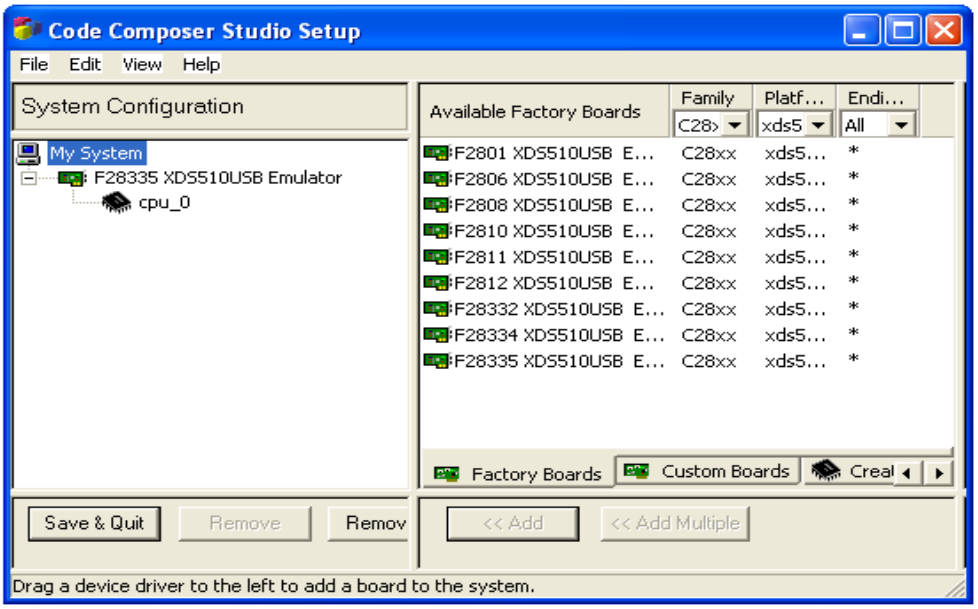


Fig. 6.3 Emulator selection

Step 3: Save and quit.

Step 4: MATLAB SIMULINK model execution(.mdl file).

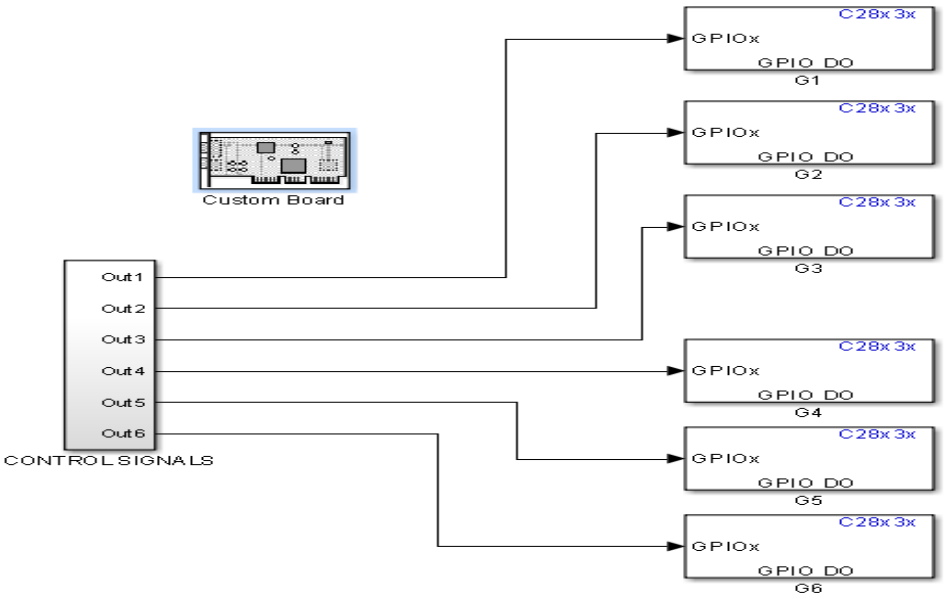


Fig. 6.4 MATLAB SIMULINK model for control signals

Custom board is selected from target prferences and as DSP is 28335 hence board selected is C2000 and processor is F28335. Fig. 6.4 shows MATLAB SIMULINK model for generation of control signals.

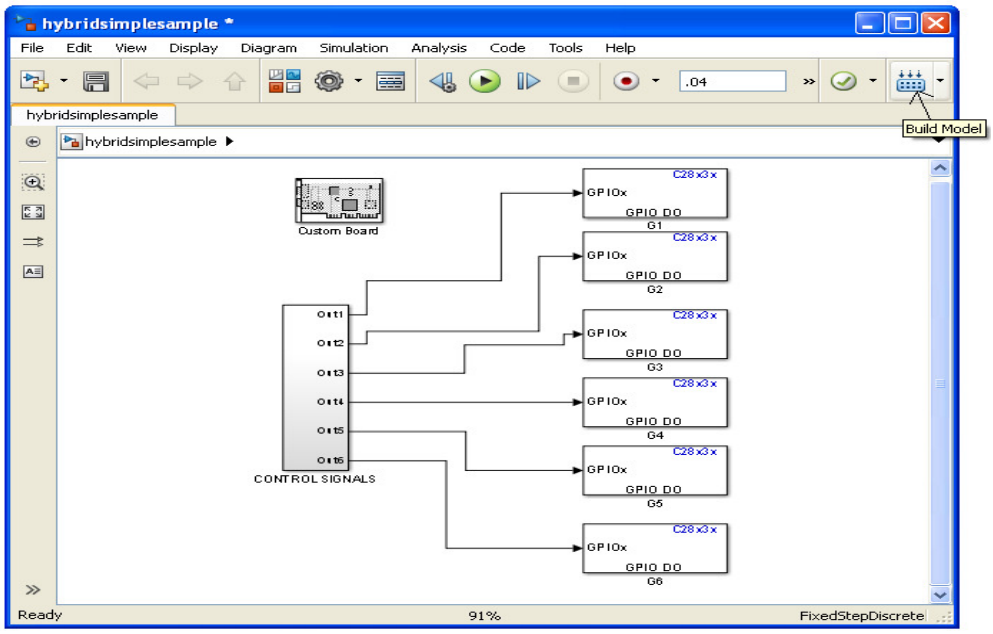


Fig. 6.5 Building model in MATLAB SIMULINK

In Fig. 6.4 six signals are shown similarly 18 signals can be obtained. GPIO pins and PWM port used for obtaining pulses are summarized as below: GPIO 48-52, 54,

57,59-63 and PWM 1A,1B,2A,2B,3Aand 3B configured to GPIO 0,1,2,3,4 and 5 are used for control signals.

Step 5: After execution of .mdl file build model as shown in Fig. 6.5. Project is built in CCS as shown in Fig. 6.6 and loaded to emulator with no error and control signals are loaded in DSP. Thus 3.3V pulses are obtained GPIO pins specified.

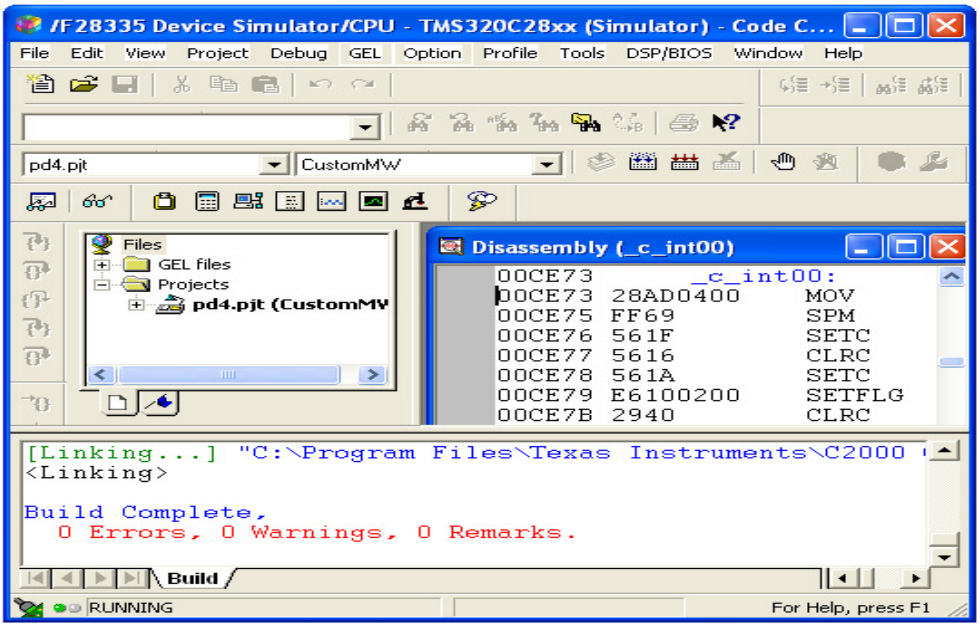


Fig. 6.6 Project built in CCS

6.3 DRIVER CIRCUIT

The gate pulses obtained from DSP go through buffer, isolation and driver stage before reaching to the power devices. As DSP can drive maximum up to 200mA current and signals taken are 18 hence buffer is required. The isolation is must when gate pulses are given to power devices connected in inverter configuration. The isolation is normally provided to gate pulses through optocouplers, which isolates power circuit and low power control circuit optically. Further these optically coupled signals are given to the driver circuit. The gate pulse, which is given to the MOSFET, is with respect to the source terminal. Fig. 6.7 shows circuit for buffer, isolation and driver which are described in brief.

Circuit is designed as per requirement of gate pulse. Buffer selected [4] can drive maximum 6 signals hence for 18 pulses three buffers are used. Buffer supply is 5V. 4049 inverting buffer is used. Component list is given in Table 6.1. R_1, R_2, R_3 and R_4 are selected as standard current limiting, pull-up resistors. Similarly C_1 and C_2 are by pass capacitors while C_3 is used for floating supply as per requirement of driver IC IR2110

[5]. Diode D_2 is fast switching diode for boost up. High speed opto isolator 2630 is used for isolation [6].

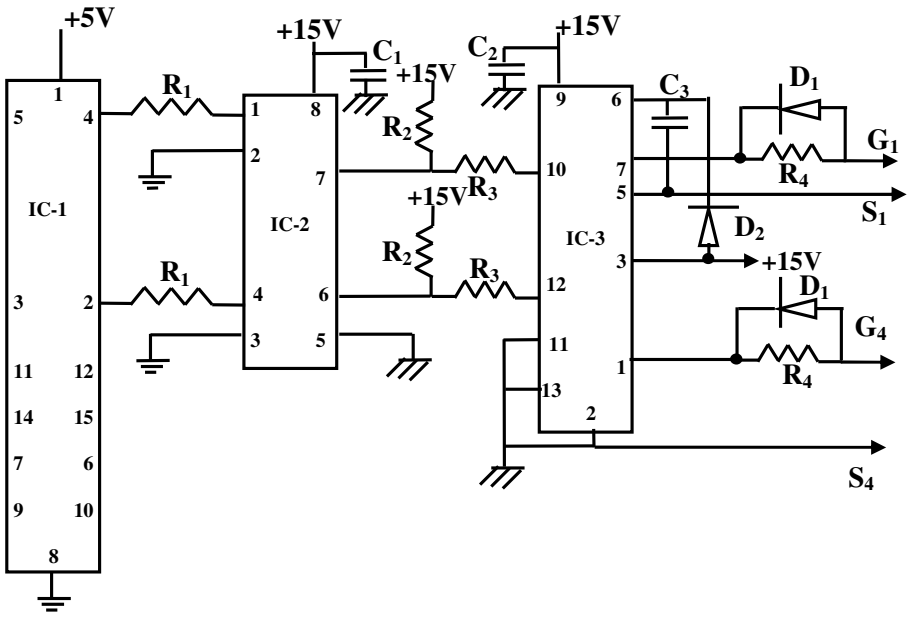


Fig. 6.7 Control circuit for generating gating signal

Table 6.1 Component List

Component	Value
R_1	330 Ω
R_2	10 kΩ
R_3	1 kΩ
R_4	3.3 kΩ
C_1	0.1 μF
C_2	0.47μF
C_3	100μF
D_1	IN4148
D_2	11DF4
IC-1	4049
IC-2	2630
IC-3	IR2110

6.4 SUMMARY

In this chapter, procedure to obtain control signals is described. Signals obtained from DSP are 3.3V compatible which are not enough for gate drive hence buffer and driver circuits are introduced. As power circuit operates at very high voltage, isolation is compulsory hence opto isolator is used.

CHAPTER 7

POWER CIRCUIT DESIGN

This chapter describes design of hybrid multilevel inverter. Single phase hybrid multilevel inverter is designed and is repeated for three phase. Regulated power supply is designed for 40 V and 80 V DC output. As discussed in previous chapter gating signals are applied through digital signal processor, buffer, isolation and driver.

7.1 DESIGN OF HYBRID MULTILEVEL INVERTER

HMLI is designed for 110V, 5A rating. Gate pulse is obtained from circuit shown in previous chapter. MOSFET is chosen for high frequency switching, high voltage and high current operation. As shown in Fig. 7.1 separate DC voltages are connected.

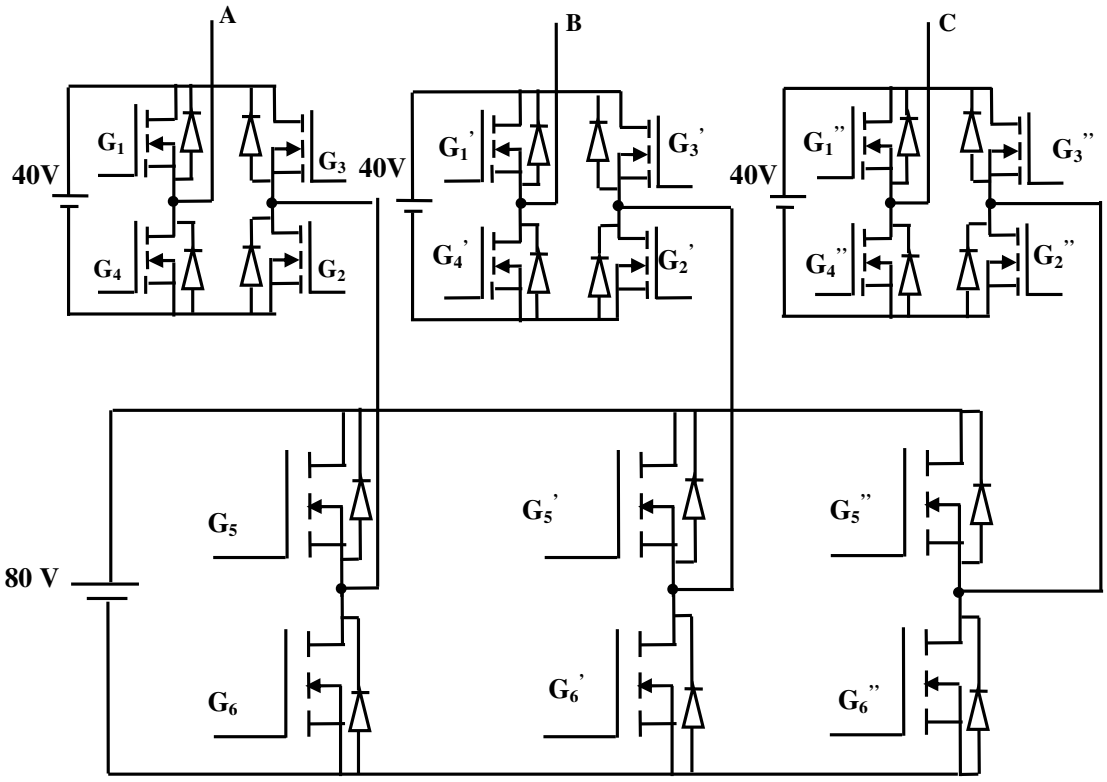


Fig. 7.1 Three phase hybrid multilevel inverter circuit diagram

7.1.1 DESIGN OF SINGLE AND THREE PHASE HYBRID MULTI LEVEL INVERTER

As shown in Fig 7.2 half bridge inverter is connected with H bridge inverter to form single leg of HMLI. As discussed switching is done at approximately 2.1 kHz frequency. Care is taken that switch has low saturation voltage and breakdown voltage is two to three times the supply voltage. Similarly for 3 phase such design is repeated.

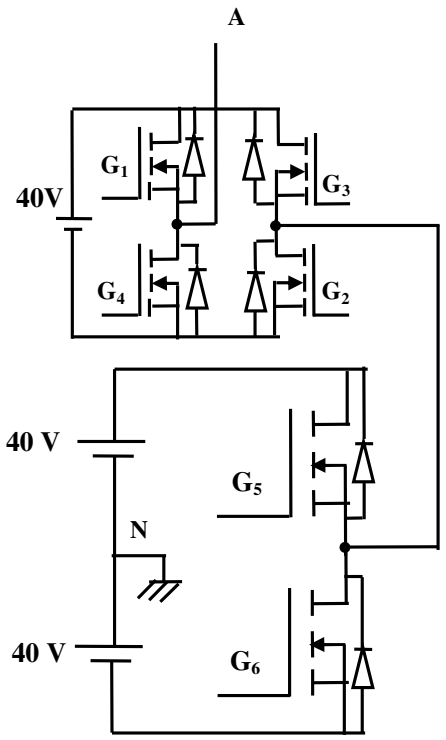


Fig. 7.2 Single leg of hybrid multilevel inverter circuit diagram

7.1.2 MOSFET SELECTION

As circuit operates at 110V rms and 5A current MOSFET is chosen accordingly.

IRF840N Power MOSFET is used. Features of IRF840 [1] are as follows:

-V_{DS} 500V

-I_D 8A(continuous)

-R_{DS} (on) Low i.e 0.85 Ω

-Exceptional dv/dt

-Low Gate Charge

-Application Oriented Characterization

- Low gate drive requirements

100KΩ resistance is connected as high impedance gate of MOSFET

K-1 type heat sink is used for MOSFET

7.1.3 DESIGN OF MOSFET SNUBBER

An RC snubber, placed across each switch can be used to reduce the peak voltage at turn-off and to damp the ringing. Design for snubber is given below.

f_s = 2 kHz

Edc = 40 V, i_L=2A

Let L = 25 μH

$t_f = 66x10^{-9}$ s

where t_f is fall time

fs switching frequency

$C = i_{L*}t_f / E_{dc}$

$= 6 * t_f / 40$

C = 0.01μF

$L = E_{dc}*t_r / i_L$

t_r = 1.26 μs

where t_r is rise time

$d_i/d_t = i_L/t_r$

= 1.58 A/μs

Switch ON

d_i/d_t = 0.395 A/μs

$R = \sqrt{(4*L/C)}$

R = 100 Ω

Hence values for snubber are chosen as 100 Ω,1W and 0.01μF/400V.

7.2 DESIGN OF REGULATED POWER SUPPLY

Step down transformers of rating 230V/45V and 230V/70V are used to obtain 40V and 80V DC respectively from voltage regulator. Current rating is 5A as design is for 110V rms from output with 5A current.

Controlled transistor series regulator circuit is designed and implemented as shown in Fig. 7.3 Components are chosen as per requirement. Selection of transistors T_1, T_2, T_3 is done on basis of V_{CEO}, gain and power rating from datasheet [2-5]. Due to high power dissipation heat sink is included in circuit.

Working principle can be explained as follows: Unregulated DC voltage is passed through filter capacitor C and bleeder resistances R_B and as per change in output load current regulation is obtained from regulator circuit. If current through load increases drop across R_6 increases which increases base current of T_3 thus increasing collector current of T_3, which increases base current of T_1, through T_2, thus finally reducing emitter current of T_1 and regulating output current and voltage. R_2, R_3 and C_2 form filter and current limiting path for T_3. Zener diode gives minimum emitter voltage of T_3 with C_1 as filter for zener diode. Component choice is done as per requirement. Darlington

pair of transistor T_1 and T_2 is control element and is called pass transistor as all load current flows through it. Zener diode and resistor R_1 act as reference element. The voltage divider R_5, R_6, and R_7 samples output voltage and delivers a negative feedback voltage to the base of transistor T_3 [6]. Design and practical readings for regulated power supply are given in Appendix A. While hardware setup is given in appendix B.

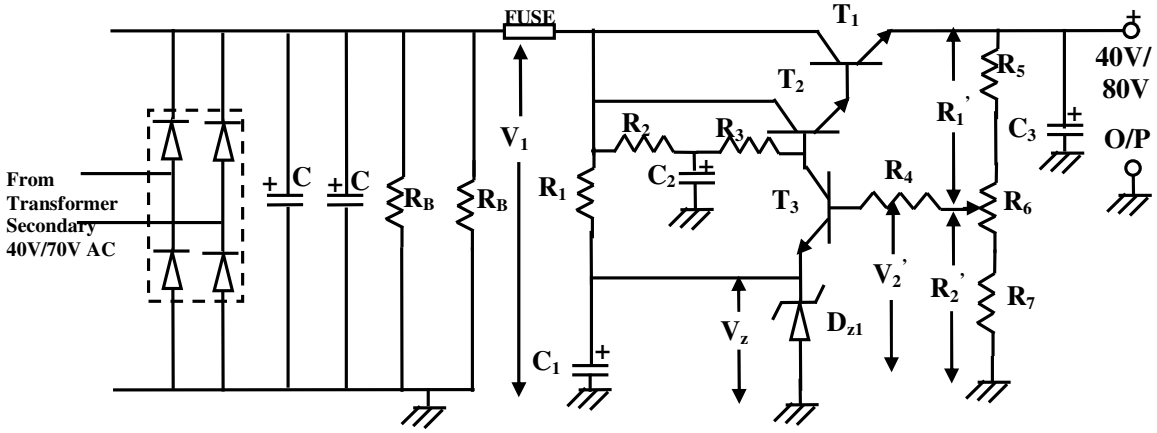


Fig. 7.3 Regulated power supply

Table 7.1 Component list

Component	Value
R_1	10 kΩ/1W-----22 kΩ/2W(for 80V)
R_2	470 Ω/0.5W
R_3	1 kΩ/0.5W
R_4	100 Ω/0.25W
R_5	6.2 kΩ------10 KΩ(for 80V)
R_6	500 Ω preset
R_7	1 kΩ
C_1	100 µF/16V
C_2	47µF/63V-----47µF/160V
C_3	100µF/63V
D_{z1}	6.2V/1W
T_1	2N3773----2N3773(for 80V)
T_2	2N3501----2N3773(for 80V)
T_3	BD139-----TIP122
Bridge rectifier 3510	35 A, 1000V
Bleeder resistance R_B	1 kΩ/10W ----2.2 kΩ/10W(for 80V)
Filter capacitor C	4700 µF/100V-----1800µF/160V(for 80V)

7.3 SUMMARY

In this chapter power circuit design is explained. Linear regulated power supply is also designed and its design is discussed. Hybrid multilevel inverter is designed. MOSFET switches were selected on design basis. Heat sink is selected as per dissipation. R-C snubber is also designed.

CHAPTER 8

EXPERIMENTAL RESULTS

In this chapter, results obtained from hardware implementation are compared with simulation results for selected scheme. Comparison is on basis of THD, output voltage obtained and fundamental voltage from FFT analysis. Hardware testing is done with lower as well as higher voltage. For lower voltage 12V batteries are taken as supply for single phase as well as three phase. Initially single leg is tested with and without modulation. Similar three cards are made and tested individually then three phase connections are done. In three phase output is obtained for different modulation techniques which have been already discussed in previous chapters. Modulation index is taken either 0.9 while frequency modulation index is 21.Control signals are applied using SIMULINK-CCS3.1-EMULATOR C2000 USB- DSP KIT 28335 as discussed in chapter 6.

Output is saved in DSO in .bmp and .csv extension. The file saved in .csv format is imported in MATLAB R2013a and then THD is found. Limitations of this method are: i) maximum 1024 points are saved ii) first half cycle output reconstructed from such points is not proper iii) maximum two cycles are obtained from points saved in .csv format.

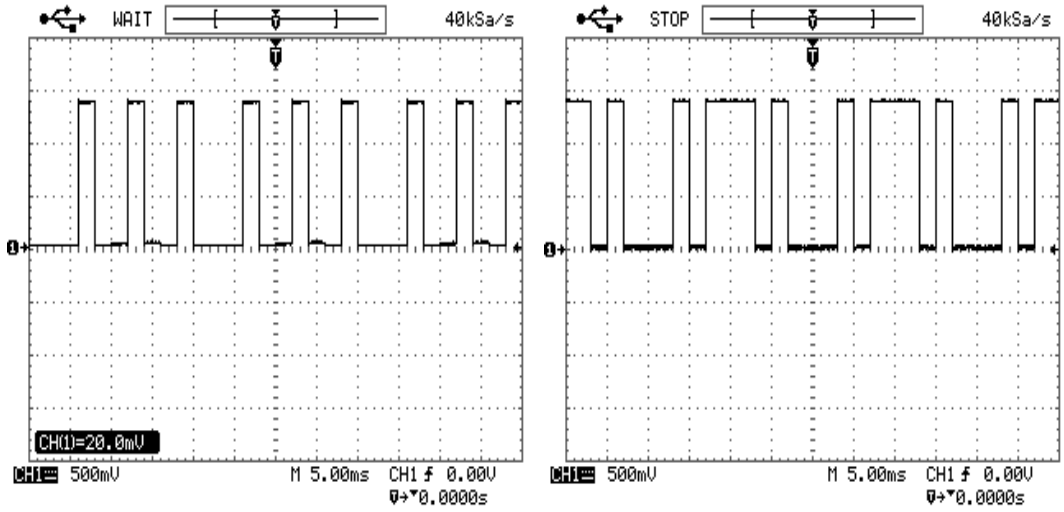
Further sections describe different outputs for various ratings of voltage and current with different gating pulses for selected configuration of single phase and three phase HMLI.

8.1 HARDWARE RESULTS FOR SINGLE PHASE HYBRID MULTILEVEL INVERTER

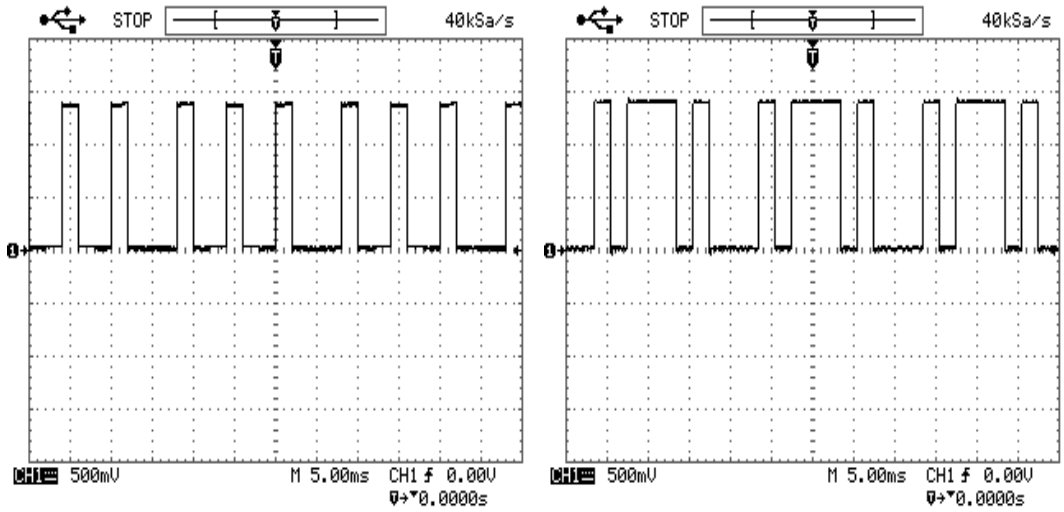
Single phase hybrid multilevel inverter is tested on 12V batteries and respective five level output is obtained. Output is taken for R and R-L load.

8.1.1 HARDWARE OUTPUT FOR SINGLE PHASE HMLI WITHOUT MODULATION

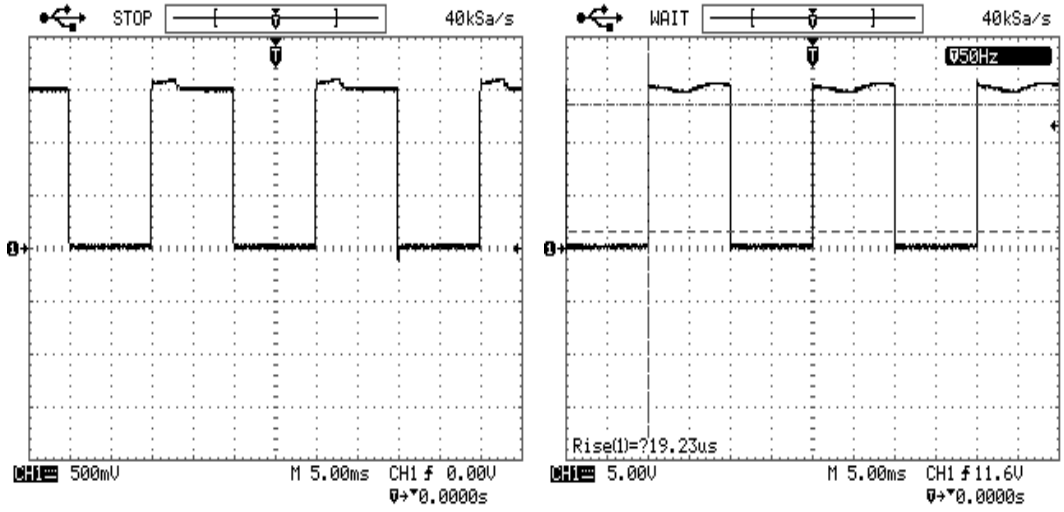
Fig 8.1 shows control signals for six switches. Fig 8.2 shows five level output 220 Ω-½ Watt resistor connected as load. Fig. 8.3 is THD obtained from .csv file imported to MATLAB.



(a) G_1 **(b) G_2**



(c) G_3 **(d) G_4**



(e) G_5 **(f) G_6**

Fig. 8.1 Control signals for single phase HMLI without modulation

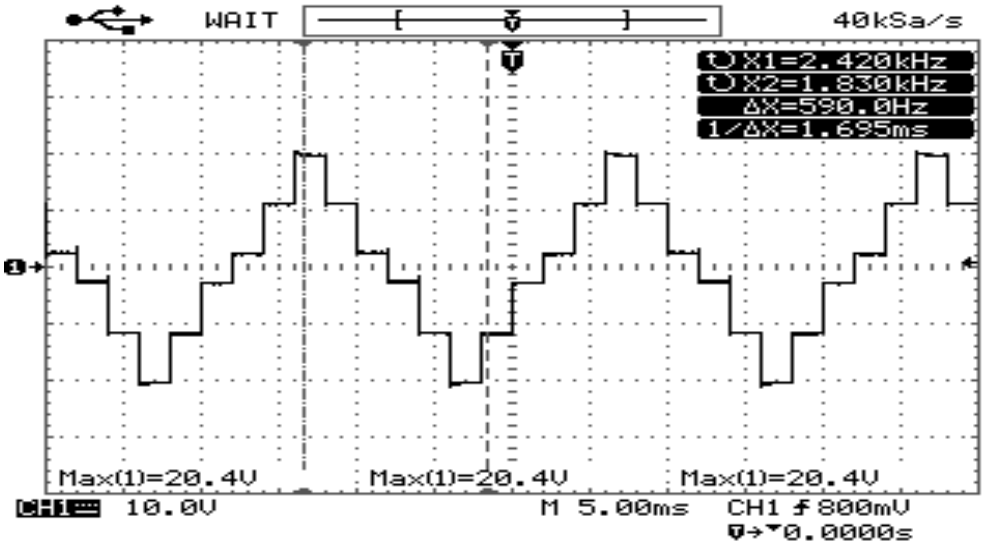


Fig. 8.2 Five level output for single phase HMLI without modulation

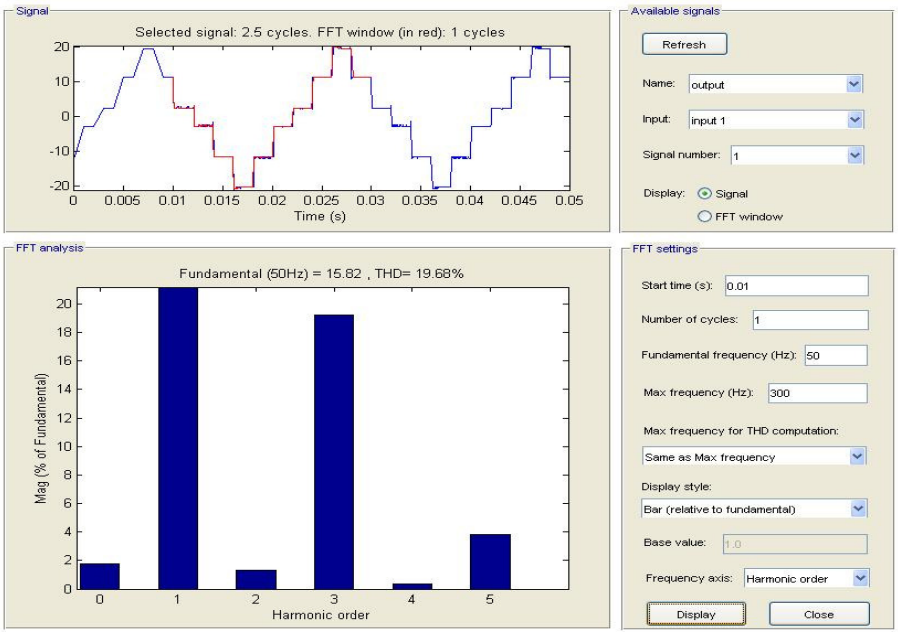
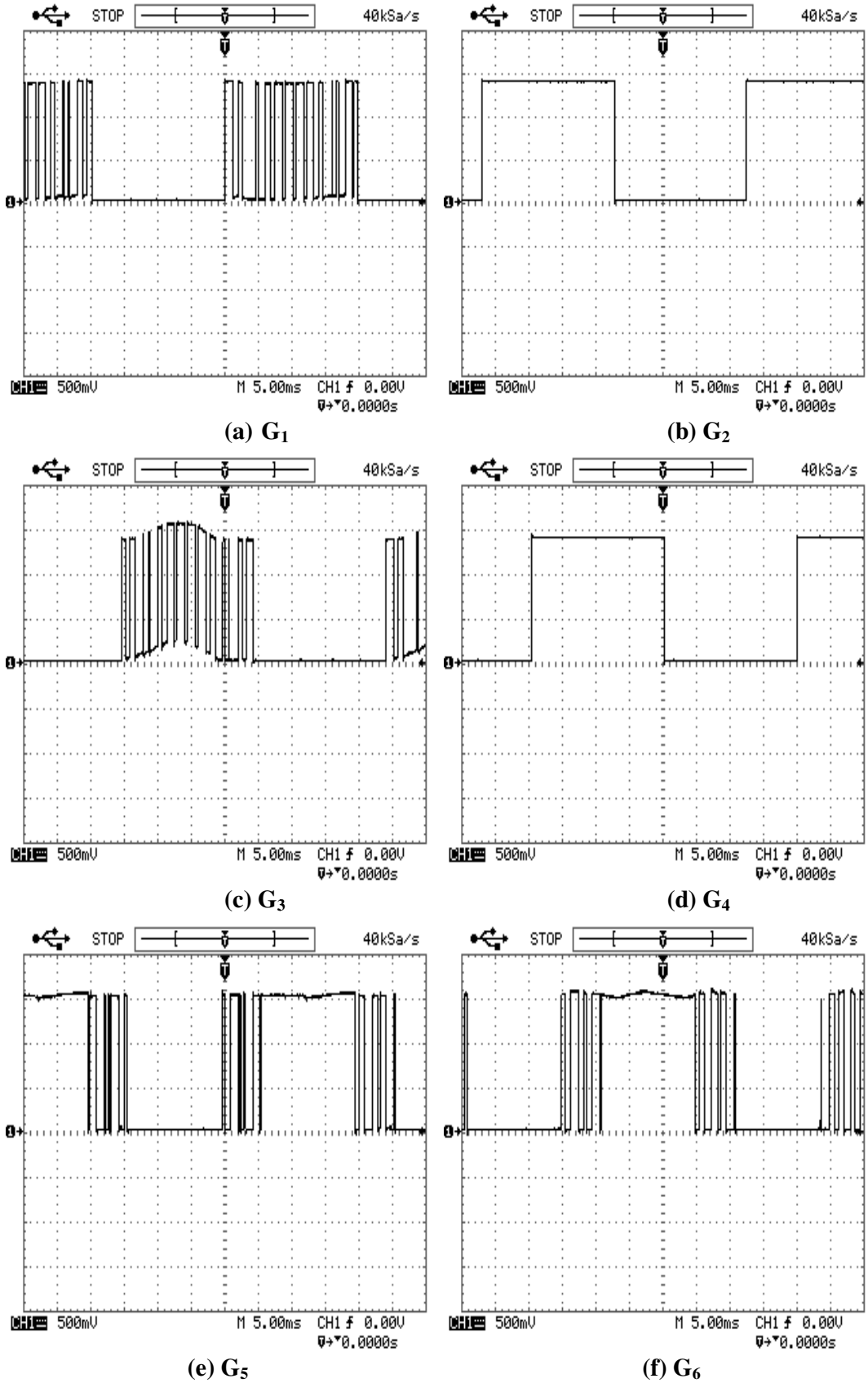


Fig. 8.3 FFT analysis and THD for single phase HMLI without modulation

8.1.2 HARDWARE OUTPUT FOR SINGLE PHASE HMLI WITH PD MODULATION TECHNIQUE

Fig 8.4 shows control signals for six switches. Fig 8.5 (a) shows five level output across 220 Ω- 1 Watt resistive load. Fig 8.5 (b) shows five level output across R-L load. Fig. 8.6 shows current through RL load for single phase HMLI with PD modulation technique. Fig 8.7 (a) is five level output with FFT for R load as mentioned above. Control signals are given at sample rate of 10 kHz which is changed to 100 kHz for better resolution as shown in Fig 8.7 (b). Fig. 8.8 is THD obtained from .csv file imported to MATLAB. Fig. 8.9 shows similar output for second card.

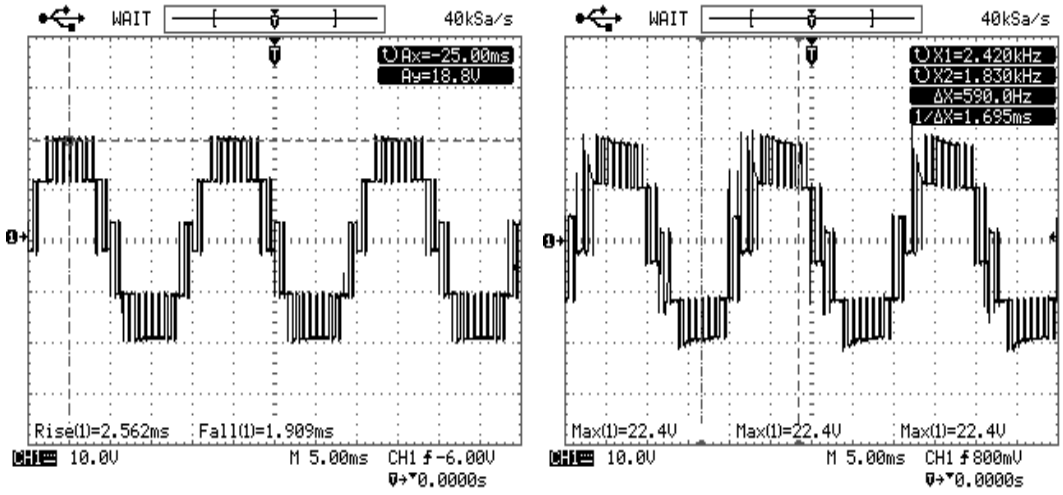


(a) G_1 **(b) G_2**

(c) G_3 **(d) G_4**

(e) G_5 **(f) G_6**

Fig. 8.4 Control signals for single phase HMLI with PD modulation technique



(a) R load **(b) R-L load**

Fig. 8.5 Single phase HMLI output with PD modulation technique

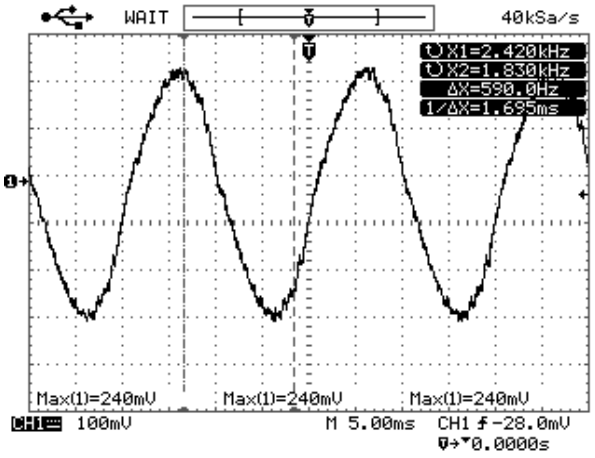
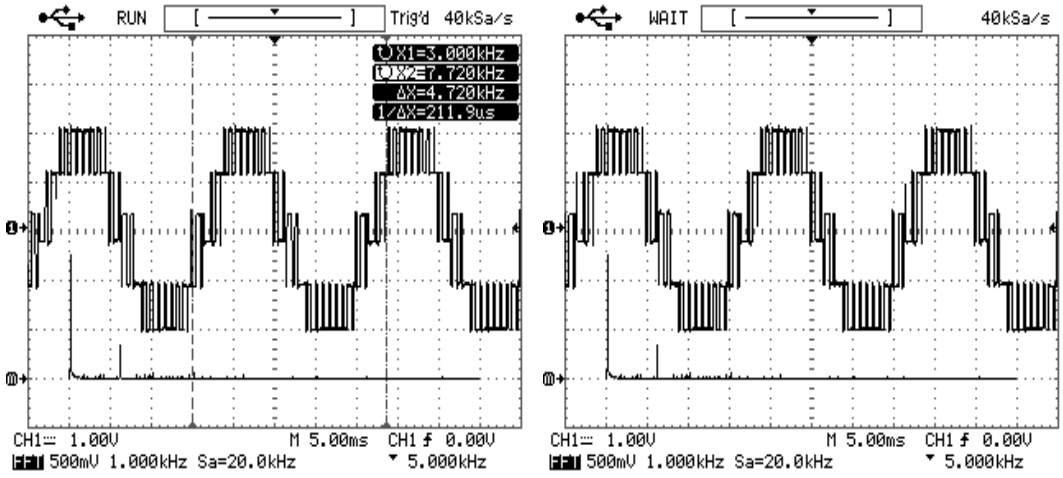


Fig. 8.6 Current through RL load for single phase HMLI with PD modulation technique



(a) Sample rate=10 kHz **(b) Sample rate=100 kHz**

Fig. 8.7 Single phase HMLI output and FFT with PD modulation technique for R load

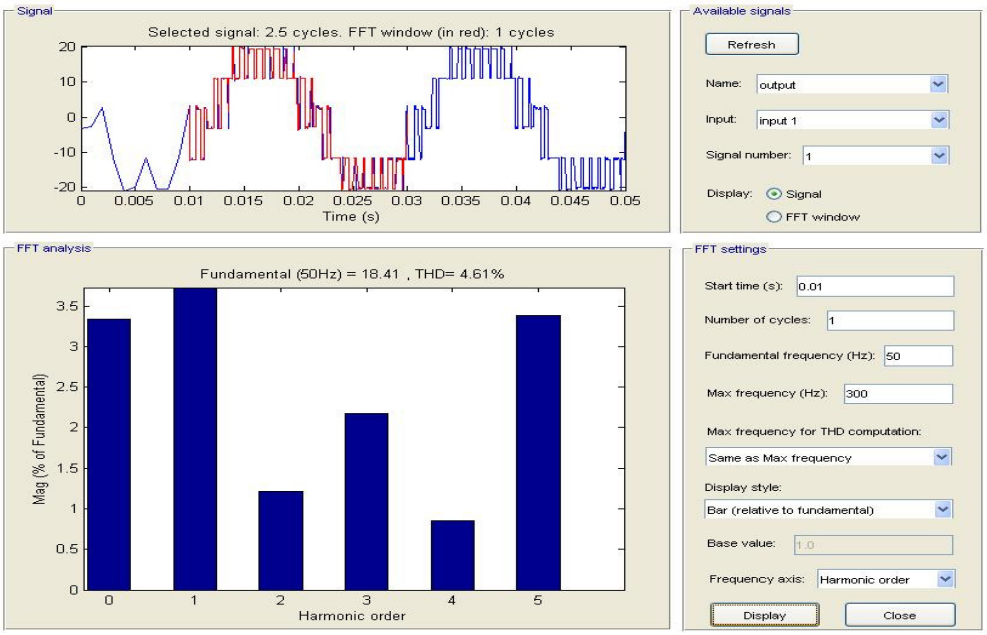


Fig. 8.8 FFT analysis and THD for single phase HMLI with PD modulation technique

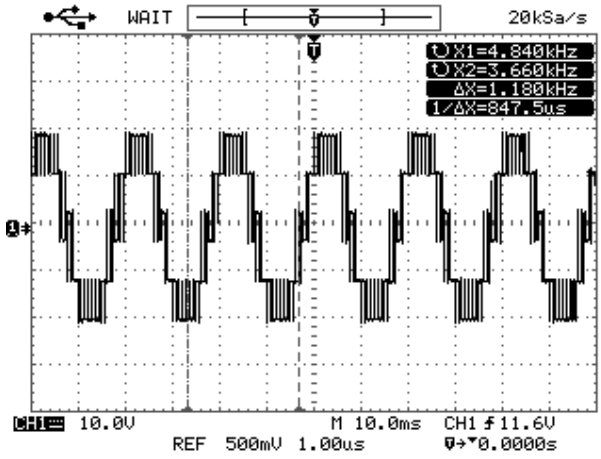


Fig. 8.9 Single phase HMLI output with PD modulation technique for R load

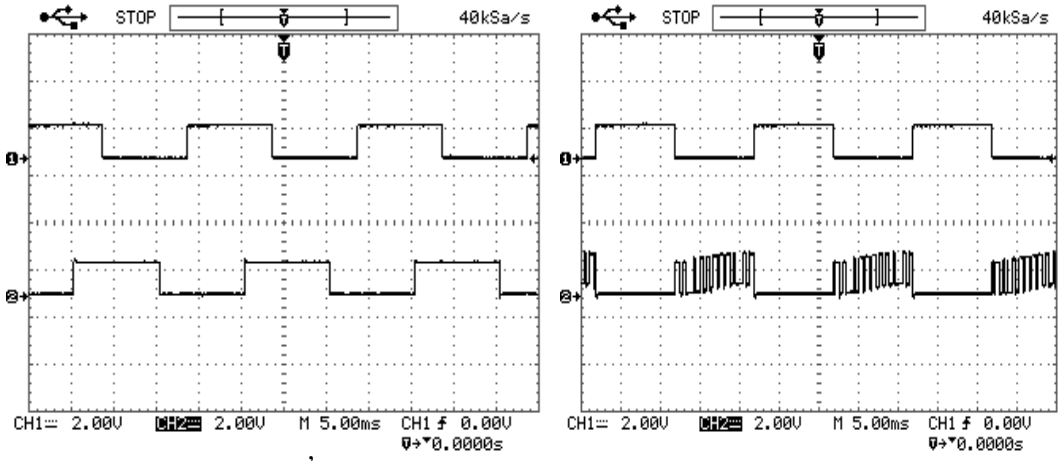
8.2 HARDWARE RESULTS FOR THREE PHASE HYBRID MULTILEVEL INVERTER

Three phase hybrid multilevel inverter is tested on 12V batteries and as discussed in chapter 7 DC supply for three phase inverter is double the H bridge supply hence two batteries in series are connected. Testing is also done with regulated power supplies of value 80V and 40V. Output is measured across resistive load in star configuration. Control signals are phase shifted by 120^0. Different modulation techniques are applied.

8.2.1 HARDWARE OUTPUT FOR THREE PHASE HMLI WITH PD MODULATION TECHNIQUE

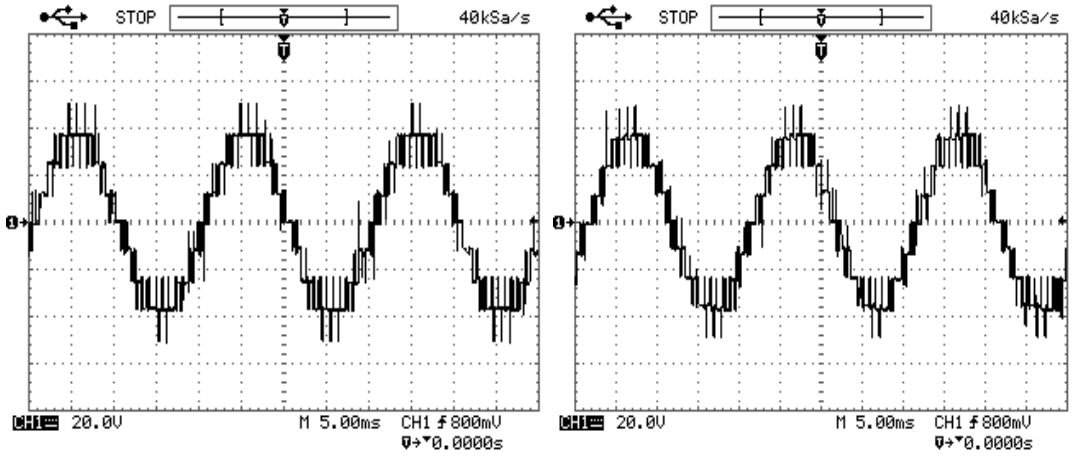
i) BATTERIES AS SUPPLY

Fig 8.10(a) shows control signals with PD modulation technique for switches of card 1 and card 2 which are 120^0 apart.



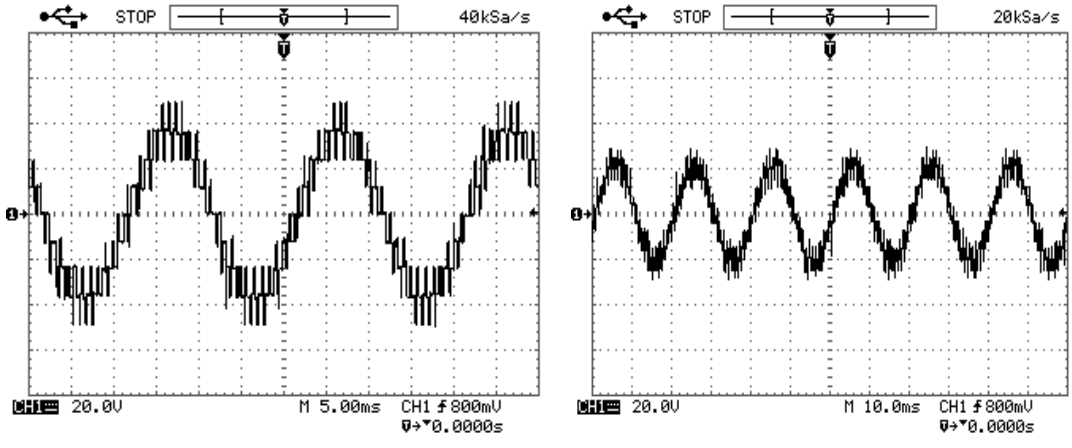
(a) G_2 G_2' **(b) G_2 G_3**

Fig. 8.10 Control signals for three phase HMLI with PD modulation technique



(a) v_{RY} **(b) v_{YB}**

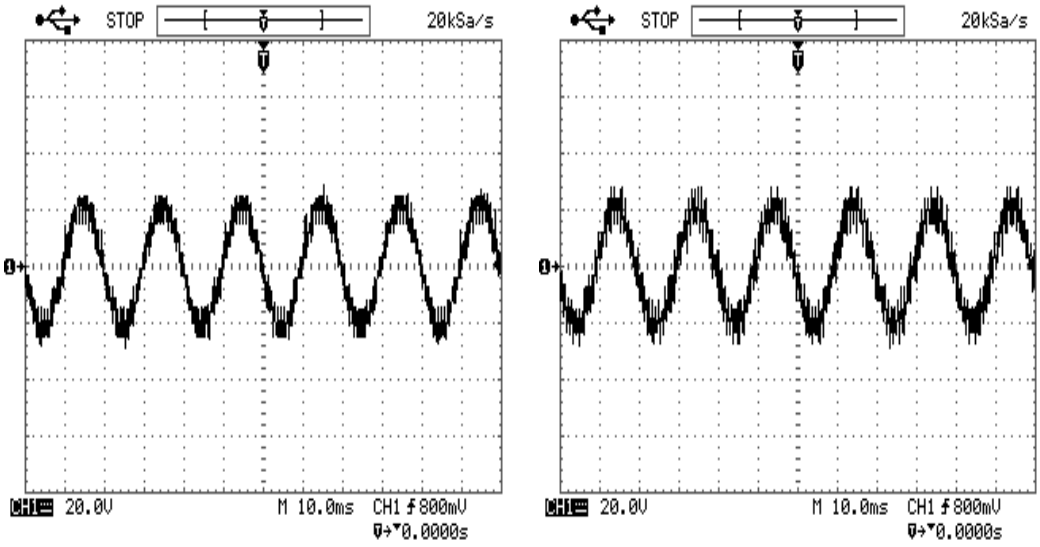
Fig. 8.11 Three phase HMLI output with PD modulation technique



(a) v_{RB} **(b) v_R**

Fig. 8.12 Three phase HMLI output with PD modulation technique

Fig 8.11(a) shows 9 level line to line output voltage(v_{RY}). 100 Ω-1W resistors are star connected as load. Fig 8.11(b) output voltage v_{YB}. Fig 8.12 (a) output voltage v_{RB}. Fig 8.12(b) shows 7 level v_R output voltage while Fig 8.13(a) and (b) shows 7 level output voltage v_Y and v_B respectively. Control signals were given at sample rate of 25 kHz due to limitation of MATLAB SIMULINK. Fig. 8.14 shows THD obtained from .csv file imported to MATLAB for one output and other values are mentioned in Table 8.1.



(a) v_Y **(b) v_B phase**

Fig. 8.13 Three phase HMLI output with PD modulation technique

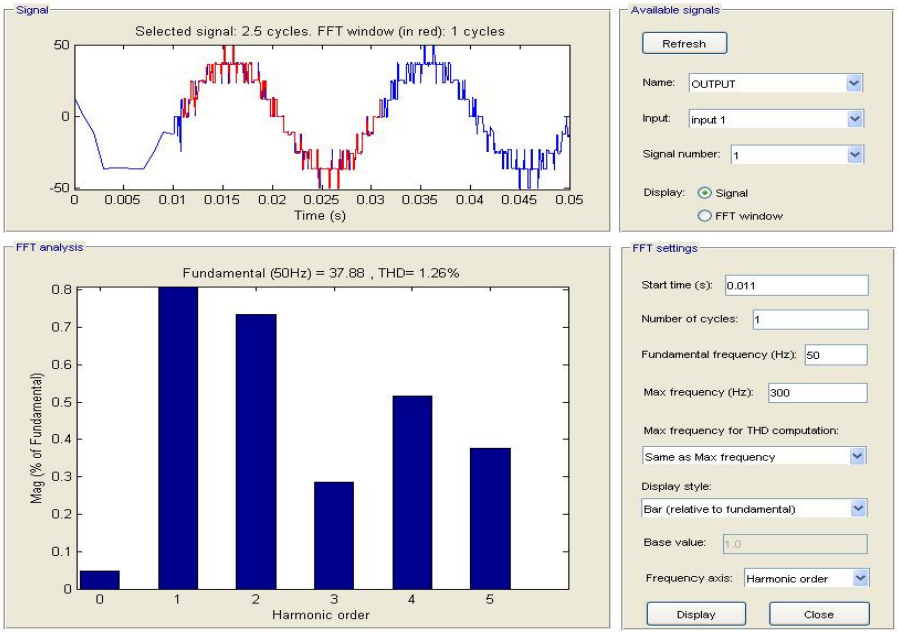
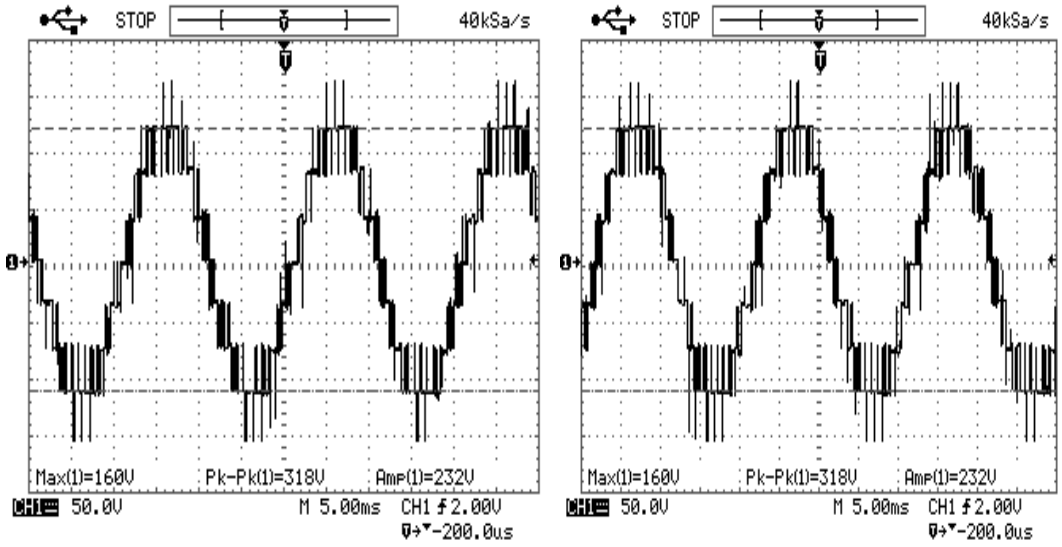


Fig. 8.14 FFT analysis and THD for 3 phase HMLI with PD modulation technique

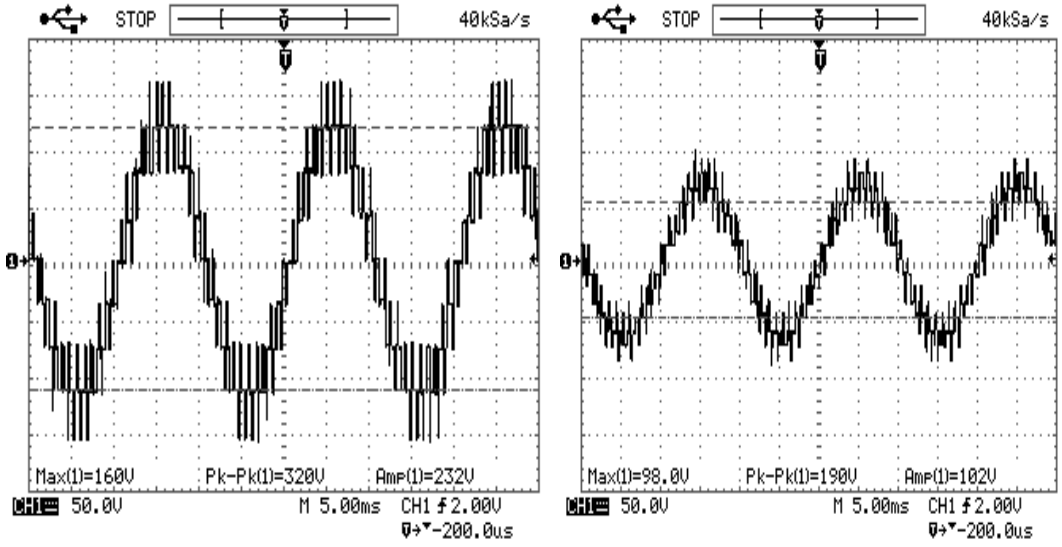
ii) REGULATED POWER SUPPLY

Fig 8.15(a) and (b) shows 9 level line to line output voltage v_{RY} and v_{YB} respectively. Three 1 kΩ- 10 W resistors are connected in parallel to obtain equivalent resistor of 330 Ω which are star connected as load. Fig 8.16 (a) output voltage v_{RB} and Fig 8.16 (b) shows 7 level v_B phase output voltage. Control signals were given at sample rate of 25 kHz due to limitation of MATLAB SIMULINK. Fig. 8.17 is THD obtained from .csv file imported to MATLAB for one output and other values are mentioned in Table 8.1.



(a) v_{RY} **(b) v_{YB}**

Fig. 8.15 Three phase HMLI output with PD modulation technique 330 Ω



(a) v_{RB} **(b) v_B**

Fig. 8.16 Three phase HMLI output with PD modulation technique 330 Ω

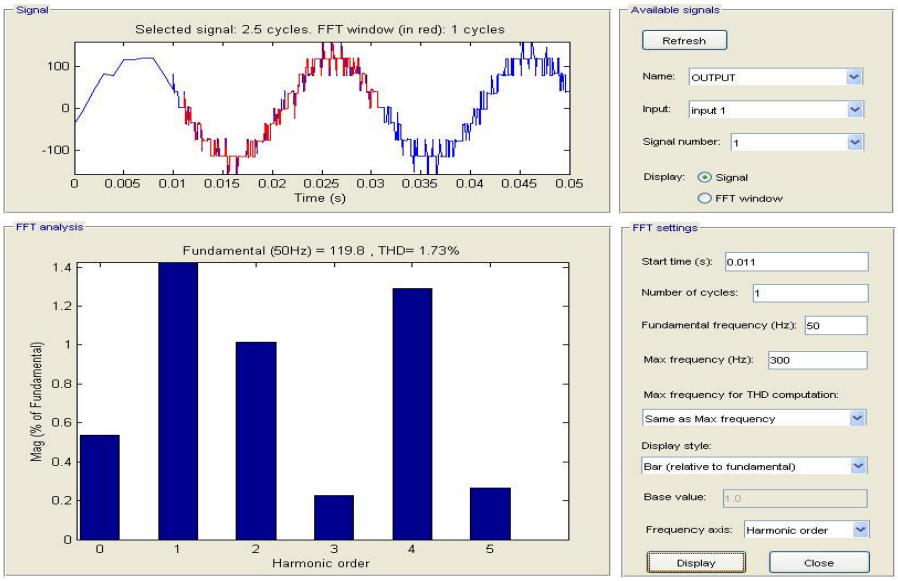
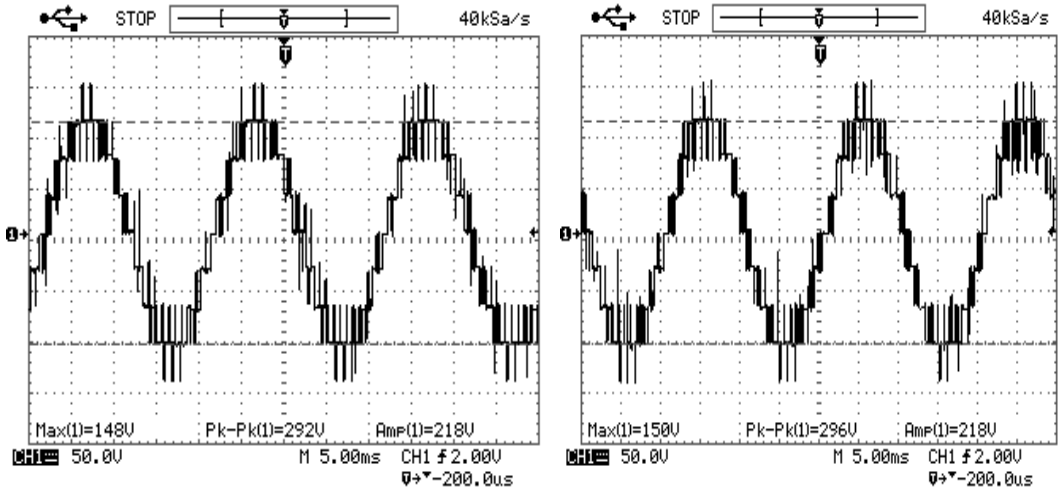


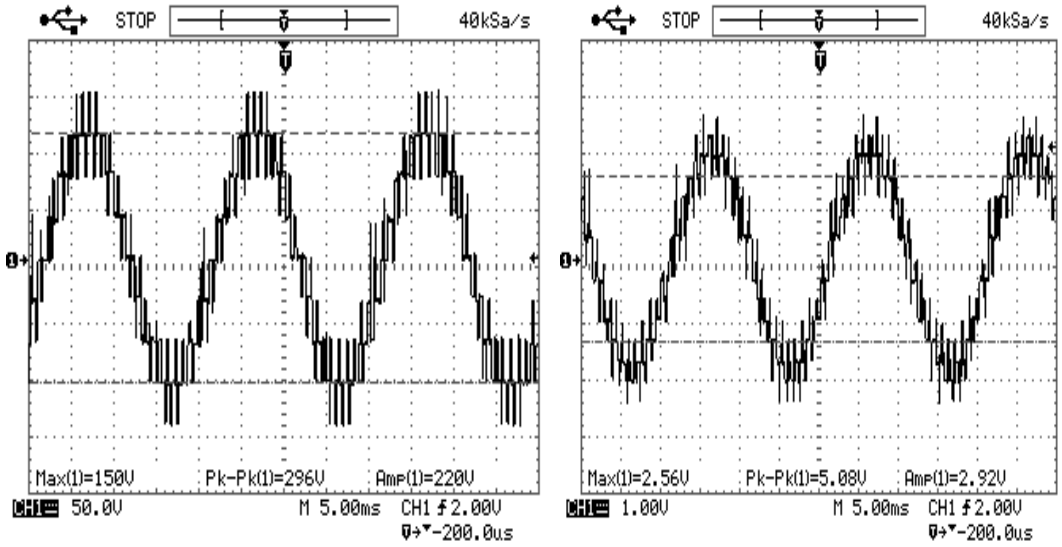
Fig. 8.17 FFT analysis and THD for three phase Line to line voltage for RY 330 Ω star load

Fig 8.18 (a) shows 9 level line to line output voltage(v_{RY}). 33 Ω- 1000 W heater coil are star connected as load. Fig 8.18 (b) shows output voltage v_{YB}. Fig 8.19 (a) shows output voltage v_{RB}. Control signals were given at sample rate of 25 kHz due to limitation MATLAB SIMULINK. Fig. 8.21 is THD obtained from .csv file imported to MATLAB for one output and other values are mentioned in Table 8.1. Fig. 8.19 (b) shows output current i_R measured across 1 Ω resistor connected in series with load. Fig. 8.20(a) and (b) show output current i_Y and i_B respectively.



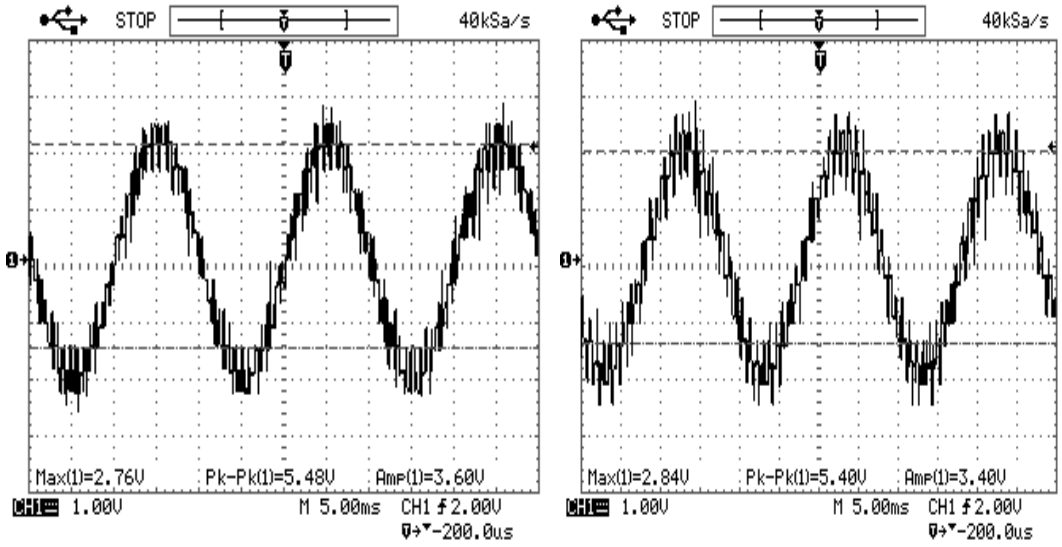
(a) v_{RY} **(b) v_{YB}**

Fig. 8.18 Three phase HMLI output with PD modulation technique 33 Ω



(a) v_{RB} **(b)** i_R

Fig. 8.19 Output voltage and current for Three phase HMLI with PD modulation technique



(a) i_Y **(b)** i_B

Fig. 8.20 Output current for three phase HMLI with PD modulation

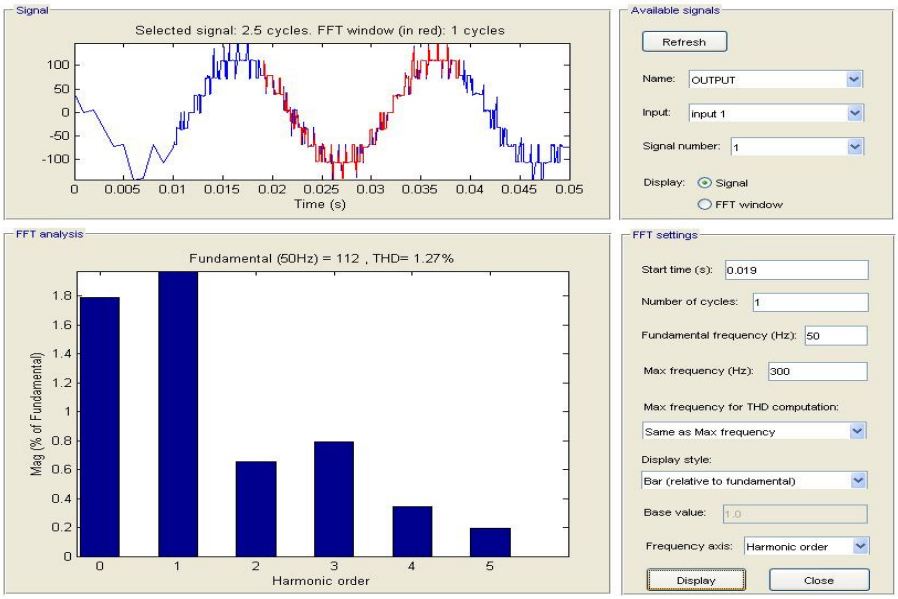
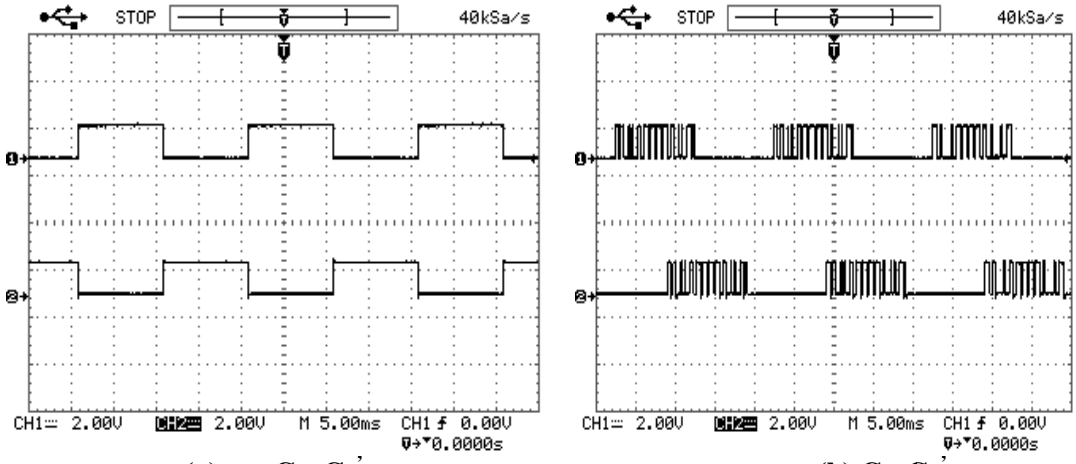


Fig. 8.21 FFT analysis and THD for 3 phase HMLI with PD modulation technique

8.2.2 HARDWARE OUTPUT FOR THREE PHASE HMLI WITH POD MODULATION TECHNIQUE

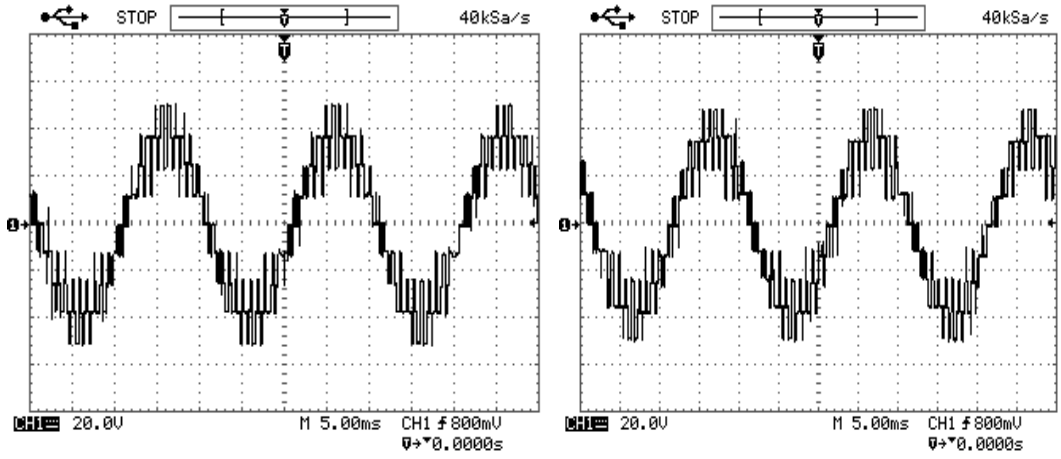
i) BATTERIES AS SUPPLY

Fig 8.22(b) shows control signals with POD modulation technique for switches of card 1 and card 2 which are 120^0 apart. Fig 8.23(a) shows 9 level line to line output voltage(v_{RY}). 100 Ω- 1 W resistors are star connected as load. Fig 8.23(b) shows output line voltage. Fig 8.24 (a) output voltage v_{RB}. Fig 8.24 (b) shows 7 level v_R phase output voltage while Fig 8.25 (a) and (b) show 7 level phase voltage v_Y and v_B respectively. Control signals were given at sample rate of 25 kHz due to limitation of MATLAB SIMULINK.



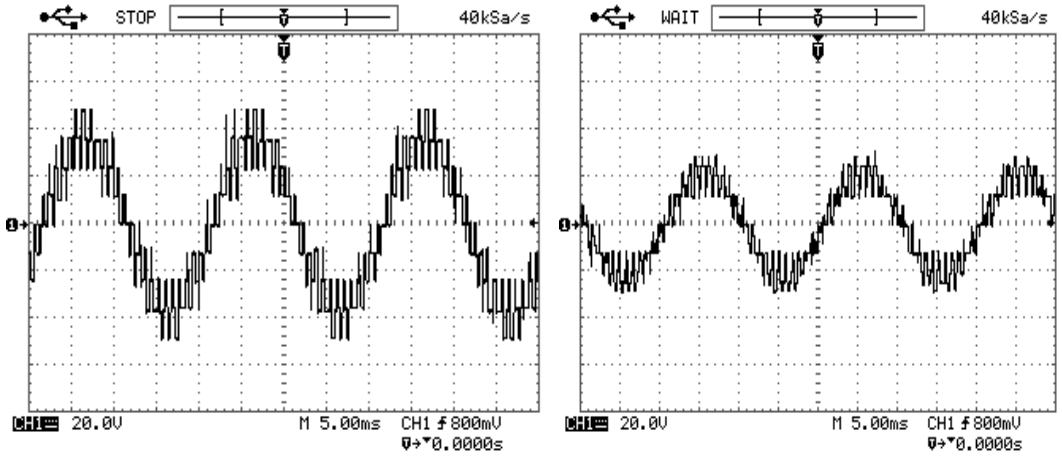
(a) G_2 G_2' **(b) G_3 G_3'**

Fig. 8.22 Control signals for three phase HMLI with POD modulation technique



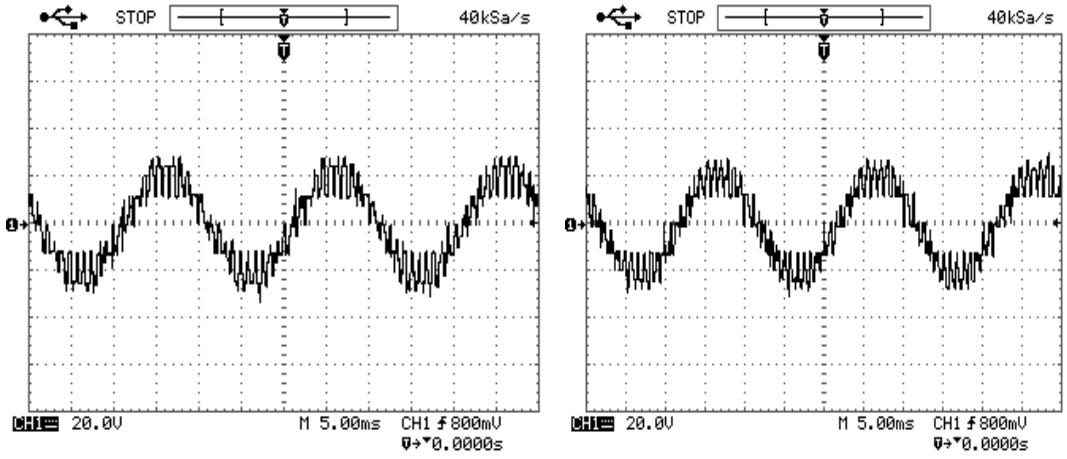
(a) v_{RY} **(b)** v_{YB}

Fig. 8.23 Three phase HMLI output voltage with POD modulation technique



(a) v_{RB} **(b)** v_R

Fig. 8.24 Three phase HMLI output with POD modulation technique



(a) v_Y **(b)** v_B

Fig. 8.25 Three phase HMLI output with POD modulation technique

Fig. 8.26 is THD obtained from .csv file imported to MATLAB for one output and other values are mentioned in Table 8.1.

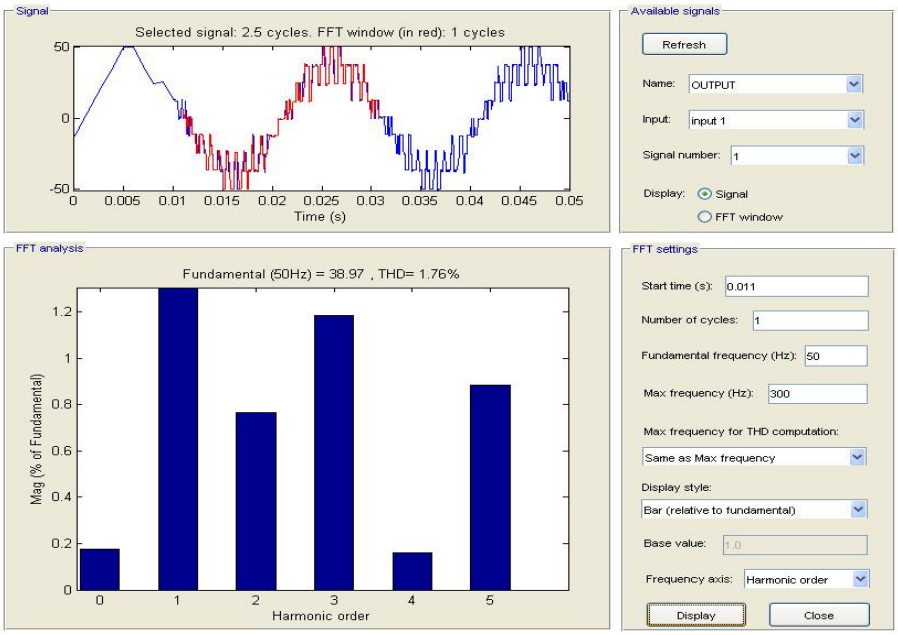
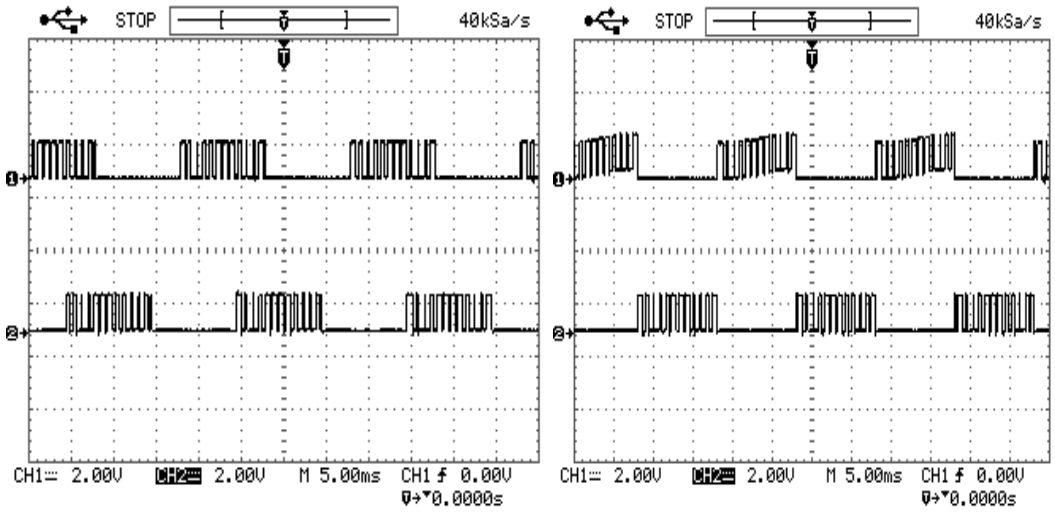


Fig. 8.26 FFT analysis and THD for 3 phase HMLI with POD modulation technique

8.2.3 HARDWARE OUTPUT FOR THREE PHASE HMLI WITH APOD MODULATION TECHNIQUE

i) BATTERIES AS SUPPLY

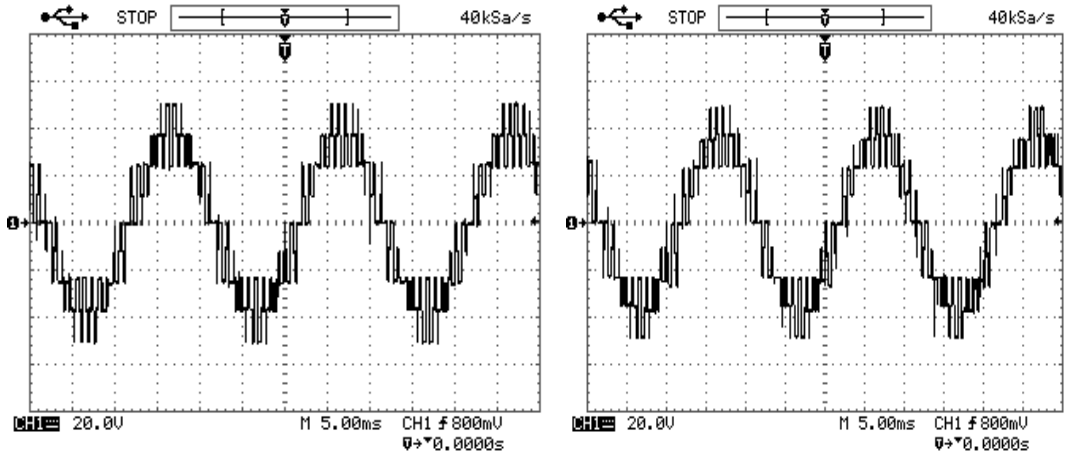
Fig 8.27(a) shows control signals with APOD modulation technique for switches which are 120^0 apart.



(a) G_1 G_1' **(b) G_1 G_3**

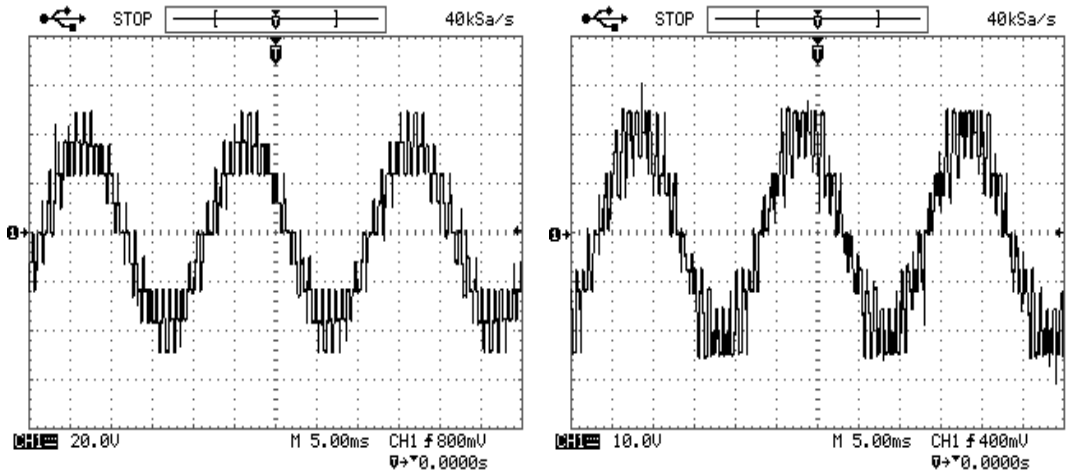
Fig. 8.27 Control signals for three phase HMLI with APOD modulation technique

Fig 8.28(a) shows 9 level line to line output voltage(v_{RY}).100 Ω- 1 W resistors are star connected as load. Fig 8.28(b) output voltage v_{YB}. Fig 8.29(a) output voltage v_{RB}



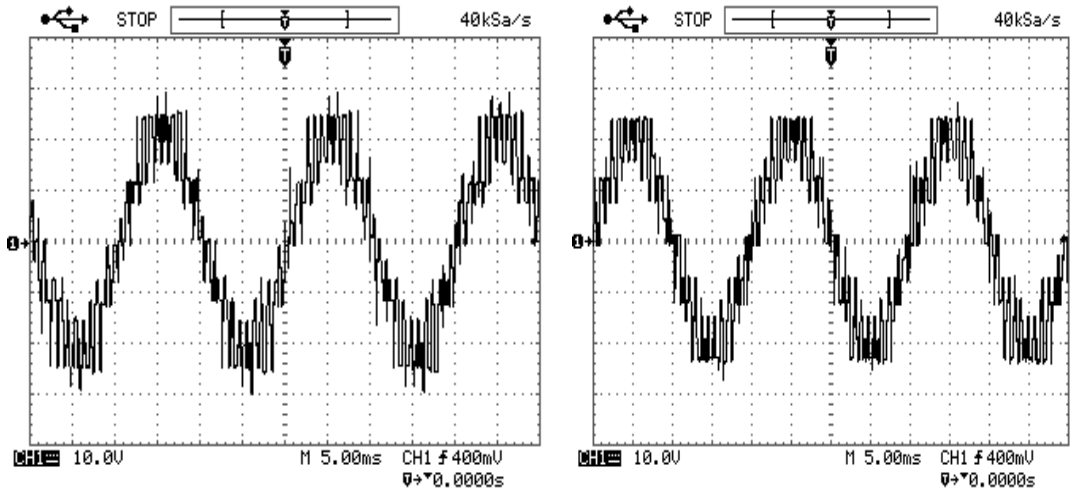
(a) v_{RY} **(b)** v_{RB}

Fig. 8.28 Three phase HMLI output with APOD modulation technique



(a) v_{YB} **(b)** v_{R}

Fig. 8.29 Three phase HMLI output with APOD modulation technique



(a) v_{Y} **(b)** v_{B}

Fig. 8.30 Three phase HMLI output with APOD modulation technique

. Fig 8.29(b) shows 7 level v_R phase output voltage while Fig 8.30 (a) and (b) show 7 level output voltages v_Y and v_B respectively. Control signals were given at sample rate of 25 kHz due to limitation of MATLAB SIMULINK. Fig. 8.31 is THD obtained from .csv file imported to MATLAB for one output and other values are mentioned in Table 8.1.

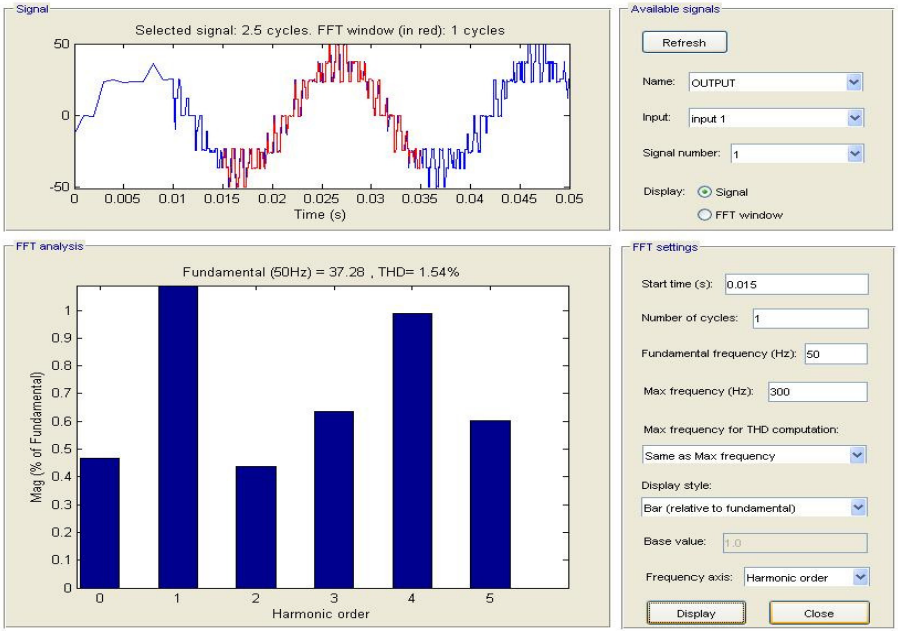
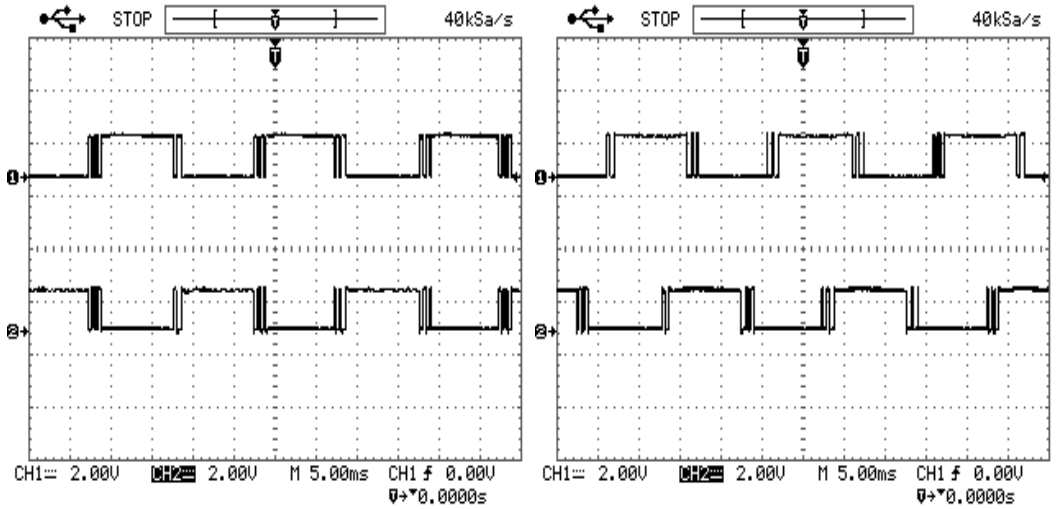


Fig. 8.31 FFT analysis and THD for 3 phase HMLI with APOD modulation technique

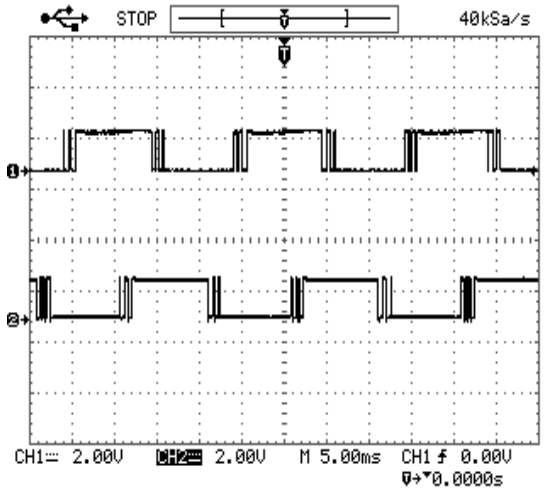
8.2.4 HARDWARE OUTPUT FOR THREE PHASE HMLI WITH THIRD HARMONIC MODULATION TECHNIQUE (PD)

i) BATTERIES AS SUPPLY

Fig 8.32(b) shows control signals with third harmonic injection modulation technique for switches which are 120^0 apart. Fig 8.33(a) shows 9 level line to line output voltage(v_{RY}). 100 Ω- 1 W resistors are star connected as load. Fig 8.33(b) shows output voltage v_{YB}. Fig 8.34(a) is output voltage v_{RB}. Fig 8.34(b) shows 7 level v_R phase output voltage while Fig 8.35(a) and (b) show 7 level output voltage v_Y and v_B respectively. Control signals were given at sample rate of 25 kHz due to limitation of MATLAB SIMULINK. Fig. 8.36 is THD obtained from .csv file imported to MATLAB for one output and other values are mentioned in Table 8.1.

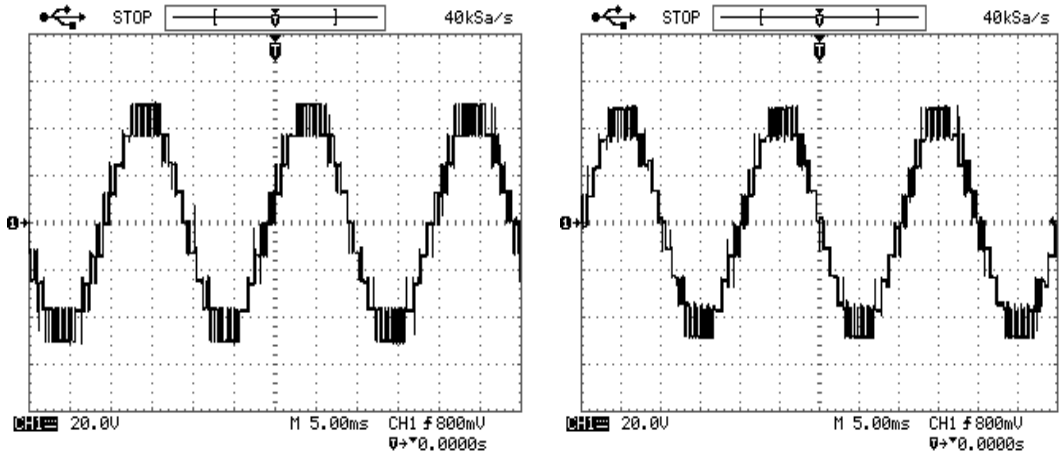


(a) G_5 G_6 **(b) G_6 G_6'**



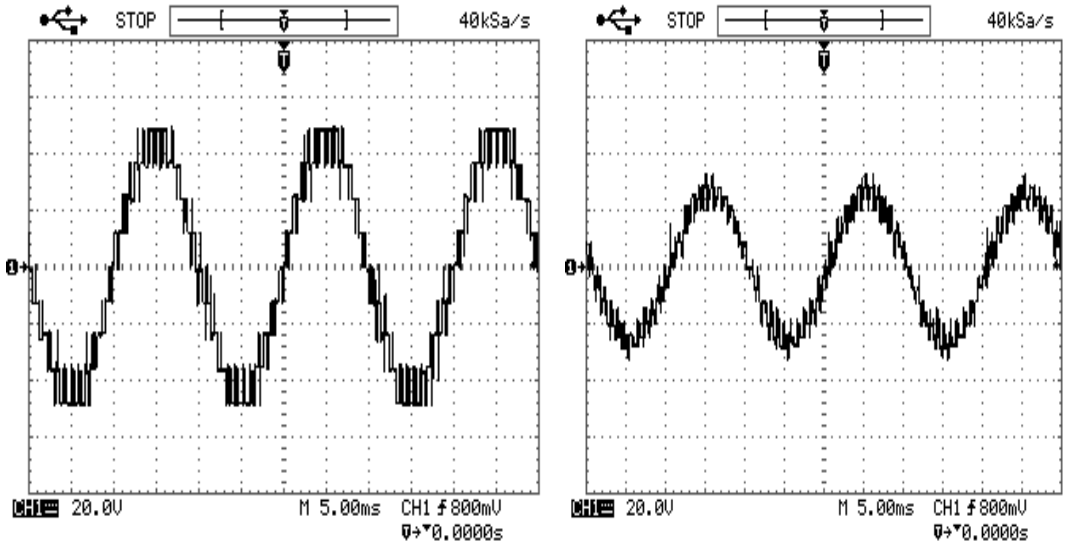
(c) G_5 G_5'

Fig. 8.32 Control signals for three phase HMLI with third harmonic injection modulation technique



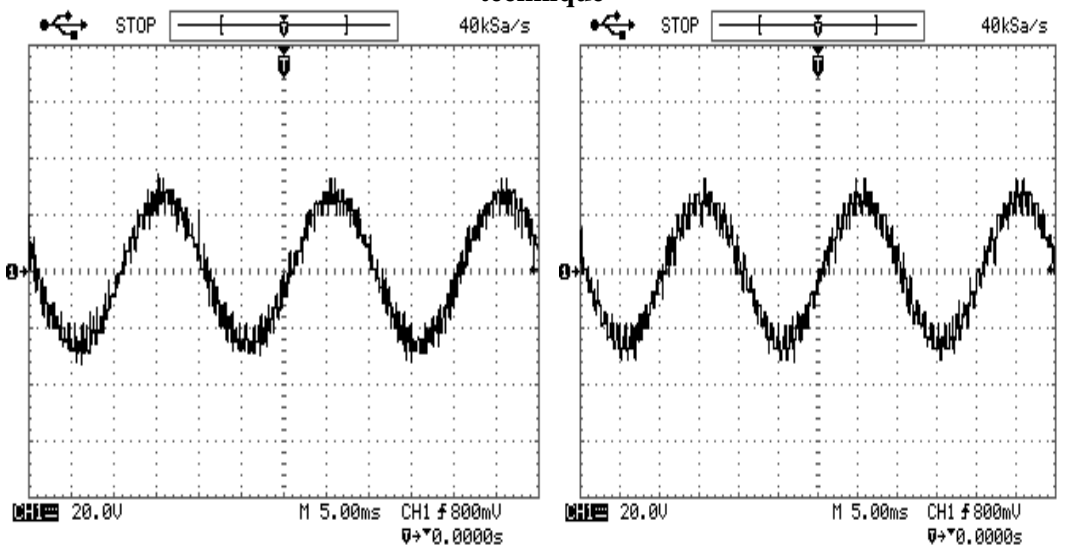
(a) v_{RY} **(b) v_{YB}**

Fig. 8.33 Three phase HMLI output with third harmonic injection modulation technique



(a) v_{RB} **(b) v_R**

Fig. 8.34 Three phase HMLI output with third harmonic injection modulation technique



(a) v_Y **(b) v_B**

Fig. 8.35 Three phase HMLI output with third harmonic injection modulation technique

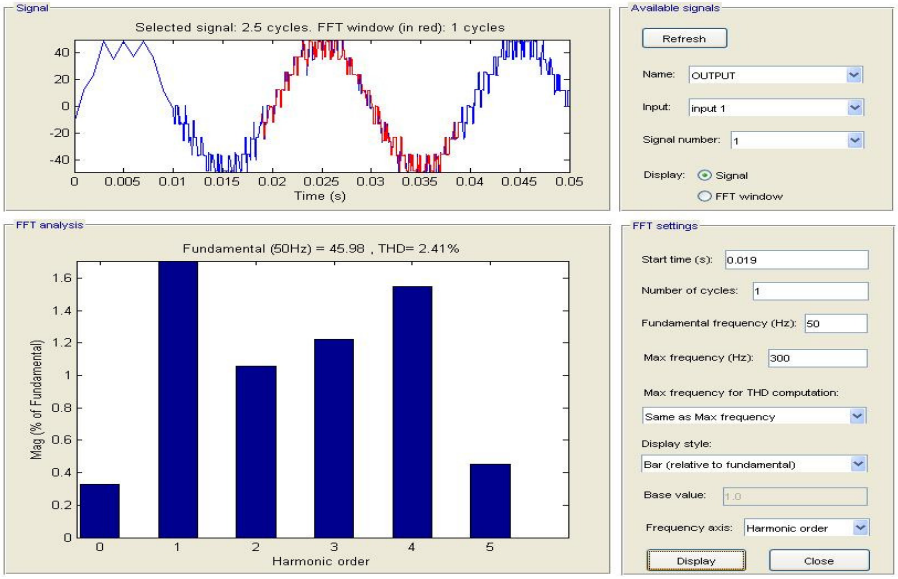
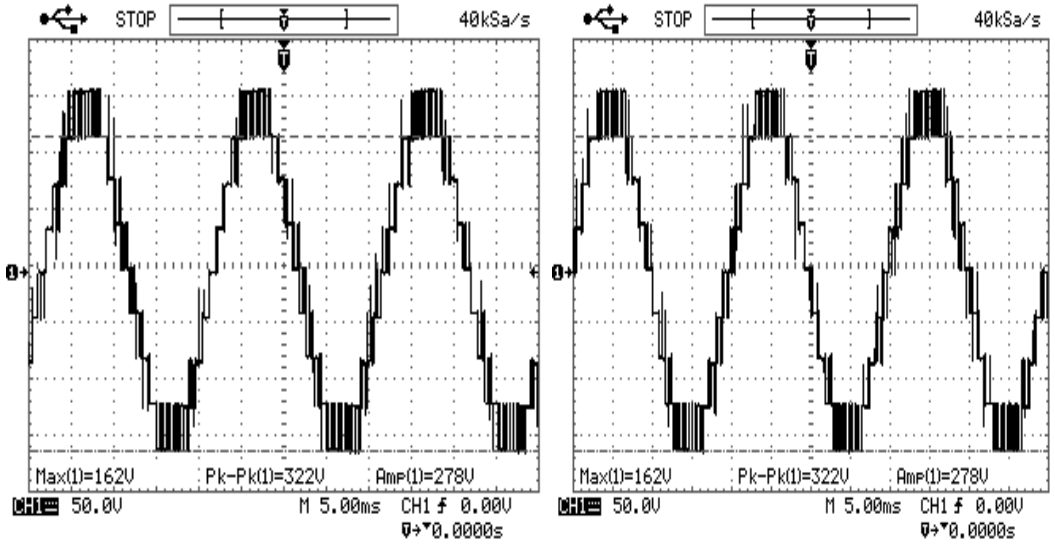


Fig. 8.36 FFT analysis and THD for 3 phase HMLI with third harmonic injection modulation technique Y-B

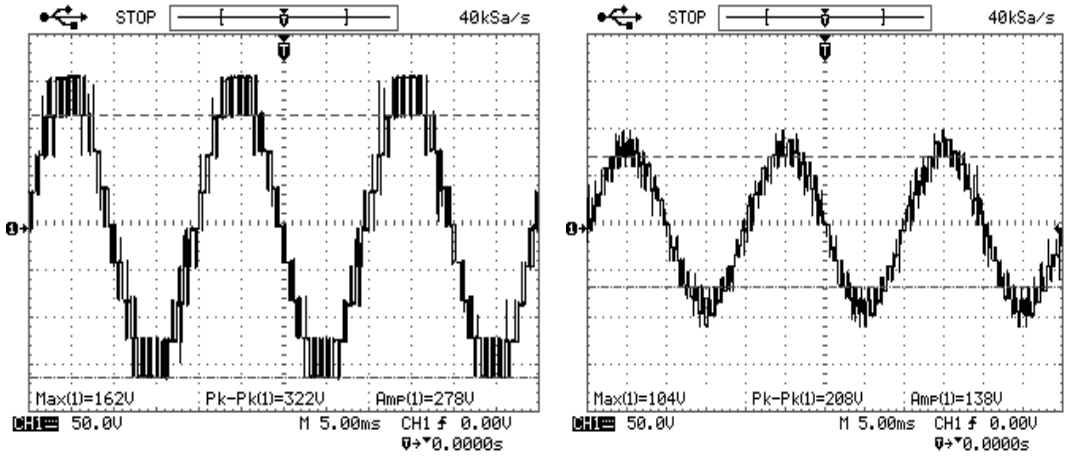
ii) REGULATED POWER SUPPLY

Fig 8.37(a) shows 9 level line to line output voltage(v_{RY}). 1 kΩ- 10 W resistors are star connected as load. Fig 8.37(b) output voltage v_{YB}. Fig 8.38(a) output voltage v_{RB}. Fig 8.38(b) shows 7 level v_R output voltage while Fig 8.39(a) and (b) show 7 level output voltage v_Y and v_B respectively. Control signals were given at sample rate of 25 kHz due to limitation of MATLAB SIMULINK. Fig. 8.40 is THD obtained from .csv file imported to MATLAB for one output and other values are mentioned in Table 8.1.



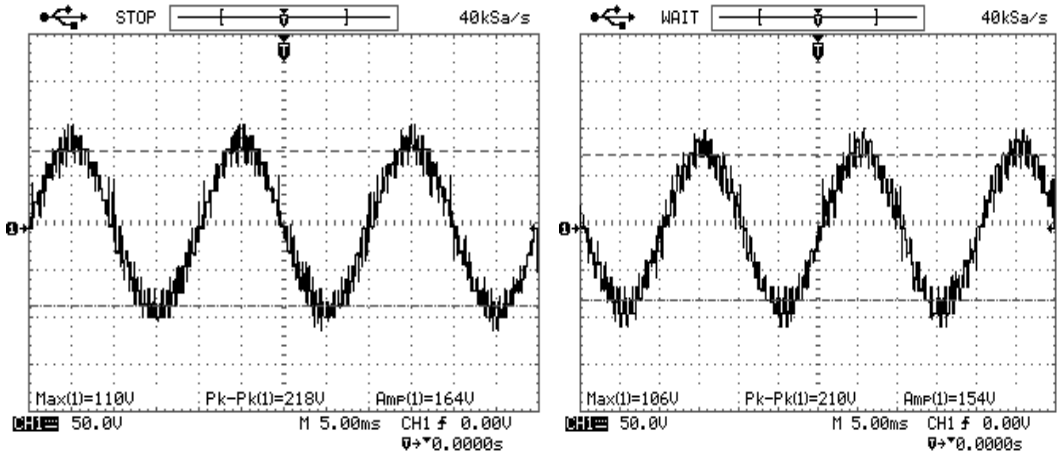
(a) v_{RY} **(b) v_{RB}**

Fig. 8.37 Three phase HMLI output with third harmonic injection modulation technique



(a) v_{YB} **(b) v_R**

Fig. 8.38 Three phase HMLI output with third harmonic injection modulation technique



(a) v_Y **(b) v_B**

Fig. 8.39 Three phase HMLI output with third harmonic injection modulation technique

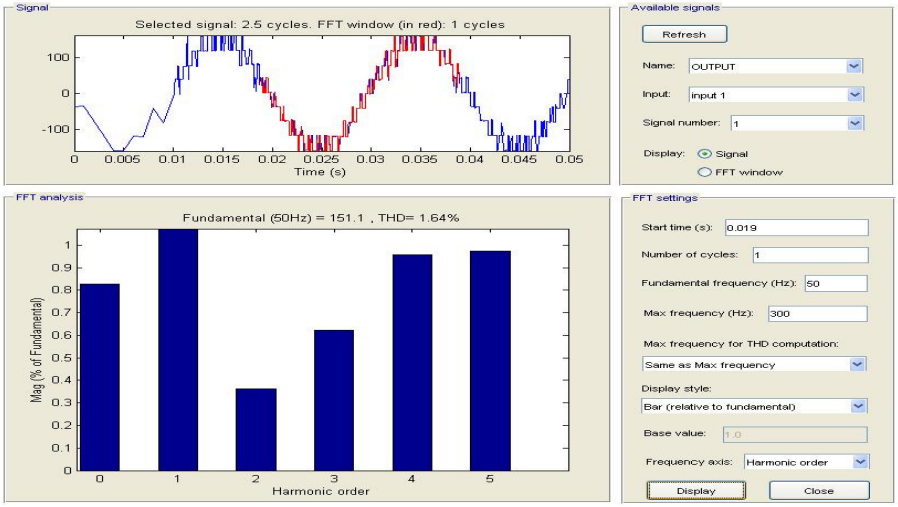


Fig. 8.40 FFT analysis and THD for 3 phase HMLI with third harmonic injection modulation technique

Table 8.1 Summary of output

Modulation Technique	Line to line voltage	DC input in Volts	Start Time	Simulation Results			Hardware Results			
				V_o	V_1	THD	V_o	load Ω	V_1	THD
PD	v_{RY}	24-12	.01/.011	96	41.64	0.59	90	100	37.88	1.26
	v_{YB}		.01	96	41.5	0.74	90	100	37.09	1.95
	v_{BR}		.01/.027	96	41.64	0.53	90	100	37	2.48
	v_{RY}	80-40					316	330	119.8	1.73
	v_{YB}						320	330	119.5	1.8
	v_{RY}	80-40	.02/.019	320	138.5	0.49	292	33	112	1.27
	v_{BR}		.02/.029	320	138.5	0.45	296	33	113.1	1.38
	v_{YB}		.02/.029	320	138.5	0.53	296	33	111.6	1.35
POD	v_{RY}	24-12	.01/.011	96	41.52	0.49	96	100	38.97	1.76
	v_{YB}		.012	96	41.56	0.58		100		
	v_{BR}		.017	96	41.57	0.65	96	100	38.28	1.58
APOD	v_{RY}	24-12	.015		41.57	0.19	96	100	37.28	1.54
	v_{YB}		.015/.01		41.58	0.37/.87	96	100	36.76	1.82
	v_{BR}		.01/.02		41.53	.18/.63	96	100	36.82	1.72
Third Harmonic Injection	v_{RY}	24-12	.01	96	45.86	2.14	96	100	46.57	2.44
	v_{YB}		.019	96	45.43	1.96	96	100	45.98	2.41
	v_{BR}		.015	96	45.82	2.37	96	100	46.13	2.52
	v_{RY}	80-40	.019/.02	320	152.6	1.51	322	1k	148.6	1.65
	v_{YB}		.019/.017	320	153	1.77	322	1k	150.4	2.06
	v_{BR}		.019/.019	320	152.6	1.51	322	1k	151.1	1.64
PD	v_O	12-12-12	.01	48	24	0.79	40	100	18.41	4.61

Number of cycles for THD----1

Output levels for 3 phase----9

V_1----Fundamental voltage

V_o----Peak to peak output voltage in volts

THD noted at maximum frequency as 300Hz.

vo----Single phase output

8.3 SUMMARY

In this chapter hardware results are given. Hardware was tested at low voltage battery and high voltage regulated power supply. Results were compared for low and high voltage for different modulation techniques. It is observed that there is no much difference in THD as voltage is increased from low to high.

It is observed that with PD modulation technique THD obtained from simulation much more less with respect to THD obtained from hardware results for low as well as high DC voltage applied. POD and APOD modulation techniques are implemented for low DC voltage. Variation in THD is more for APOD modulation technique when simulated and applied for hardware as compared to POD modulation technique results.

It was expected that THD would be less for third harmonic injection modulation technique as compared to other modulation techniques, but practically THD is more.

CHAPTER 9

CONCLUDING REMARKS and FUTURE SCOPE

The hybrid multilevel inverter is presented in this work. The project work presents the design, simulation, analysis and implementation of hybrid multilevel inverter. Many projects are implemented with this theory and circuit but in this research work, DSP 28335 with MATLAB/SIMULINK, CCS 3.3 and emulator C2000 series is used to obtain control signals along with DC regulated power supply. The DSP based control unit reduces the system hardware and makes it more flexible in comparison with conventional digital control.

Hybrid multilevel inverter has many merits such as: ability to synthesize waveforms with better harmonic spectrum, an output voltage level that is higher than those of the power semiconductor switching devices', reduced THD, dv/dt stress and common mode voltage and different approaches to achieve the goal of multilevel output.

9.1 GOALS REACHED

- The work presents the use of different modulation techniques simulation, analysis and implementation of the control of hybrid multilevel inverter.
- Regulated power supply for DC 40V/80V is developed with 5A current rating. Load regulation is 7.09%.
- Simulations are done for single phase cascaded multilevel inverters(five level, seven level and nine level) and THD is compared.
- Simulations are also done for different hybrid multilevel inverters like asymmetric hybrid multilevel inverter, symmetrical hybrid multilevel inverter and half bridge module based hybrid multilevel inverter with single phase and three phase configurations. Simulations are done with and without modulation. As obvious THD is high for simulated circuits without modulation. For simulated circuits with modulation THD is varying from 0.6% to 1.8% for different topologies with different modulation techniques for single phase and three phase as done in MATLAB R2009a.
- Similarly, simulations are done for selected hybrid multilevel inverter with different modulation techniques for single phase and three phase and comparison is done on basis of THD. For single phase THD varies from 1.15% to 1.52% and for three phase THD varies from 0.84% to 1.41% as done in MATLAB R2009a.
- In hardware for single phase hybrid multilevel inverter 5 levels are obtained using 12V/24V batteries.

- The circuit is further developed for three phase hybrid multilevel inverter. In the project multicarrier modulation techniques including PD, POD, APOD and THIPDPWM is used for implementation purpose with constant modulation index which can be changed to achieve different results.
- THD obtained as low as 1.2% from hardware and 0.19% from simulations in MATLAB R2013a as shown in chapter 8. Trying recent tools it may be possible to modify the system to reduce THD.
- This system can work for 1.5KW power output.

9.2 INNOVATIONS

- The power module and digital controller interface is developed as separate units with provisions for change of configuration or up gradation in power module as well as hardware interface to make it suitable for load up to 1.5 KW.
- The control signals are developed using combination of MATLAB/SIMULINK, code composer studio and emulator which eliminates writing a code for the software. The technique can be used by the user who is not proficient in programming.

9.3 FUTURE PLANS FOR EXTENSION

- Software can be generated for closed loop system.
- Circuit of HMLI with capacitors as voltage source can be used as other HMLI topology. For portable HMLI regulated power supply can be replaced with batteries and rechargeable voltage source, which may be taken as future project.
- The power module can be modified to realize other hybrid multilevel inverters such as symmetrical or asymmetrical hybrid multilevel inverter or half bridge multilevel inverter for single phase or three phase and modulation techniques developed in this project can be used with minor modifications.
- It is possible to realize different power electronics system applications such as drives, EV.
- As already stated it is possible to modify the power and control circuit so that HMLI can be used for load more than 3 KW otherwise same power and control circuit can be used.
- With some small modification other topologies can be developed for HMLI.
- It is possible to implement this system with digital signal controller and make the system more cost effective.

- Other modulation techniques can be applied to this system to reduce THD.

9.4 INDUSTRY, INVOLVEMENT AND INTERACTION

- The wiring for the power module, signal conditioning circuits and assembly work was done with the help of technical assistant at the Control System Engg., GIDC, Makarpura, Vadodara manufacturers of drives.
- The software development tools for DSP were supplied by Edutech Systems, Dandia Bazar, Vadodara. The software engineers of the company helped in software development and interfacing EPB29335 with power circuit module.

CHAPTER 10

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APPENDIX A

DESIGN and PRACTICAL READINGS for REGULATED POWER SUPPLY

A.1 DESIGN FOR REGULATED POWER SUPPLY

As explained in chapter 7 regulated power supply is controlled transistor series regulator and equations used to determine values of resistors are standard transistor equations.

As T_1 is series pass element its V_{CEO} should be high and as per datasheet of 2N3773 V_{CEO} is 140V hence this power transistor is selected. For T_2 current gain and V_{CEO} should be high and as per datasheet of 2N3501 h_{FE} is 300(maximum) and V_{CEO} is 150V hence this transistor is selected. BD139 is used for negative feedback from output.[Ref. Fig. 7.3]

The voltage provided by potential divider R_1' and R_2' is equal to sum of base-emmiter voltage of transistor T_3 and zener diode.

$$V_{BE3} + V_Z = V_2' = \frac{R_2'}{R_2' + R_1'} V_{out}$$

Output voltage required is 40V or 80V, zener is taken as 6.2V for emitter voltage of T_3. Assume value for one of the resistors and find other. Negative feedback gain can be adjusted by inserting potentiometer in circuit. Current through zener is limited by resistance R_1.

$$I_Z = \frac{V_1 - V_Z}{R_1}$$

where V_1 is unregulated DC obtained from bridge rectifier.

I_Z is I_{E3} which is maximum 1A from datasheet ($I_C = I_E + I_B$) thus I_Z taken as less then 500mA. Hence from equation R_1 is found.

A.2 PRACTICAL RESULTS FOR REGULATED POWER SUPPLY

Practical readings obtained for voltage regulator are given in Table A.1 and A.2. Transformer used is 230/40V and 210/40V for testing. Load resistor is varied such that output current is from 0 to maximum i.e 5A. Load regulation is calculated by given equation:

% Load Regulation = $(V_{NL} - V_{FL})/V_{NL} * 100$

where V_{NL} is output voltage at no load

V_{FL} is output voltage at full load

Table A.1 Load regulation for 230V input

Unregulated output (V)	Regulated output voltage(V)	Load current(A)
54.7	42.3	0
50.7	39.9	1.5
49.7	39.8	2
49	39.7	2.5
47.8	39.6	3
46.5	39.5	4
45.5	39.4	4.5
44.5	39.3	5

% Load Regulation = (42.3-39.3)/42.3 *100

= 7.09%

Table A.2 Load regulation for 210V input

Unregulated output (V)	Regulated output voltage(V)	Output current(A)
55.5	40.8	0
51.5	40.4	1.5
50.4	40.3	2
49.3	40.2	2.5
47.9	40.2	3
46.3	39.9	4
45.3	39.6	4.5
44.9	38.1	5

% Load Regulation = (40.8-38.1)/40.8 *100

= 6.61%

APPENDIX B

PHOTO GALLERY

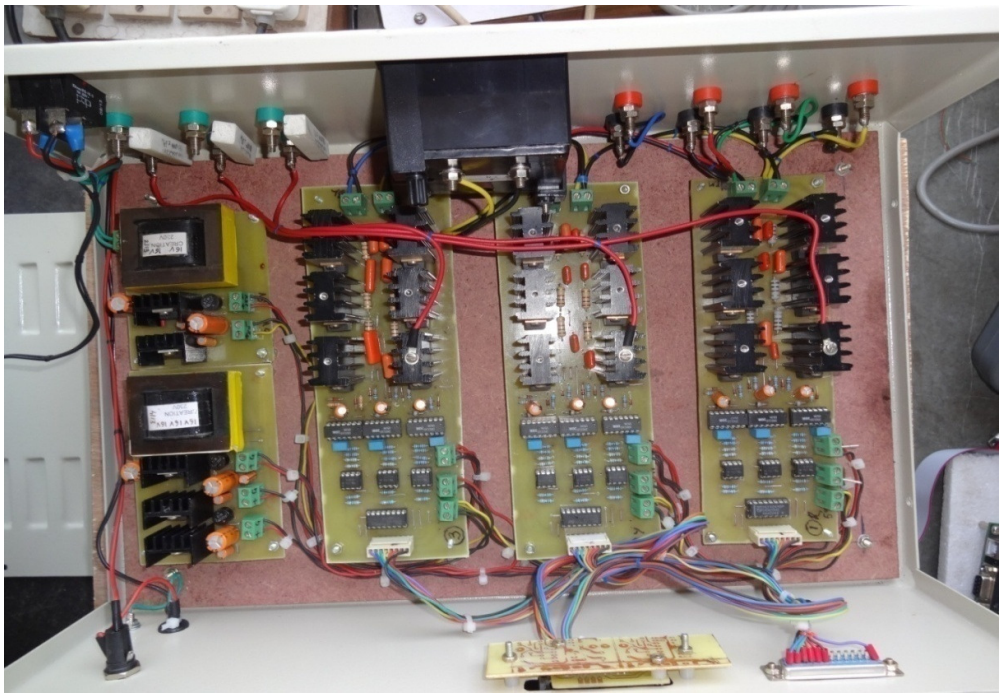

Fig. B.1 Hardware for control and power circuit

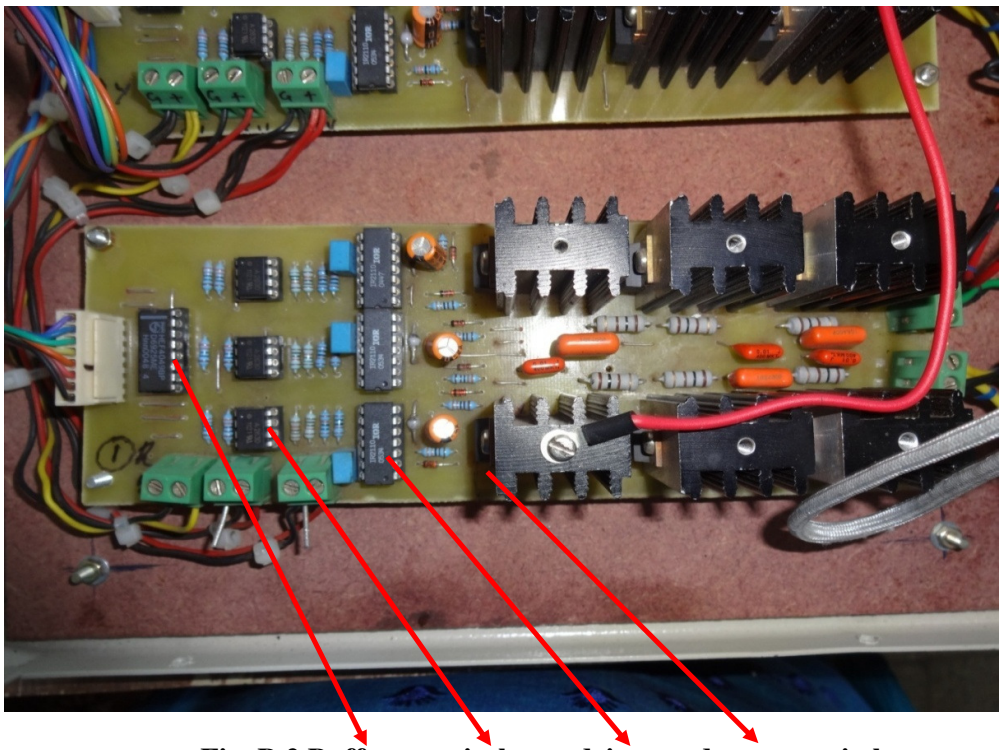

Fig. B.2 Buffer, optoisolator, driver and power switch

Fig. B.3 Panel for control and power circuit

Fig. B.4 Gating signals

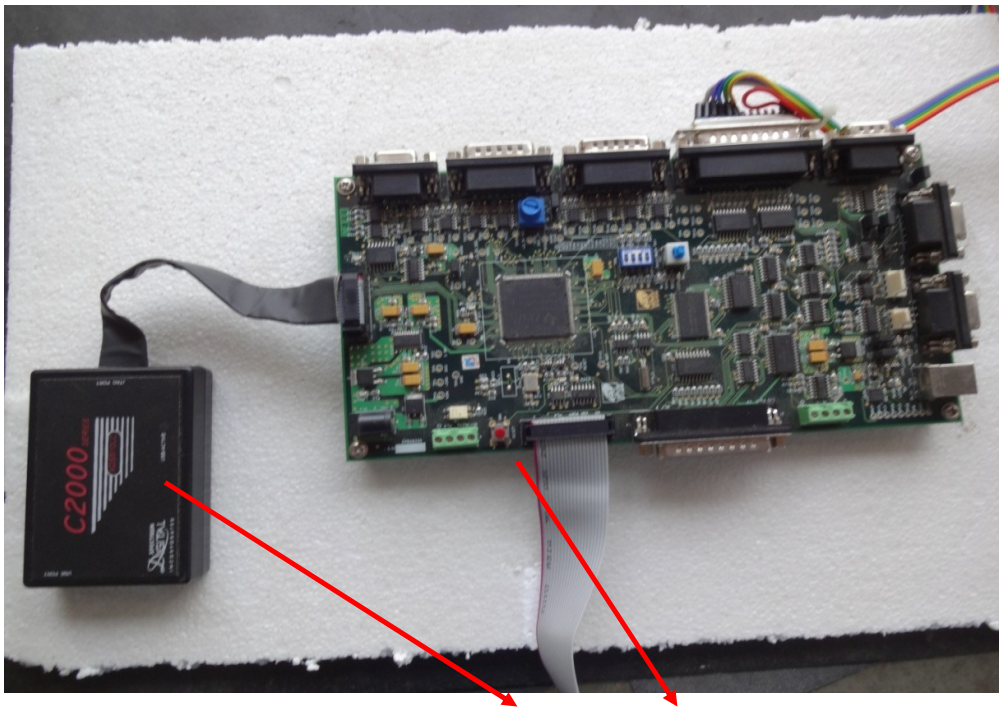

Fig. B.5 Emulator and EPB28335

Fig. B.6 Hardware for regulated power supply

Fig. B.7 Panel for regulated power supply

Fig. B.8 Primary voltage selector

Fig. B.9 Setup for current measurement

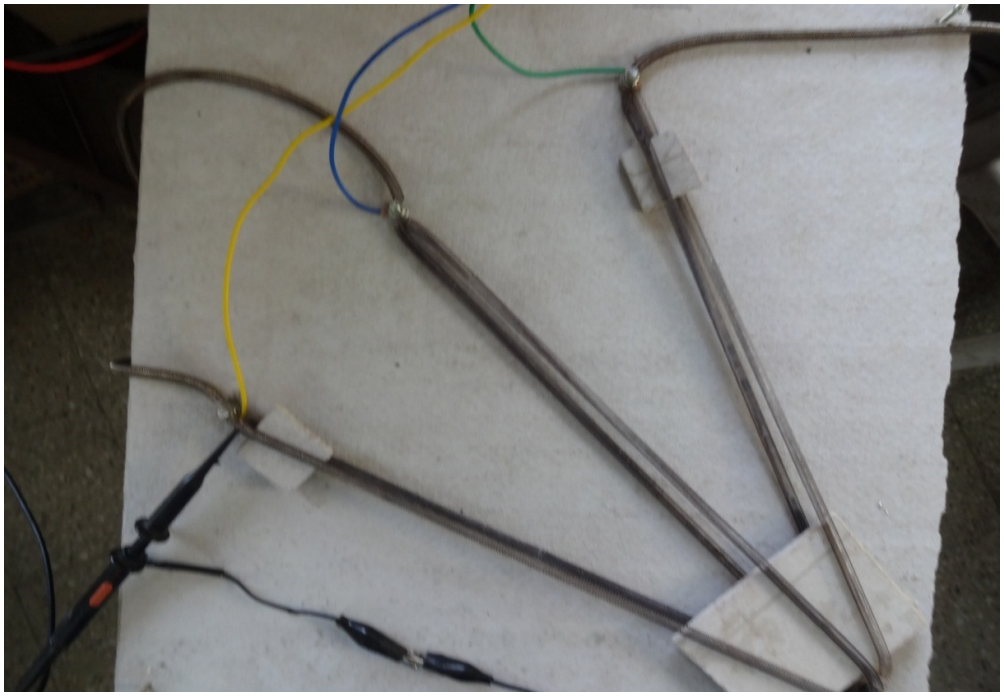

Fig. B.10 Load

Fig. B.11 System setup

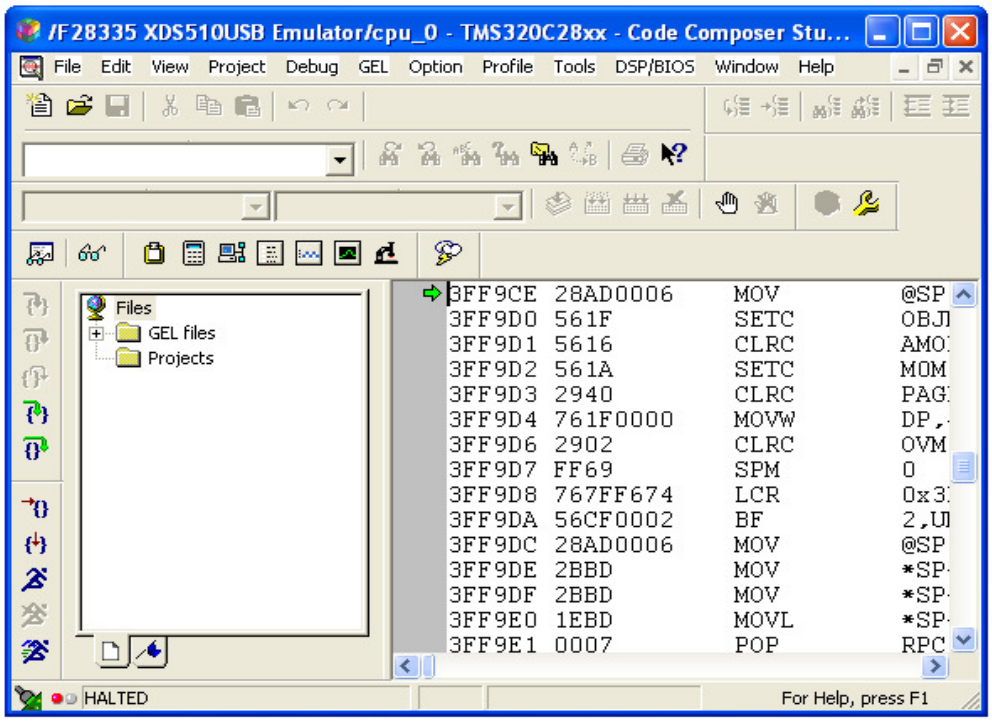

Fig. B.12 Emulator connected

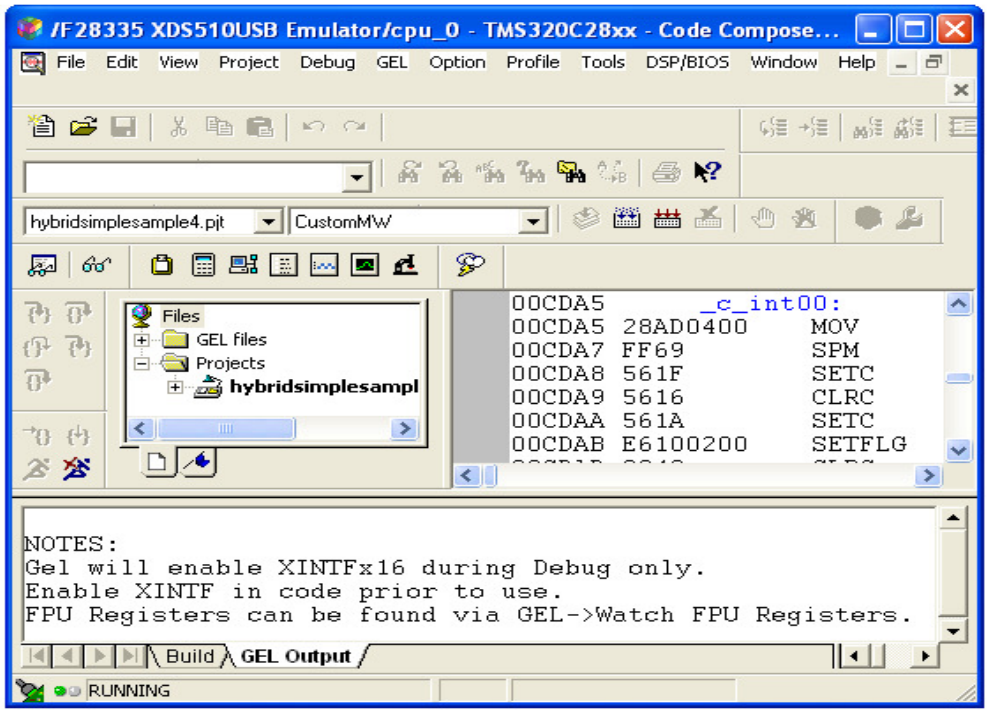

Fig. B.13 Project built

APPENDIX C

WORKSHOPS ATTENDED and PAPERS PRESENTED/PUBLISHED

Workshops attended

- ISTE approved Short Term Training Programme on " Recent Trends in Electrical Drives "27th December 2010 to 1st January 2011 conducted by Department of Electrical Engineering, Institute of Technology, Nirma University, Ahmedabad.
- Workshop on "Embedded systems and VLSI Design", April 11-15, 2011, conducted by Electrical Engineering Department, Faculty of Technology & Engineering The Maharaja Sayajirao University of Baroda
- Workshop on "Spoken Tutorial for Latex and Scilab" on 25th and 26th June 2012 at ITM Universe, Vadodara in association with Spoken Tutorial Project, IIT Bombay.
- Workshop on "Smart Controllers 2012 Embedded Controllers for Solid State Drives & Power Converters", August 21-25, 2012, conducted by Electrical Engineering Department, Faculty of Technology & Engineering The Maharaja Sayajirao University of Baroda

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