Chapter 8

Hardware Implementation of Throughput Optimization Algorithms

Hardware Implementation of Throughput Optimization Algorithms

8.1 Embedded Architecture Implementation

The algorithm developed for Throughput Optimization of LTE-A Downlink Physical Layer are implemented on Spectrum Digital TMS320C6713 DSK and Xilinx Atlys Spartan 6 Development Kit. The embedded architecture implementation of these algorithms are carried out in close-loop testing with MATLAB based LTE-A Link Level Simulator. Figure 8.1 shows the design flow for real-time implementation of proposed algorithms for Throughput Optimization. The Mathworks Model based design FPGA and DSP implementation and verification is discussed in Section 3.3.

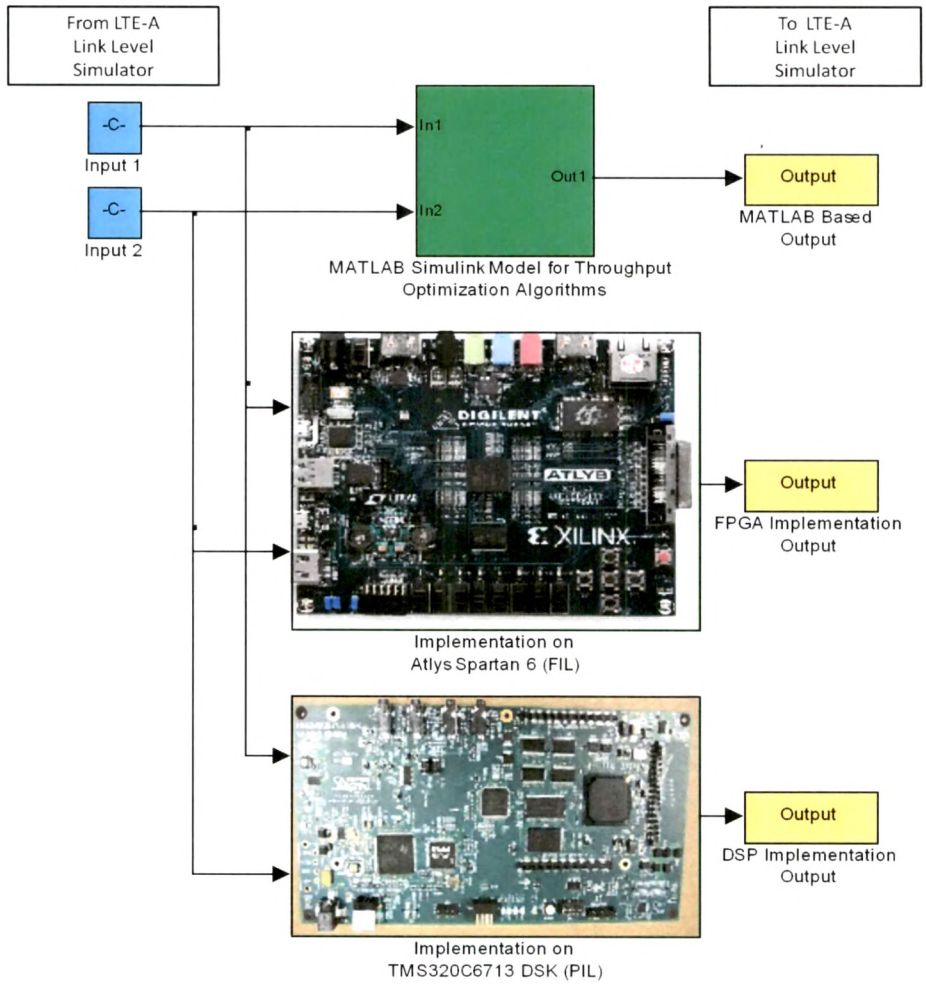

Figure 8.1: Design Flow for Real-time Implementation on Target Hardware

Throughput Optimization of LTE-A Downlink Physical layer is addressed in the research work. Following are the proposed techniques for throughput optimization:

- ANN based MIMO channel estimation techniques are developed which maximizes Throughput of LTE-A Downlink Physical Layer as discussed in Chapter 6.
- Fuzzy Logic Decision model is developed for MIMO mode switching to achieve maximum throughput of LTE-A Downlink Physical Layer discussed in Chapter 7.

8.1.1 XUP Atlys Spartan-6 Development Kit

The Xilinx University Program (XUP) Atlys Development Kit [1,2] is based on high-capacity Spartan-6 LX45 FPGA [3,4], and includes the circuits and devices that enable advanced digital system designs. The on-board high-speed DDR2 memory, HDMI ports, Gigabit Ethernet, and advanced clocking and power supply circuits makes the kit an ideal platform for research work as shown in Figure 8.2. The Atlys Functional Block Diagram with all the peripherals and connectivity are shown in Figure 8.3. The Atlys board includes Adept USB2 system, which offers device programming, real time power supply monitoring, automated board tests, virtual I/O, and simplified user data transfer facilities.

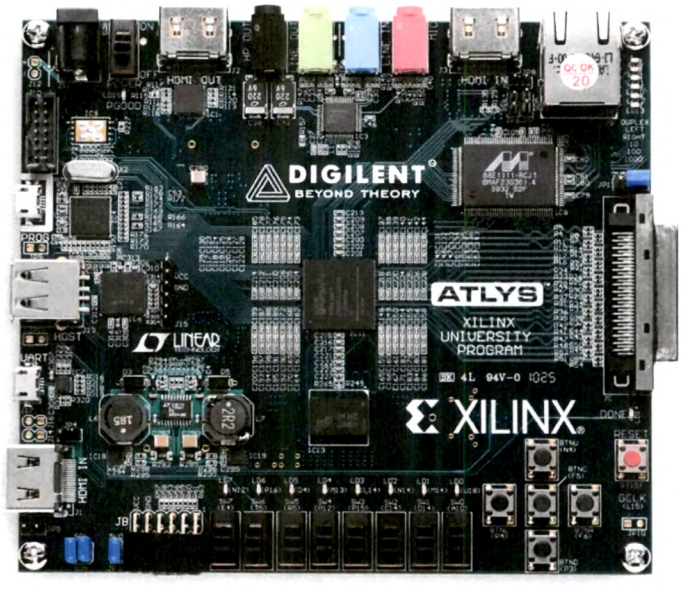

Figure 8.2: XUP Atlys Spartan-6 Development Kit

XUP Atlys Board is one of the supported FPGA devices for FPGA-in-the-loop simulation in MATLAB. FIL Simulation provides the capability to use Simulink models for testing designs in real hardware for any existing HDL code. The FIL process provides synthesis, logical mapping, Place-and-route (PAR), programming file generation and communication channel.

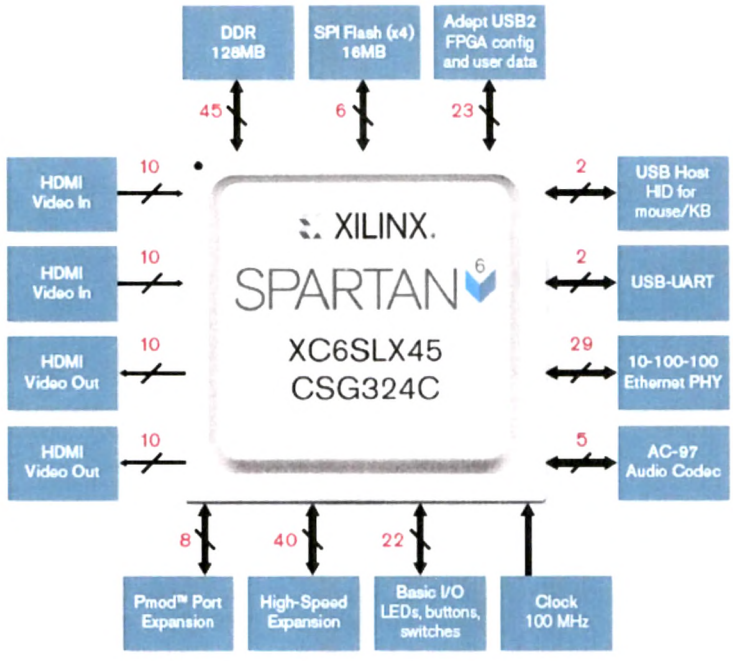

Figure 8.3: Functional Block Diagram of Atlys board

8.1.2 TMS320C6713 DSP Starter Kit

The TMS320C6713 DSP Starter Kit (DSK) [5] is a standalone development platform that enables users to evaluate and develop applications for the TI's TMS320C6713 DSP operating at 225MHz [6] as shown in Figure 8.4. The DSP on the starter kit interfaces to on board peripherals through a 32bit wide External Memory Interface (EMIF) as shown in Figure 8.5. The SDRAM, flash and CPLD are all connected to the bus. EMIF signals are connected to daughter card expansion connectors which are used for third party add in boards. The kit is designed to work with TI's CCS IDE. Code composer communicates with the starter kit through an embedded JTAG emulator with a USB host interface.

MATLAB's Embedded coder toolbox provides Processor-in-the-loop simulation for developed algorithm simulation, testing and validation. DSK C6713 is one of the many Target device which supports PIL Simulation for close loop simulation. The C code generated from the Simulink model

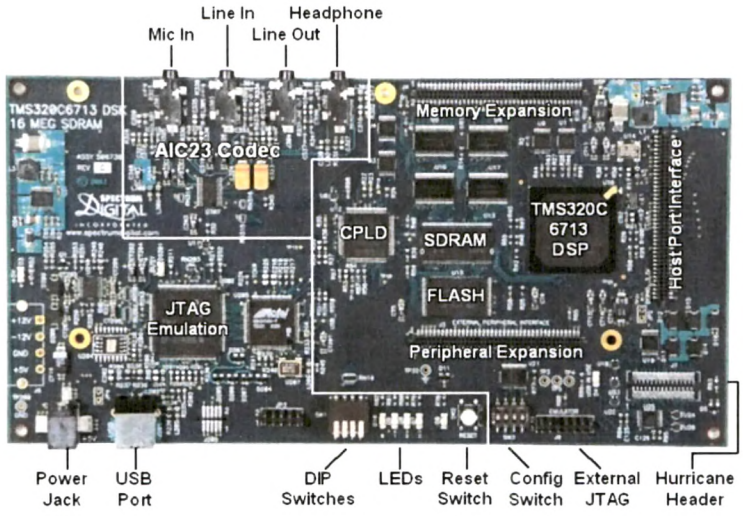

Figure 8.4: TMS320C6713 DSP Starter Kit

runs on actual target and in close loop simulation with MATLAB.

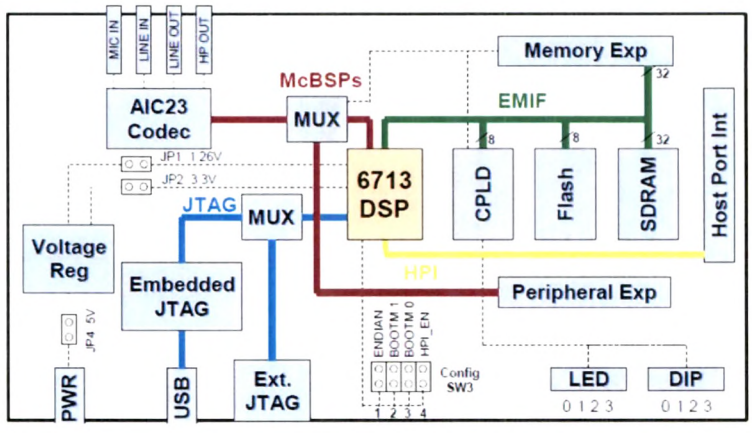

Figure 8.5: Functional Block Diagram of DSK 6713

8.1.3 Implementation of FL Decision model for MIMO mode switching

FL Decision model is designed using Fuzzy Logic Toolbox for MIMO mode switching in LTE-A Downlink Physical Layer. The FL Decision Model consists of two inputs Average Condition Number and Receive SNR and one output is MIMO mode selected. The FL Decision model is converted to Fixed-point model to validate its performance on FPGA and DSP. GUI is designed to ease the throughput analysis of Physical Layer and to perform the real-time implementation on Target Hardware.

8.1.3.1 Implementation on Atlys Spartan 6 Development kit

The FL Decision model is developed for MIMO mode switching to maximize throughput of LTE-A Downlink Physical Layer. The design and simulation results of the Fuzzy Decision model is presented in Chapter 7. The Decision model is verified with the real-time implementation and real-time testing on Atlys Spartan 6 Development kit. Figure 8.6. shows the MATLAB Simulink models for verification on target device.

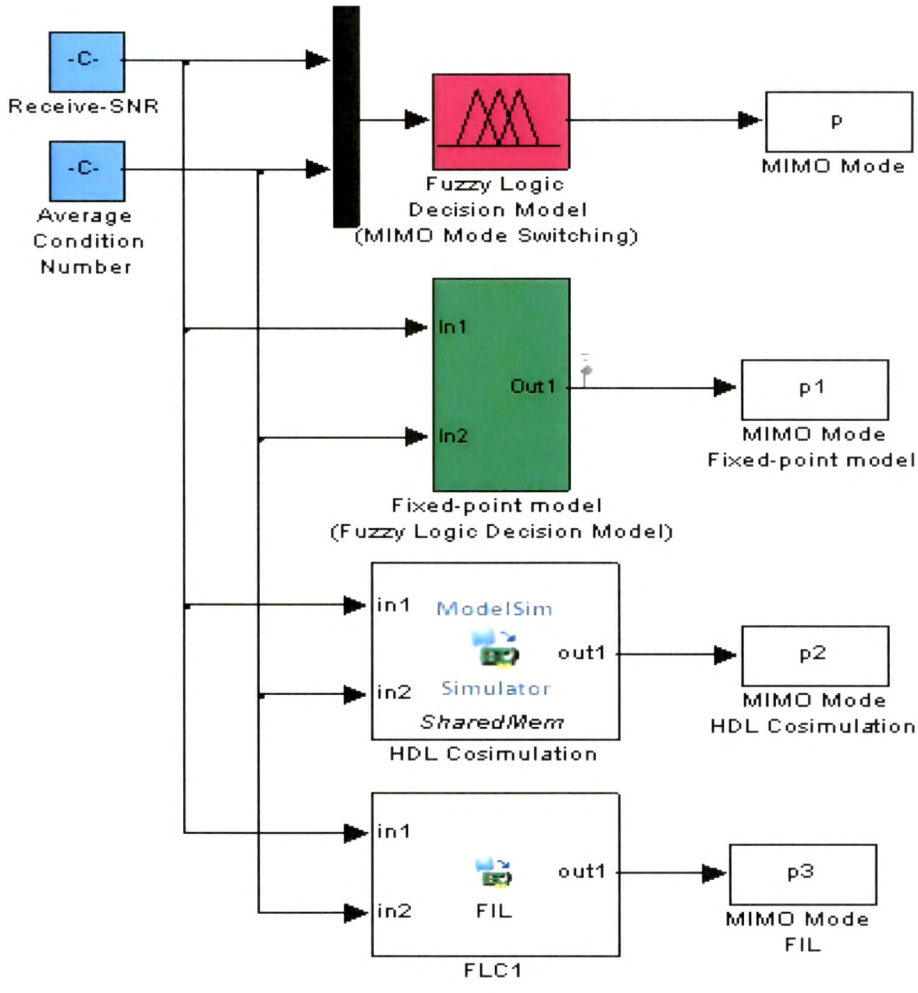

Figure 8.6: Simulink Models for FL Decision model for HDL Co-simulation and FIL Simulation

The steps for Hardware Implementation of Fuzzy Decision model in Atlys Spartan 6 Development kit is as below:

1). The simulation model FLC is designed using Fuzzy Logic Toolbox and is verified in close-

loop with LTE-A Link Level Simulator. The input membership functions of Channel Condition Number and Receive SNR and Fuzzy Rule base is as given in Section 7.4.

2). The SIMULINK model is converted to Fixed-point model (to implement on FPGA), using Fixed-Point Toolbox.

3). HDL code is developed for the designed Fixed-Point model of Fuzzy Decision model using HDL Workflow Advisor. Using HDL Workflow Advisor we can set the Target Device, prepare the model for HDL Code Generation and HDL code is generated for the Target device specified. FPGA Synthesis and Analysis in Xilinx ISE Design Suite is carried out and the programming file generated is downloaded to the Target.

4). Once the HDL Code is generated, the code is verified with ModelSimXE III 6.2c Simulator using EDA Simulator Link. Figure 8.7 shows the result of ModelSim Simulator, which is same as we got using Fixed-Point model.

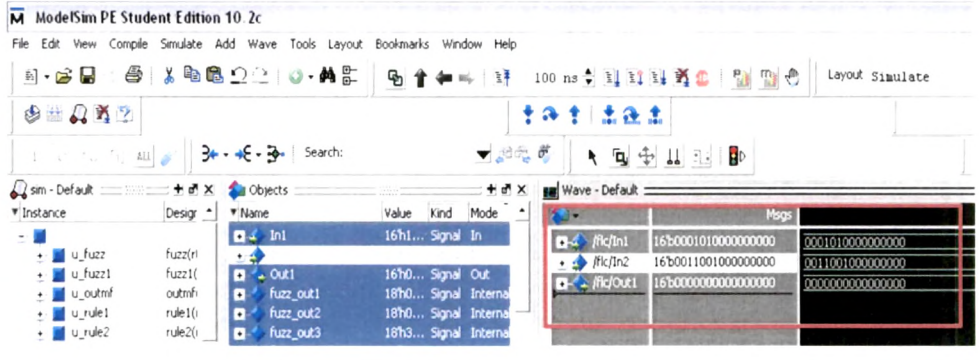

Figure 8.7: ModelSim Simulator Results

5). After verification of the HDL code using ModelSim Simulator, the code is downloaded to the target and the results is verified. FIL simulation mode is used for close-loop simulation with LTE-A Link Level Simulator.

8.1.3.2 Implementation on TMS320C6713 DSP Starter Kit

The MATLAB Simulink Fuzzy Logic Decision model is implemented and real-time testing is done on C6713 DSP Starter kit. The standalone C code of the Simulink model is generated using the Simulink Coder. The generated code for the Target Device C6713 is used for real-time applications, including simulation, rapid prototyping and hardware-in-the-loop testing.

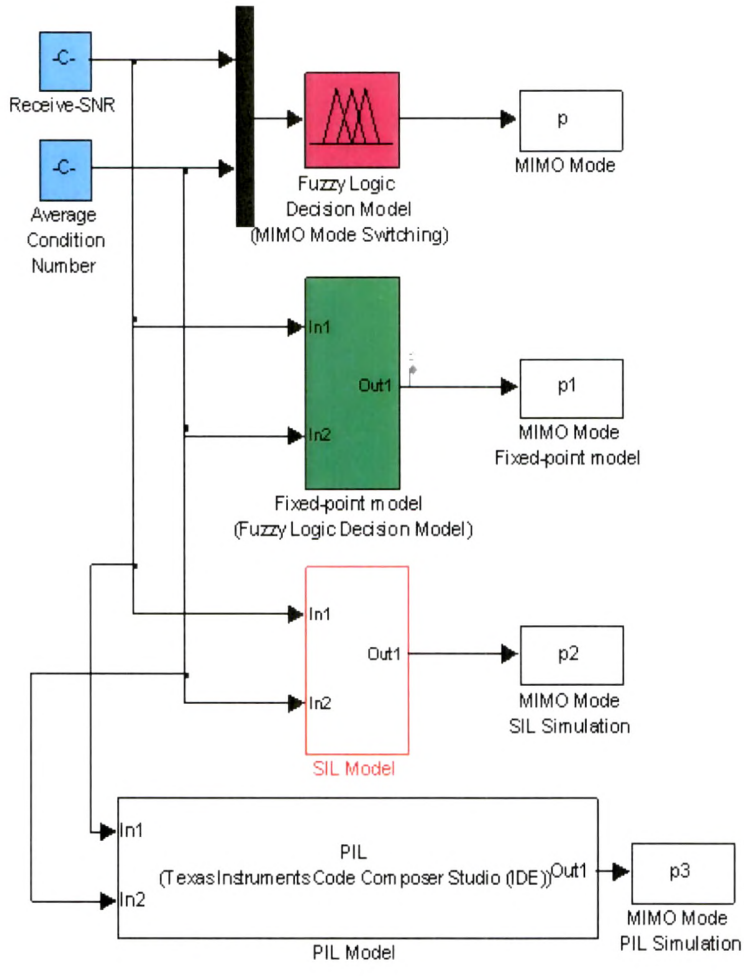

Figure 8.8: Simulink Model for FL Decision model for SIL and PIL Simulation

Using the Simuink Coder the Simulink model is build for C code generation for the Target device specified. Once the code is generated, the SIL simulation is carried out using CCS IDE. The C code is verified with software simulator and then downloaded to the target for in-loop testing. Using PIL Simulation mode, the PIL block is generated and the code is verified with in-loop testing with LTE-A Link Level Simulator. Figure 8.8 shows the MATLAB Simulink blocks for FLC, SIL model and PIL model for Texas Instruments CCS IDE. The snapshot of the CCS IDE is as shown in Figure 8.9.

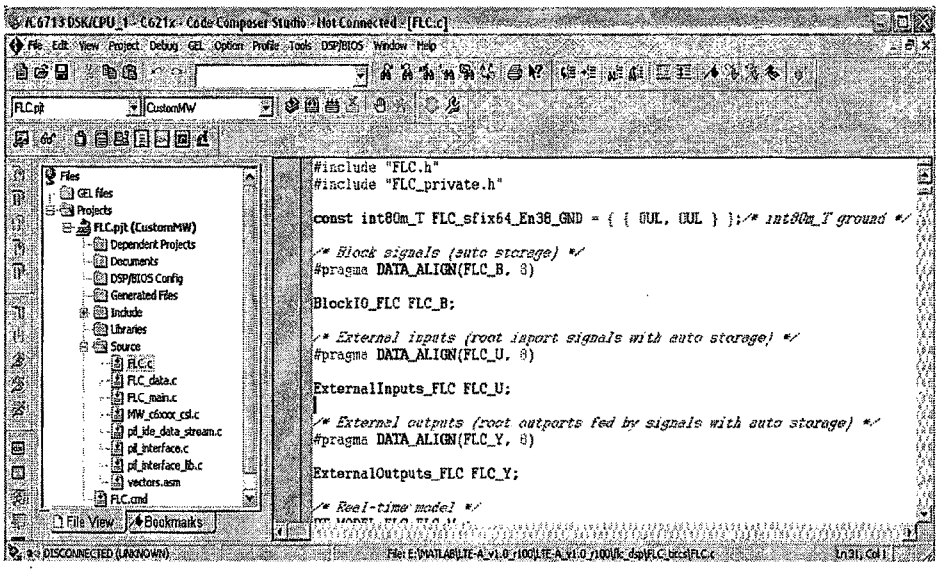

Figure 8.9: Code Composer Studio IDE Window

8.1.3.3 Implementation Results

GUI is developed to ease the Throughput Analysis for FL Decision Model for MIMO mode Switching in LTE-A Downlink Physical Layer. The User Manual and steps for setup for real-time implementation using the GUI is given in Appendix A. The user can select the Initial Simulation parameters using the Pop-up menu editor for Average SNR, Antenna Configuration, Receiver Configuration, Channel Configuration, Transmit Correlation and MIMO mode. The average condition number, Receive SNR and MIMO mode selected using FL Decision model is displayed in GUI.

Simulation results for different Initial Simulation Parameters, with FL Decision Model for MIMO mode switching is implementation on DSP and on FPGA. Figure 8.10-8.15 shows the results of throughput for various six different Case scenarios to test the performance of FL Decision model with different antenna configurations, transmission modes and channel configuration.

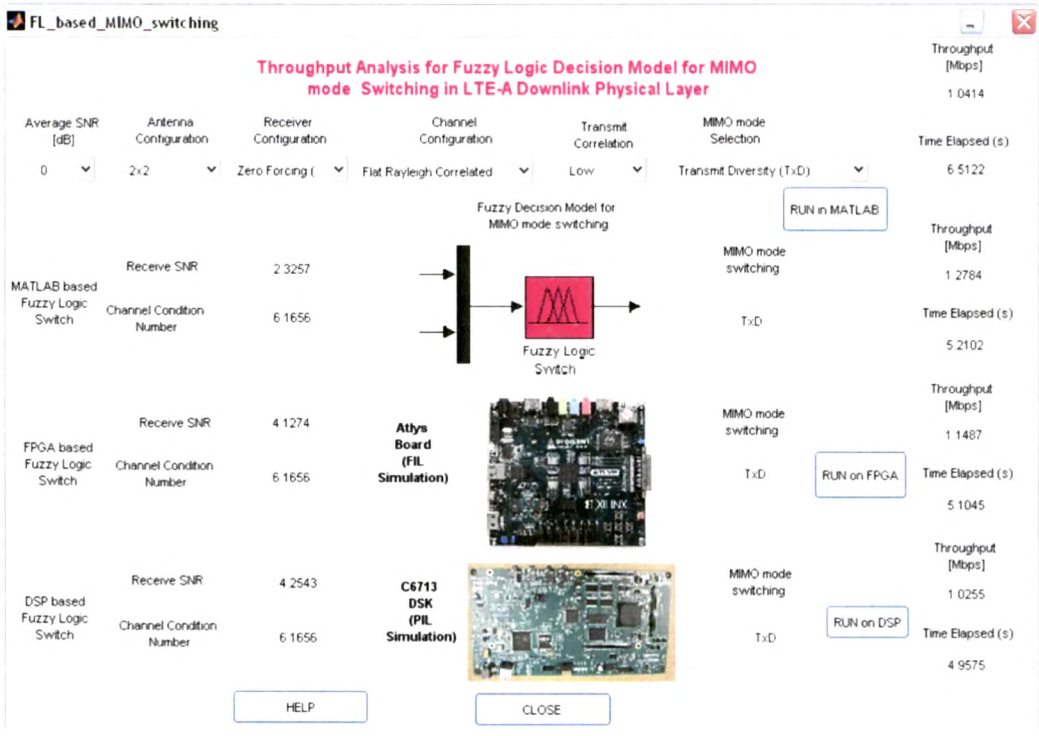

Figure 8.10: Throughput Analysis of Case 1 Scenario

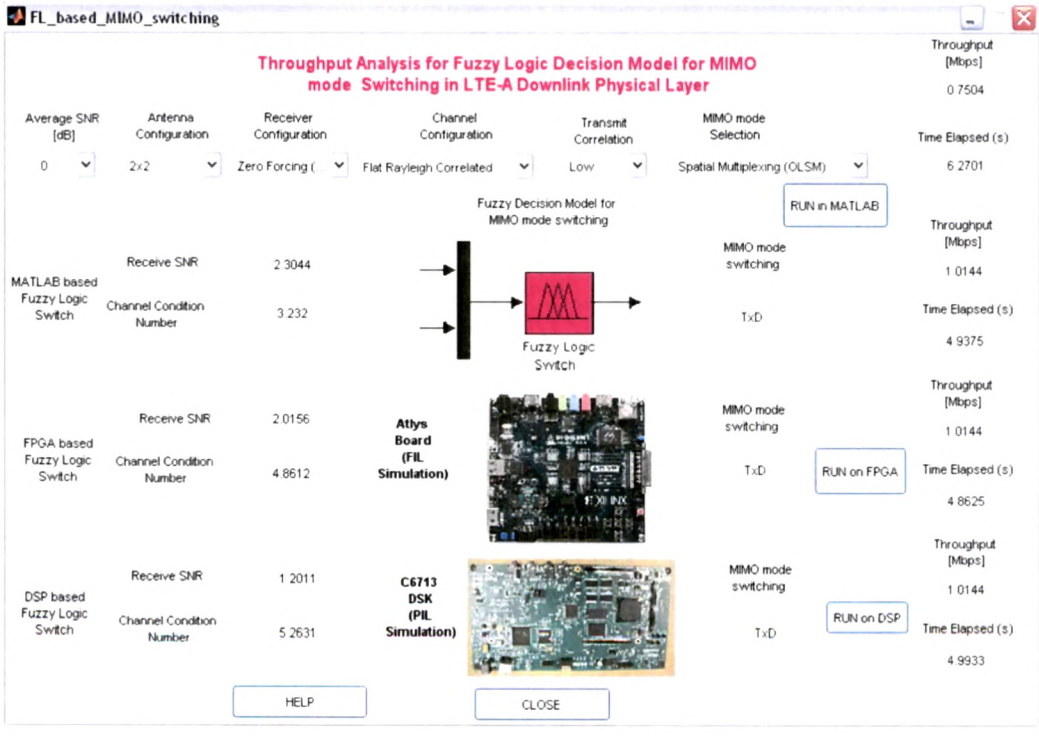

Figure 8.11: Throughput Analysis of Case 2 Scenario

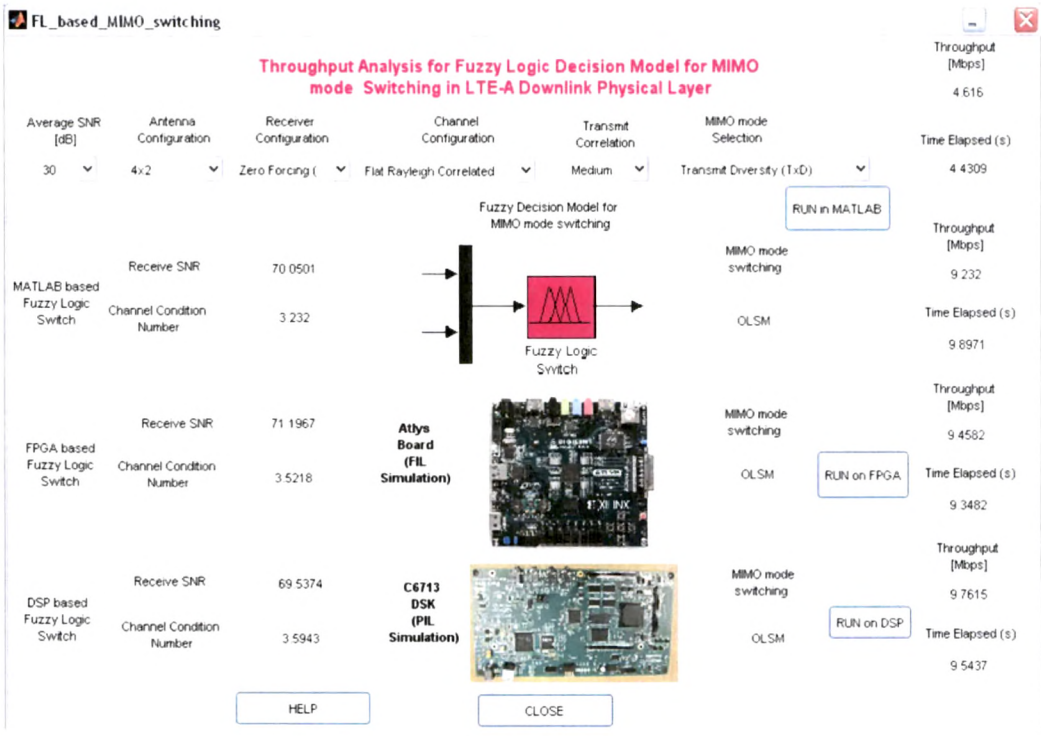

Figure 8.12: Throughput Analysis of Case 3 Scenario

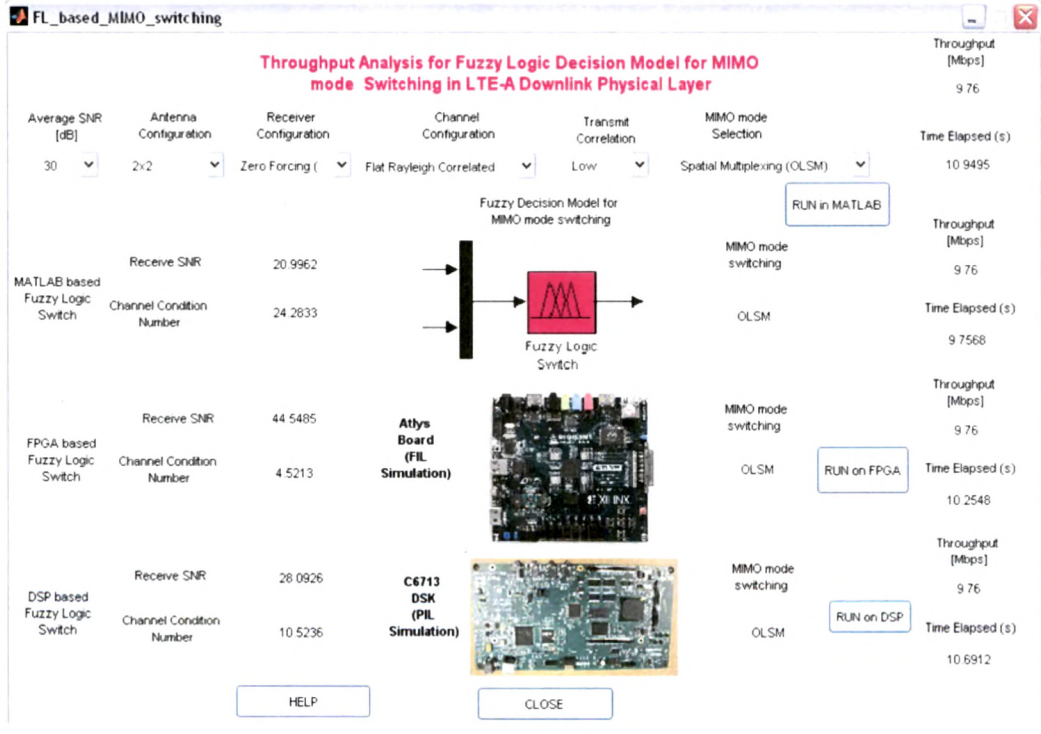

Figure 8.13: Throughput Analysis of Case 4 Scenario

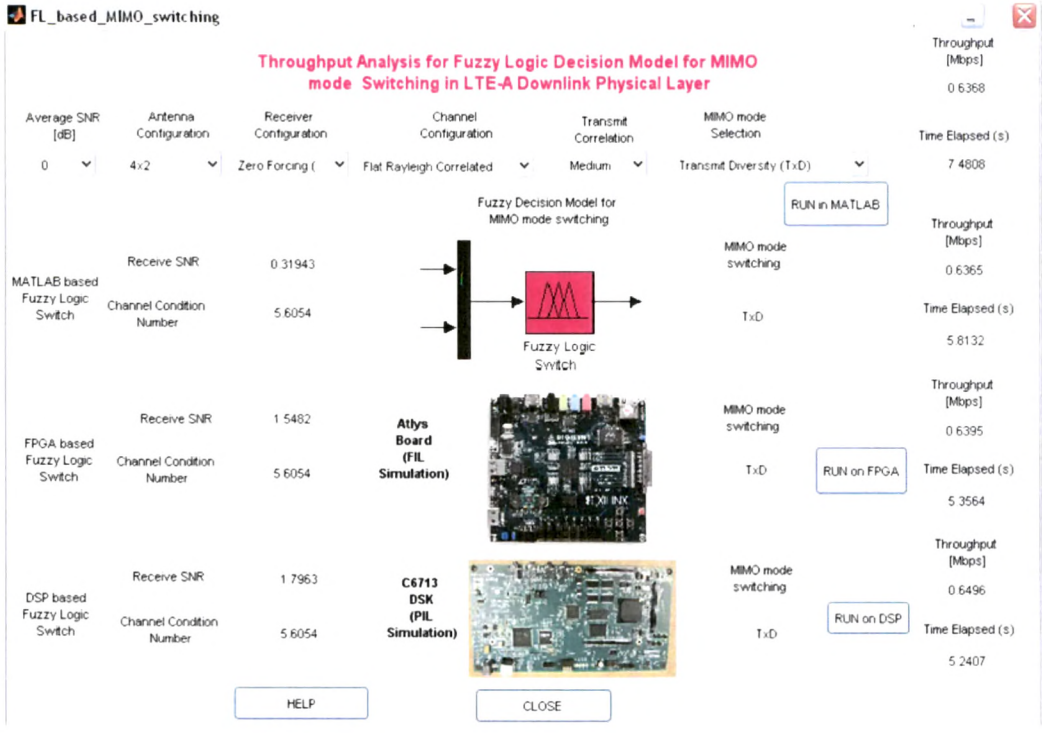

Figure 8.14: Throughput Analysis of Case 5 Scenario

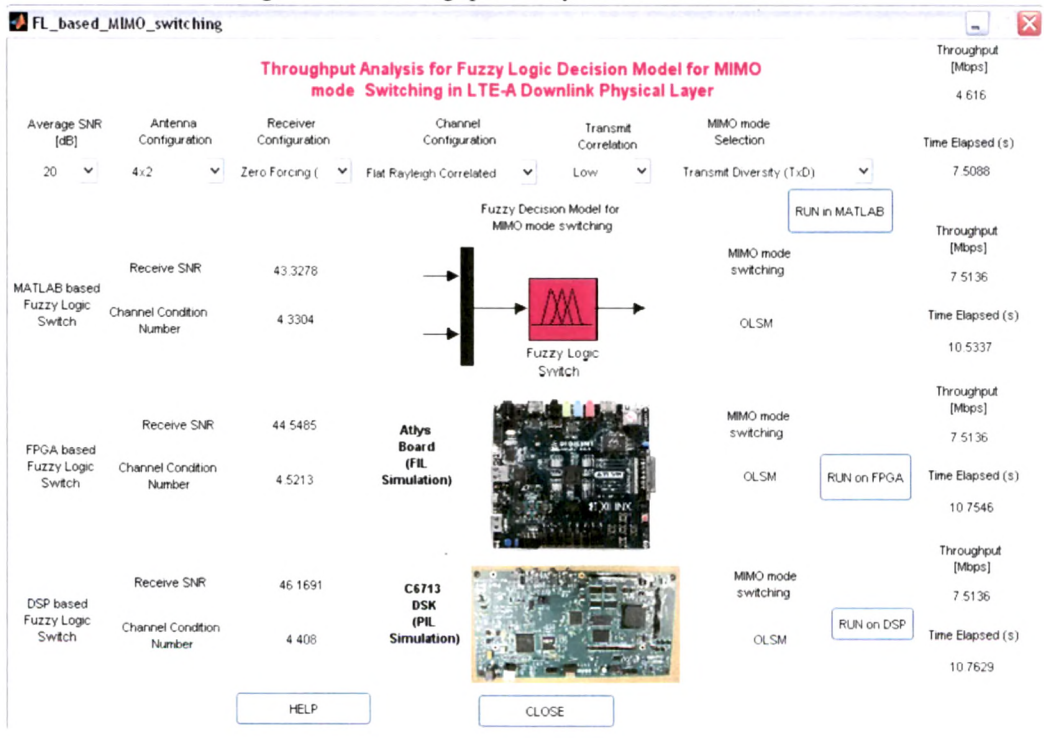

Figure 8.15: Throughput Analysis of Case 6 Scenario

Initial Simulation Parameters Scenarios	Initial Throughput (Mbps)	FL Decision Model Throughput (Mbps)	FPGA Throughput (Mbps)	DSP Throughput (Mbps)
Case 1: 0dB,2x2, Low Correlation, TxD	1.0414	1.2784	1.1487	1.0255
Case 2: 0dB,2x2, Low Correlation, OLSM	0.7504	1.0144	1.0144	1.0144
Case 3: 30dB,4x2, Medium Correlation, TxD	4.616	9.232	9.4582	9.7615
Case 4: 30dB,2x2, Low Correlation, OLSM	9.76	9.76	9.76	9.76
Case 5: 0dB,4x2, Medium Correlation, TxD	0.6368	0.6365	0.6395	0.6496
Case 6: 20dB,2x2, Low Correlation, TxD	4.616	7.5136	7.5136	7.5136

Table 8.1: Summary of throughput results for various case scenarios for FL Decision model

Table 8.1 shows the summary of throughput results for various case scenarios to test the throughput performance of LTE-A Downlink Physical Layer with FL Decision model and its implementation.

8.1.4 Implementation of ANN based MIMO Channel Estimation

The ANN based MIMO Channel Estimation Algorithm developed is discussed in detail in Chapter 6. GRNN based MIMO Channel estimation algorithm is implemented and verified in close-loop with LTE-A Link Level Simulator for Throughput Analysis.

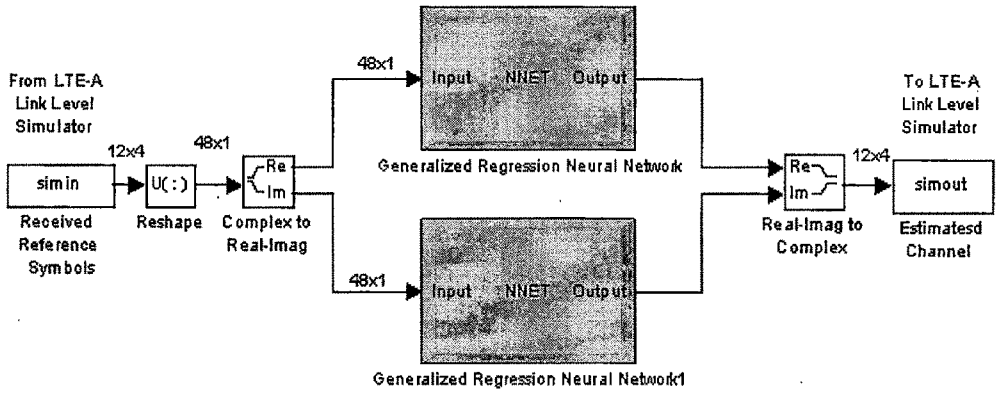

Figure 8.16: ANN based MIMO Channel Estimation Simulink Model

Out of different ANN based MIMO Channel Estimation Techniques, GRNN is implemented as the time taken for the technique is minimum as compared to others and also it gives better per-

formance in terms of throughput as compared to other channel estimation techniques. The input to Neural Network is 12x4 matrix Received reference symbol and output channel estimated is also 12x4 channel matrix. After reshape the input data is 48x1. The ANN cannot support complex data as input and training data, hence two neural networks are designed one for real part and other for imaginary part. The MATLAB Simulink model for ANN is as shown in Figure 8.16.

If we convert the model to Fixed-point model and consider sfixed data of 16 bits (8 fraction bits), the input should be equal to 48x1 data. So if we assign 16 pins for each data, we need 16x48 = 768 pins for input and 768 pins for output. Hence, real-time verification of channel estimation algorithm on FPGA is not practically feasible due to limitation of IOB's on Atlys Spartan 6 Development kit.

8.1.4.1 Implementation on TMS320C6713 DSP Starter Kit

The GRNN based MIMO channel estimation technique is implemented on TMS320C6713 DSK. The real-time verification is done with LTE-A Link Level Simulator. MATLAB Simulink model of GRNN based Channel Estimation developed is implemented on C6713 DSK.

Similar procedure as discussed in Section 8.1.3.2 for implementation on TMS320C6713 DSK is followed. Software simulation is verified using Code Composer Studio 3.3 and the code is download to the Target device TMS320C6713 and verified in close loop with LTE-A Link Level Simulator. GUI is developed for Throughput Analysis of ANN Based MIMO Channel Estimation in LTE-A Downlink Physical Layer is developed. Throughput for Perfect, LS, GRNN and DSP based channel estimation can be analyzed in GUI.

8.1.4.2 Implementation Results

GUI is developed for to ease the Throughput Analysis for ANN based MIMO Channel Estimation in LTE-A Downlink Physical Layer. The User Manual and steps for setup for real-time implementation using the GUI is given in Appendix A. The user can select the Initial Simulation parameters using the Pop-up menu editor for Average SNR, Antenna Configuration, Receiver Configuration, Channel Configuration , Channel Estimation Technique and MIMO mode. After running simulation the average condition number, Receive SNR and MIMO mode selected using FL Decision model is displayed in GUI. The comparative analysis for throughput and Elapsed time can be observed. GUI also consists of options for Simulations of GRNN based MIMO channel estimation on TMS320C6713 DSK for throughput analysis.

Simulation results for different Case Scenarios with FL Decision Model for MIMO mode switching implementation on DSP is as shown in Figure 8.17-8.22.

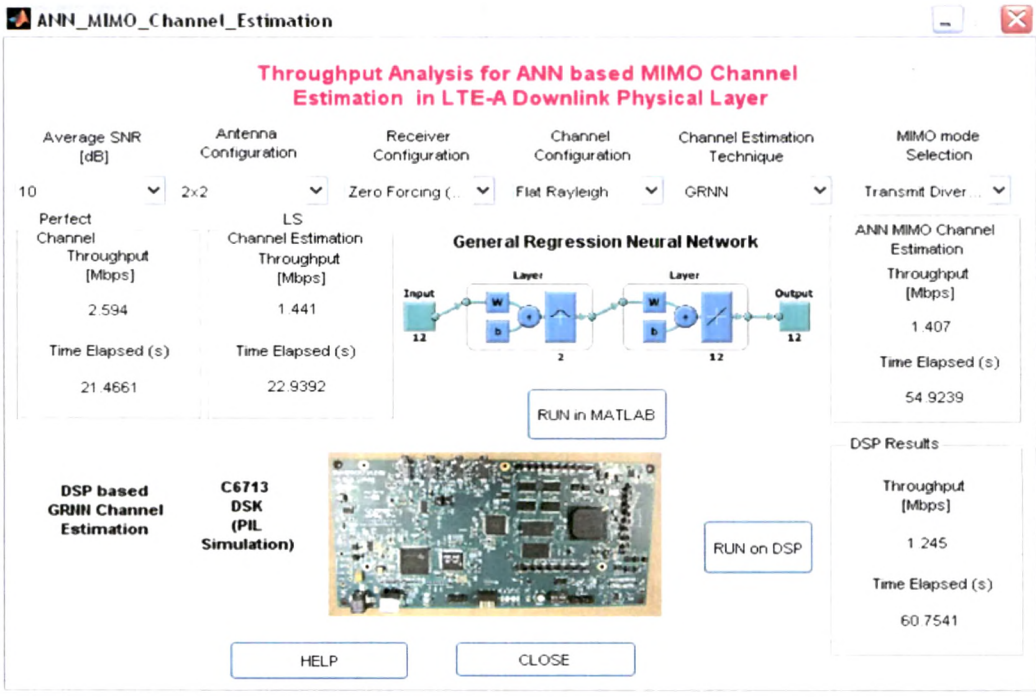

Figure 8.17: Throughput Analysis of GRNN Case 1

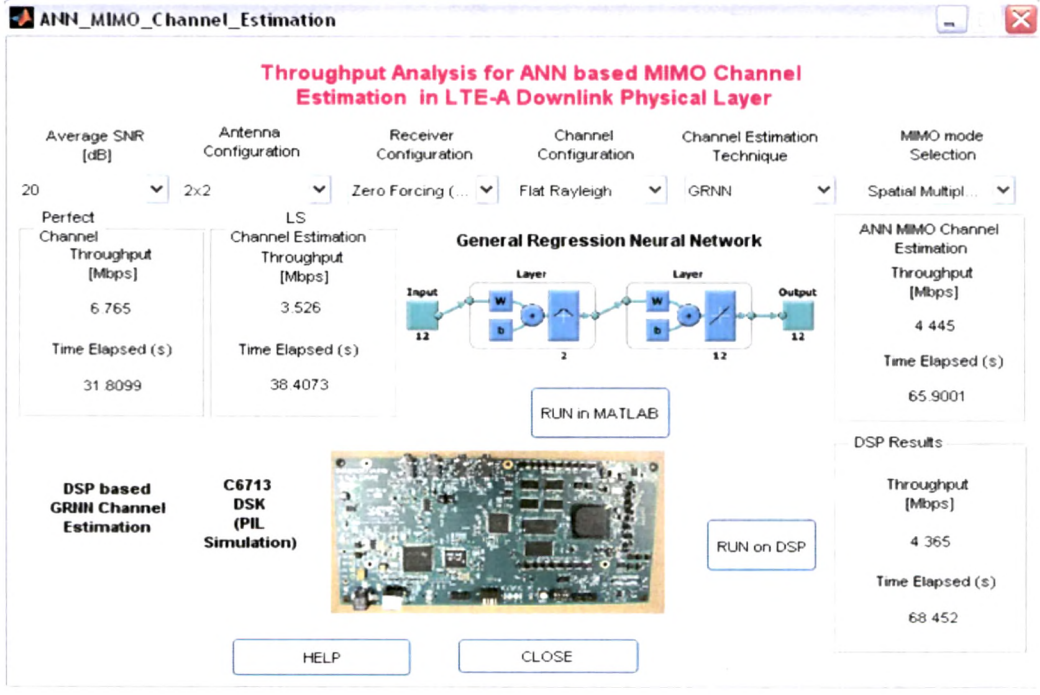

Figure 8.18: Throughput Analysis of GRNN Case 2

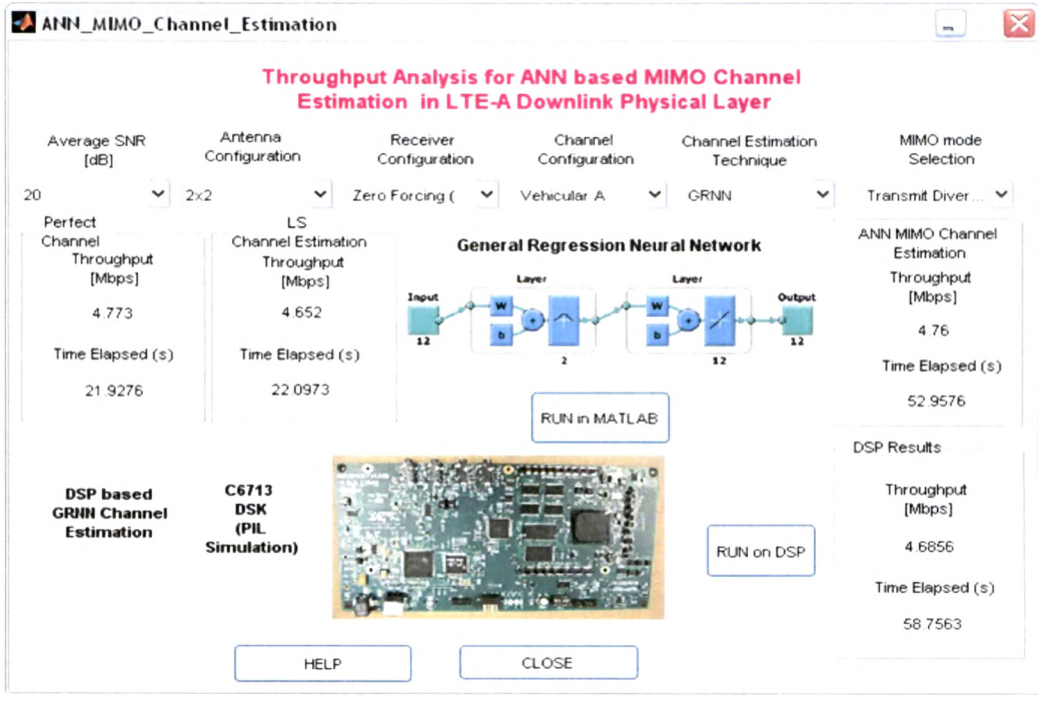

Figure 8.19: Throughput Analysis of GRNN Case 3

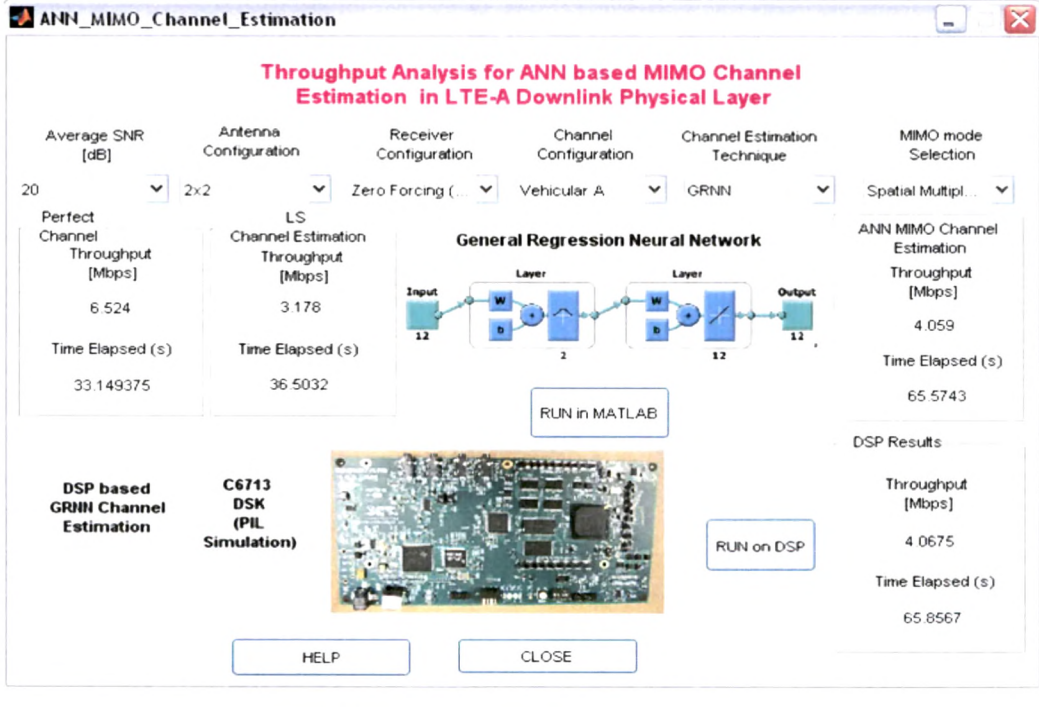

Figure 8.20: Throughput Analysis of GRNN Case 4

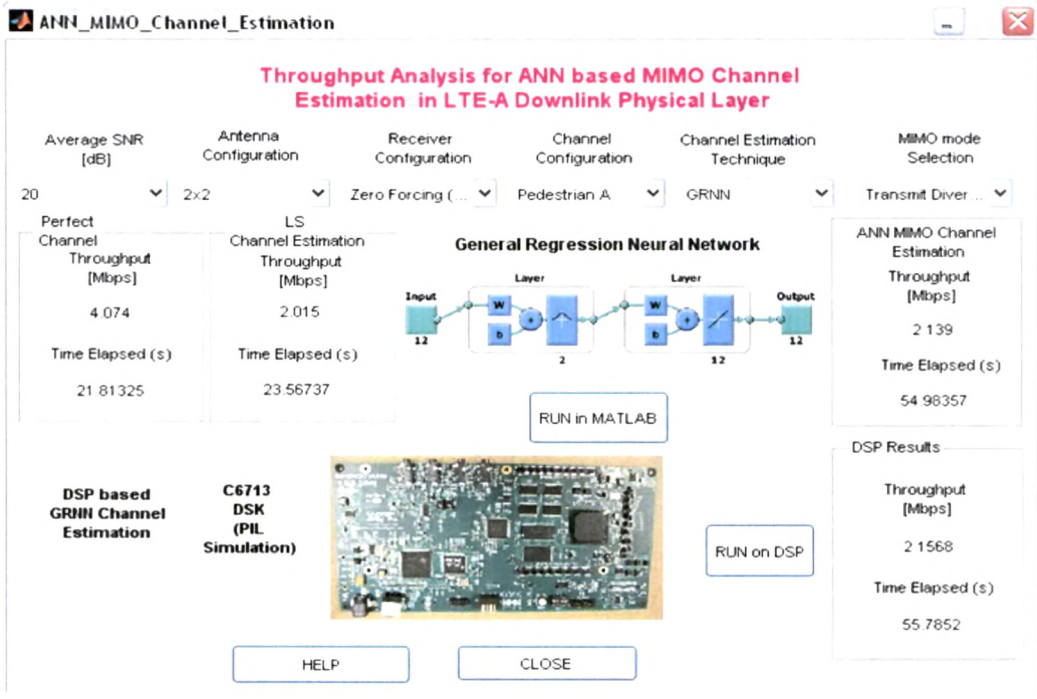

Figure 8.21: Throughput Analysis of GRNN Case 5

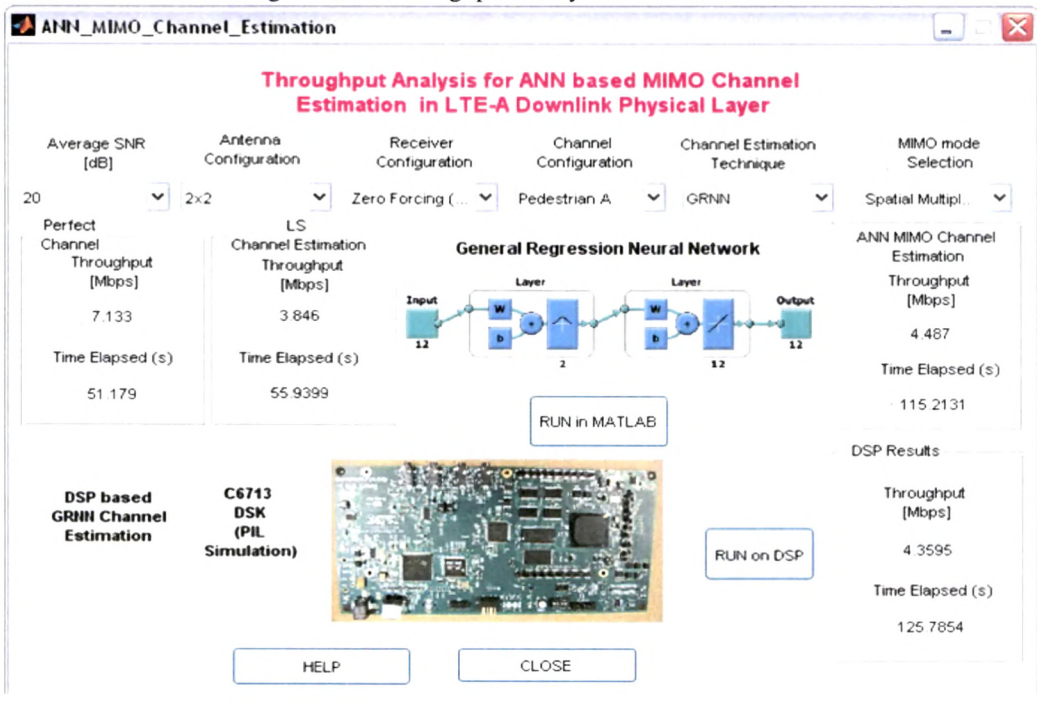

Figure 8.22: Throughput Analysis of GRNN Case 6

Table 8.2 shows the summary of throughput results for different simulation parameters and channel estimation techniques and DSP implementation of GRNN based channel estimation.

Simulation parameters Case Scenarios	Perfect channel (Mbps)	LS (Mbps)	GRNN (Mbps)	DSP (Mbps)
Case 1: 10 dB, 2x2 TxD, Flat Rayleigh	2.594	1.441	1.407	1.245
Case 2: 20 dB, 2x2 CLSM, Flat Rayleigh	6.765	3.526	4.445	4.365
Case 3: 20 dB, 2x2 TxD, Veh A	4.773	4.652	4.76	4.6856
Case 4: 20 dB, 2x2 OLSM, Veh A	6.524	3.178	4.059	4.065
Case 5: 20 dB, 2x2 TxD Ped A	4.074	2.015	2.139	2.1568
Case 6:20 dB, 2x2 OLSM Ped A	7.133	3.846	4.487	4.3595

Table 8.2: Summary of throughput results for case scenarios for ANN Channel estimation

8.2 Concluding Remarks

This chapter presents the real-time verification of the developed throughput optimization algorithms on Atlys Spartan 6 Development kit and TMS320C6713 DSK. The GRNN based MIMO channel estimation and FL Decision model for MIMO mode switching in LTE-A Downlink Physical layer are implemented on real-time hardware for performance analysis. FL Decision model is implemented on FPGA and DSP and is found to give satisfactory results when compared to MATLAB Simulation result. GRNN MIMO channel estimation is implemented on DSP and gives similar performance to MATLAB Simulation results. Throughput analysis of the algorithms are carried out in close-loop testing with LTE-A Link Level Simulator.