List of Figures

.

Figure No.	Name of Figure	Page No.
2.1	Hybrid Communication Network	14
2.2	A taxonomy of current practice in wireless networking	15
3.1	TOSSIM Architecture	26
3.2	The TrueTime toolbox	29
3.3	Workflow	31
3.4(a)	Ethernet network model for 50 Ethernet stations	33
3.4(b)	Wireless network model for 50 users	33
3.5(a)	Traffic sent (bits/sec) of different scenarios having 25,50,100 users	34
3.5(b)	Traffic received (bits/sec) of different scenarios having 25, 50, 100 use	34
3.6	Collision count in wireless network	35
3.7	Throughput (bits/sec) of different scenarios on node 21 for Ethernet	35
3.8(a)	Data dropped for different scenarios for Wireless LAN	35
3.8(b)	Retransmission attempts of different scenarios for Wireless LAN	35
3.9	Throughput (bits/sec) of different scenarios for Wireless LAN	36
3.10(a)	Throughput of Ethernet and WLAN on node 07	36
3.10(b)	Throughput of Ethernet and WLAN on node 37	36
3.10(c)	Throughput of Ethernet and WLAN on node 97	36
3.11	Hybrid Network	37
3.12(a)	Light Traffic	38
3.12(b)	Heavy Traffic	38
3.13(a)	Delay for Light Traffic	38
3.13(b)	Delay for Heavy Traffic	38
4.1	WSN	40

v

4.2	Simulink model in truetime	47
4.3	Random Network Topology	47
4.4	Results on Command window for MOTES Simulink model	48
4.5	power (mW) V/S average visiting time (Sec)	48
4.6	Receiver threshold level (dbm) V/S Signal Reach	49
4.7	Power (dbm) V/S Signal Reach	49
4.8	Power (mW) V/S Average Visiting Priority for each node	49
4.9	Power (mW) V/S Average Visiting Priority	49
5.1	IEEE820.15.4/ZigBee protocol stack architecture	51
5.2	IEEE 802.15.4 Network Topologies	52
5.3	IEEE 802.15.4 Operational Modes	54
5.4(a)	Non Beacon mode	55
5.4(b)	Beacon mode	55
5.5	the Superframe Structure	56
5.6	Example of the structure of a Superframe	57
5.7	The Inter Framing Spacing	59
5.8	Number of Hopes (Tree, Mesh)	61
5.9	End to end delay	61
5.10	End to end delay for Router 1	61
5.11	Load per PAN	61
5.12	Throughput	62
5.13(a)	Tree structure	62
5.13(b)	Mesh Route	62
5.14	Snapshot of the Network when Coordinator Fails	63
5.15	Load per PAN	64
5.16	PAN Affiliation	64
		VI

5.17	Global Output Report at simulation time 360, 60,720	64
6.1	The structure of the IEEE 802.15.4 Simulation Model	69
6.2	Packet flow structure in GTS enabled mode	71
6.3	The utilization of the transmission time inside the GTS	72
6.4	Simulation model	75
6.5(a)	GTS throughput v/s superframe order for 1 k buffer capacity	76
6.5(b)	GTS throughput v/s superframe order for 4 k buffer capacity	76
6.6	Global Throughput v/s BO	77
6.7(a)	PMAD v/s superframe order for 4 k buffer capacity	78
6.7(b)	PMAD v/s superframe order for 1 k buffer capacity	78
6.8	Wasted Bandwidth v/s superframe order for 4 k buffer capacity	79
6.9	Comparisons of Wasted Bandwidth Results	81
7.1	an Artificial Neuron	84
7.2	MATLAB Command Window	88
7.3	Simulink View	88
7.4	ANFIS Editor GUI	89
7.5	ANN with respective inputs and outputs	91
7.6	Training of Artificial Neural Network for Packet size	91
7.7(a)	Packet Medium Access Delay v/s Superframe Order for 700 bits Packet	92
	Size	
7.7(b)	Packet Medium Access Delay v/s Superframe Order for 50 bits Packet	92
	Size	
7.8 (a)	GTS Throughput v/s Superframe Order for 700 bits Packet Size	93
7.8(b)	GTS Throughput v/s Superframe Order for 50 bits Packet Size	93
7.9 (a)	Wasted B.W. v/s Superframe Order for 700 bits Packet Size	93
7.9 (b)	Wasted B.W. v/s Superframe Order for 50 bits Packet Size	93
7.10	ANFIS training	94

VП

	7.11	System Setup for ANFIS based GTS Mechanism	. 95
	7.12(a)	Result analyses among traditional, ANN and ANFIS GTS Mechanism	95
	7.12(b)	Result analyses among traditional, ANN and ANFIS GTS Mechanism	95
	7.13	Soft GTS Mechanism Simulator	97
	7.14	Snapshot of menus facility provided in given simulator	97
	7.15	Snapshot of GTS Throughput result in designed simulator	98
	8.1	Design Flow	99
	8.2	Design implementation of ANN on FPGA	101
	8.3	Output of ANN from ISIM Using VHDL code	102
	8.4	Relative Difference	103
	8.5	Hardware setup of ANN configuration on FPGA kit	104
	8.6	Enlarge view of Spartan 6 demo Kit	104
	8.7	Snapshot of programming FPGA kit	105
	8.8	Output on LED for given combination of the inputs	105
	8.9	Typical wireless sensor nodes size	106
	8.10	Wireless sensor node components	106
	8.11	MICAz mote [courtesy Crossbow]	107
	8.12	Photo of top view of an MIB520CB	108
a	8.13	MDA 100CB	109
	8.14(a)	Programming Environment of Motes	111
	8.14(b)	Programming Environment of Motes	111
	8.15	Snapshot of successful programming done in motes	11 2
	8.16	Screenshot of the database in Health view	11 2
	8.17	Experimental Test bed using MICAz Motes	113
	8.18(a)	Simulation Test bed	114
	8.18(b)	MICAz Nodes & Gateway Setup	114
	8.19	Snapshot of connecting mote on gateway through USB port	115

8.20	Snapshot of Uploading program	115
8.21	Test bed versus Simulation results	116
A.1	Project Navigator Desktop Icon	136
A.2	New Project Wizard—Create New Project Page	136
A.3	New Project WizardDevice Properties Page	137
A.4	Adding VHDL Test Bench	137
A.5	Process Pane	138
A.6	ISim Properties Dialog Box	138
A. 7	ISim Graphical User Interface	139
A.8	Cable Set up	140
A.9	Cable Communication Setup	140
A.10	Snapshot of Boundary Scan	141
A.11	Program Launch Window	141
A.12	Snapshot of Programming Notepad 2	143
A.13	Output Section of PN2	143
A.14	Mode Configurations	144
A.15	Gateway Configuration	145
A.16	Database Configurations	145
A.17	Sensor Board Configurations	146
A.18	MICAz Nodes & Gateway Setup	146
B. 1	Spartan-6 XC6SLX45 CSG324C Evaluation Board	147
B.2	System Setup for FPGA Implementation of ANN	147
B.3	Output observed on LEDs	148
B.4	Crossbow's real time Hardware foe WSN	148
B.5	Mote connected on Gateway Setup	149
B.6	Hardware Setup	149
B.7	Status of Mote when data received	150

B.8	Snapshot of uploading Program	150
D.1	IEEE 802.15.4 WSN -User Interface	152
D.2	IEEE 802.15.4 WSN -Documentation	152
D.3	IEEE 802.15.4 WSN –Hardware Implementation Menu	153
D.4	IEEE 802.15.4 WSN -Demo	153

÷

2 1 1 . .

Х