Chapter 6

DSP based techniques for processing of power quality parameters

6.0 Introduction

In this chapter a **D**igital **S**ignal **P**rocessor (*DSP*) based real time digital signal acquisition and processing of various power quality parameters is described. The proposed system is centered on a Texas Instruments 32-bit fixed point *TMS320F2806 DSP*. An in house *DSP* board is developed and multiprocessor system is implemented for real time measurement and processing of various power quality parameters. The firmware for the various algorithms proposed before in earlier chapters for measurement of frequency, power, harmonics and flicker is done in C-language. The multiprocessor architecture is also interface to *personnel computer* (PC) using the *RS232* port. *Visual Basic (VB)* based software is developed for capturing and display of all the data to the computer. Three phase voltage and current signals are continuously sampled by each of the card of the multiprocessor architecture and the digital values of these signals are evaluated by DSP processor to compute various power quality parameters. Continuous measurement of power quality parameters such

as voltage, current, frequency, active power, reactive power, 4-quadrant power measurement, power factor, harmonics and flicker are measured and captured on PC *(Personnel Computer)*. The proposed system is flexible and can be upgraded in future to capture remaining power quality parameters (PQ).

6.1 Application of DSP for PQ Measurement

DSP designs are optimized to handle real-time applications with high bandwidth requirements. In the following, the features native to DSPs that facilitate high throughput are illuminated [53]–[56]. DSPs architecture are built with Harvard architecture. This configuration employs separate program and data memories and associated data and address buses. The benefit of this arrangement is increased speed because instructions and data can move in parallel instead of sequentially [58]. DSPs, like many advanced microprocessors, use pipelining to operate on several instructions simultaneously [59].

1) **Hard-Wired Logic:** In DSPs, most instructions execute in one machine cycle because all functions are performed internally in hard-wired logic. Hardware multipliers in DSPs perform multiplication in a single cycle.

2) **Scaling:** Hardware shifters allow scaling of data used in computations. This helps prevent overflows, and keep the required precision [57].

3) **Saturation:** In DSPs, the accumulator handles overflow by saturating to the most positive or least negative value, thus eliminating rolling over.

4) **Word Length:** Some DSPs support a large word length, thus reducing the quantization error. They also support a larger intermediate word length for intermediate computational results.

5) **Other Features**: Many DSP chips include input/output (I/O) functionality, timing circuitry, internal analog to digital converter (ADC), and high-speed memories on-chip.

DSPs also significantly increase execution speed by performing multiple operations in parallel. For instance, in the same instruction cycle that a MAC operation is being performed, a parallel data move can be carried out. Thus, the special DSP instructions supplement the computational speed of DSPs and make them ideal for high-performance real-time applications

The present day DSP hardware makes it possible to perform online calculation of power quality parameters. In this thesis a Texas Instrument DSP TMS320F2806 based power quality measurement is described. The TMS320F2806 is a 32-bit floating point digital signal processor available from Texas instruments. The 60-ns cycle time allows it to execute operations at rate of 33MFLOPS. The device performance is also enhanced through its large on-chip memories, two internal 10-Bit analog to digital converter ADC.

Digital signal processors (DSP) are distinct from general-purpose microprocessor, mainly due to their capacity for real-time computing. With more optimized architectures towards faster multiplications and accumulations than general-purpose microprocessors, DSPs have wide applications in speech, digital audio, image, and video processing, and telecommunications.

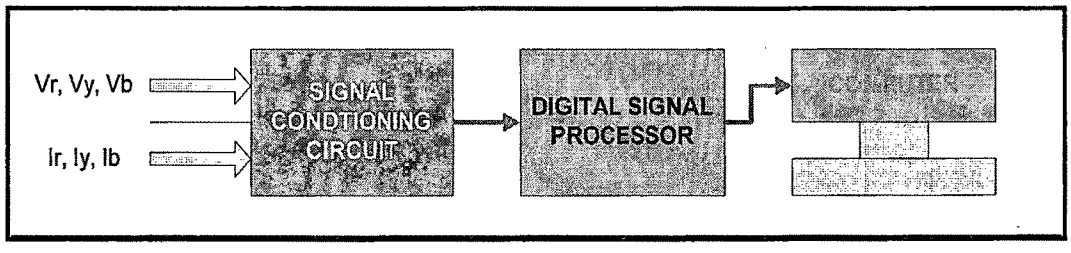

Fig. 6.1-1 General Block diagram of DSP based measuring instrument

1. Signal conditioning:

Non-electrical signal coming from the various sources are converted into scalable voltage using the current and voltage transducers. Signal conditioning is further necessary to adapt the output scale range of the transducers to the input signal characteristics of the A/D converters. Programmable Gain Amplifiers are usually used to adjust the scale range of the input electrical signal with a properly scaled factor.

In addition, a prefitering of the input signal is usually done. The maximum sampling rate of signal acquisition is known a *priori* on each and every DAQ system. On the other hand, Nyquist's Sampling Theorem states that, for a correct and unique digital representation of sampled signals, the maximum frequency of the analog signal must be less than half of the sample rate.

$$f_{INmax} < \frac{1}{2} F_s \qquad (6.1)$$

Where: f_{INmax} is the maximum frequency of the input signal and F_s is the sampling rate.

Therefore, the input signal is pre-filtered with a proper low-pass filter of analog type (an R-C). This operation eliminates the signal aliasing phenomena. The frequency of the low pass filter in each case is twice that of the sampling frequency.

2. Analog-to-Digital conversion (ADC):

Analog to digital conversion of signals is one of the main goals of a data acquisition system. A/D conversion is the set of operations that establish an exact correspondence between an analog electrical value (current, voltage) and a finite-length binary code.

ADC is a three phase process as shown in Fig. 6.1-2, all of them being currently performed sequentially by a monolithic device-the analog-to-digital converter.

Periodic extraction of values samples from the input analog signal $x(t)$ in Fig. 6.1-2 is the first step of the A/D conversion-"sampling". In most cases the sampling period is constant (T_s). The resulting signal is a discrete time signal. As depicted in Eq 6.2 sampling establishes a direct relation between the two independent time-variables, t (continuous time) and n (discrete-time).

$$t = n.T_s \tag{6.2}$$

Sampling is needed for practical reasons: the value of the signal at the input of the quantization module must be constant while quantization is performed. Consequently the sampling period corresponds exactly to the quantization period

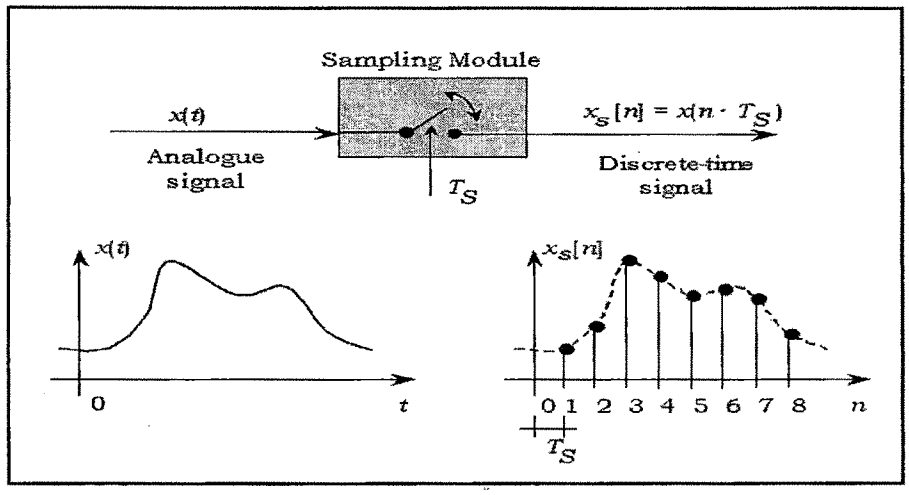

Fig. 6.1-2 Uniform sampling of signals

The last step employed by the A/D conversion is binary coding. This operation assigns a distinct code of $b-bits$ length to each quantization level. Therefore, the quantization resolution b also specifies the length of the resulting binary code of the A/D conversion process. There are many coding schemes used of map the quantization values into binary codes. The most frequency used are presented in Table 6.1-1

Quantization level for $x_q[n]$	Corresponding binary code
$x_q^{max}[n]$ (FSR)	1 1 . . . 1 1
$x_q^{max}[n] - 1\ LSB$	1 1 . . . 1 0
. . .	. . .
$x_q^{min}[n] + 1\ LSB$	0 0 . . . 0 1
$x_q^{min}[n]$ (0)	0 0 . . . 0 0

Table 6.1-1 Unipolar straight Binary coding scheme

The entire set of operation described above and employed by the A/D conversion are currently executed by single, monolithic devices i.e DSP.

3. Data communication with DSP

An important problem related to DSP systems is how data communication with the DSP system is implemented and managed. Several aspects of the communication problems can be stated as follows:

Speed/data throughput: Major improvements of the communication speed were performed in recent years due to the increasing number of applications requiring high performance data manipulation and processing.

Communication protocol: Special care must be taken regarding design and implementation of the communication interface in a simple and efficient manner. The interface should also match the specifications and communication protocol of the DSP system which actual usually as master.

6.1.1 Architecture of DSP

DSP's are key component of any power quality monitoring algorithm. A DSP system is an autonomous digital electronic device with main functions:

To process discrete-time signals according to well-defined algorithms

To control and command the signal exchange with the environment through DAQ system.

From a larger perspective, a DSP system is a set of particular, highly specialized signal processing algorithm along with the digital automation which implements these algorithms.

Fig. 6.1.1-1 and Fig. 6.1.1-2 present the basic differences of the classic (Von-Neumann) Harvard and the modified Harvard architecture respectively.

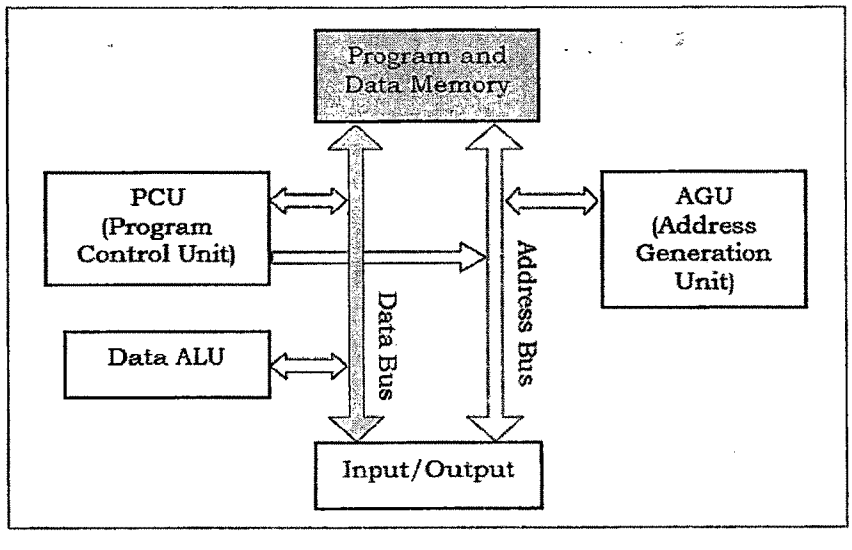

Fig. 6.1.1-1 Von Neumann architecture

Von Neuman architecture specifies a common memory for instruction code (program) and for operands (data). Internal buses of a Von Neumann digital system consist of a Data Bus and an Address Bus as shown in Fig. 6.1.1-2.

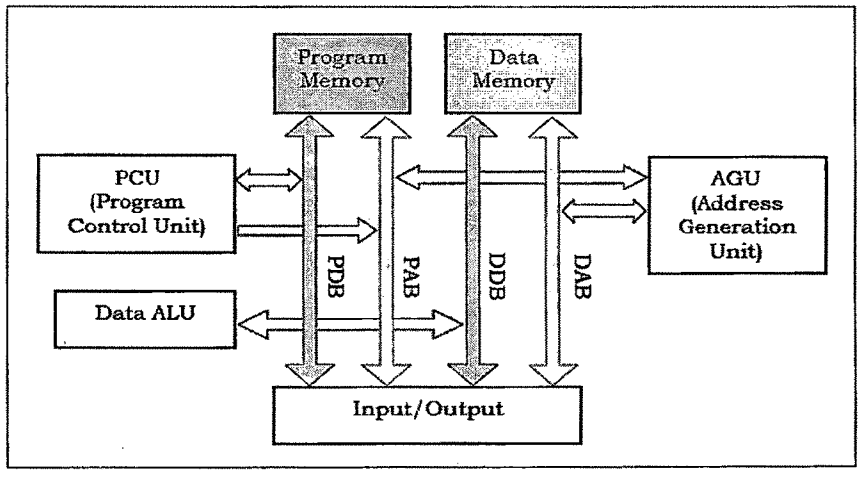

Fig. 6.1.1-2 Harvard architecture

With the Harvard architecture, execution of the convolution loop can be improved by parallelizing arithmetic and logic instruction along with data/address moves. Harvard architectures provide distinct program busses and data busses, which can operate in parallel.

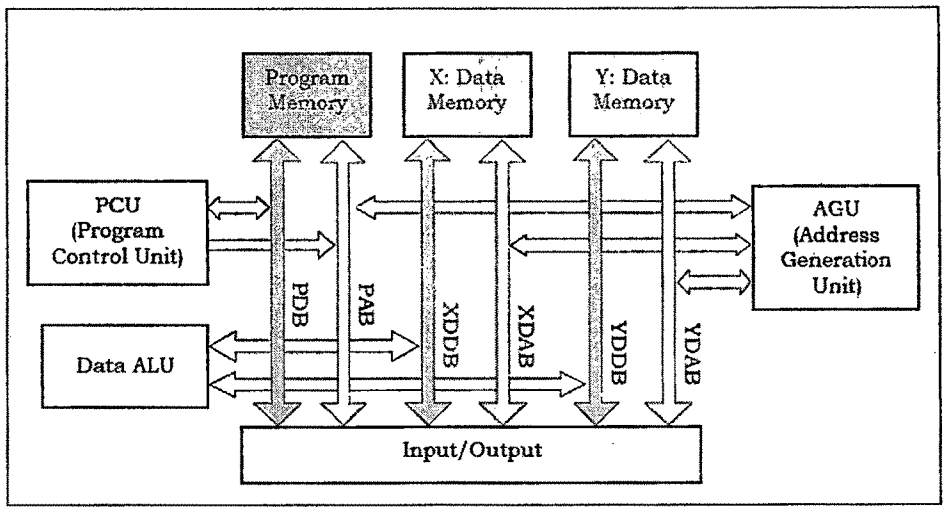

Fig. 6.1.1-3 Modified Harvard architecture

As a result, modified Harvard architectures can significantly increase the instruction parallelism particularly to code sequences that appear more frequently in digital signal processing algorithm, from the statistical point of view.

Examples of the Harvard based DSP architecture includes the Texas Instruments TMS320Cxx family of processors: TMS320C1x, TMS320C2x and TMS320C2xx- fixed point 16-bit DSP as shown in Fig. 6.1.1-4.

The Texas processor TMS320F2806 is chosen for the application is a fixed-point Harvard architecture DSP and can adequately meet the processing requirements at reasonable cost. The TMS320F2806 has microprocessor- style on-chip peripherals, data memory, and a memory expansion port. Its interface capabilities allow the DSP chip to rapidly transfer data into the chip and to interface with the host processor. This provides *12-bit* resolution and dynamic range to handle the voltage and current channel input signal. The DSP has four number of SPI channels making it enable to communicate with four slave devices simultaneously.

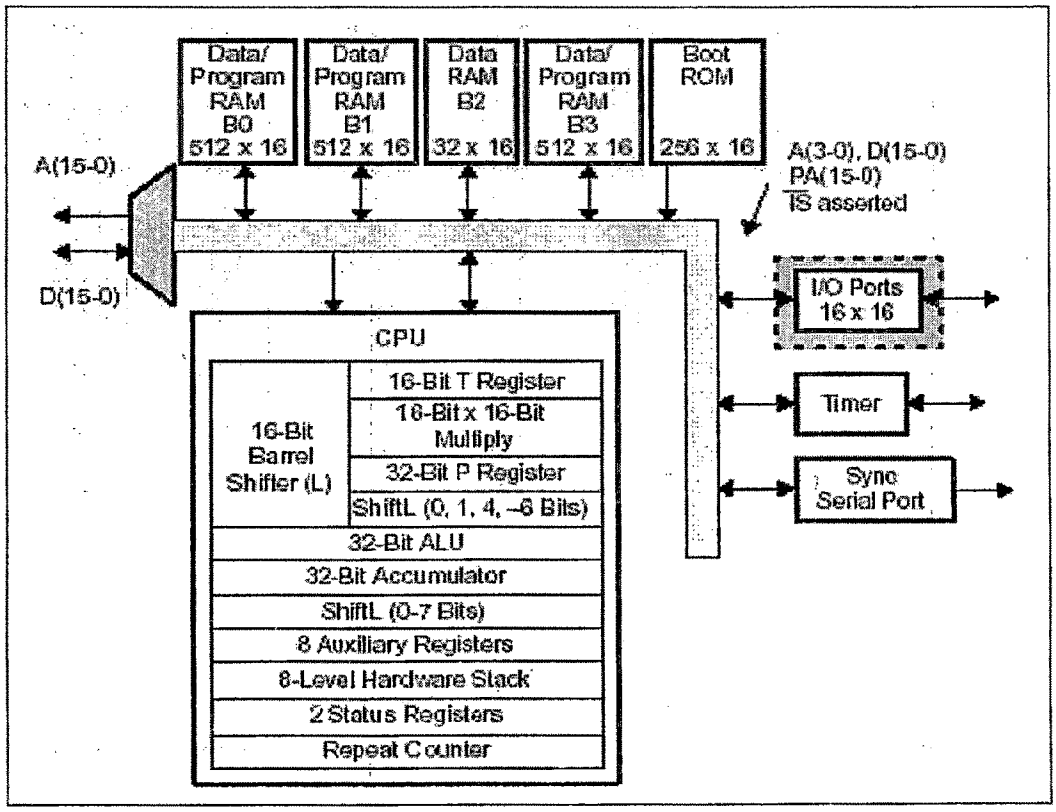

Fig. 6.1.1-5 Block diagram of TMS320F2806

Digital signal processing architectures features additional logic to improve DSP-specific algorithm programming and execution. For example, the Texas TMS320F2806 processor implements the following enhancements. A architecture of TMS320F2806 is as shown in the Fig. 6.1.1-5.

The C28xx DSP generation is the newest member of the TMS320C2000 series DSP platform. The C28x is source code compatible to the 24x/240x DSP devices, hence existing 240x users can leverage their significant software investment. Additionally, the C28x is a very efficient C/C++ engine, hence enabling users to develop not only their system control software in a high-level language, but also enables math

algorithms to be developed using C/C++. The C28x is as efficient in DSP math tasks as it is in system control tasks that typically are handled by microcontroller devices.

The 32 x 32-bit MAC capabilities of the C28x and its 64-bit processing capabilities, enable the C28x to efficiently handle higher numerical resolution problems that would otherwise demand a more expensive floating-point processor solution.

The C28x has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables the C28x to execute at high speeds without resorting to expensive high-speed memories.

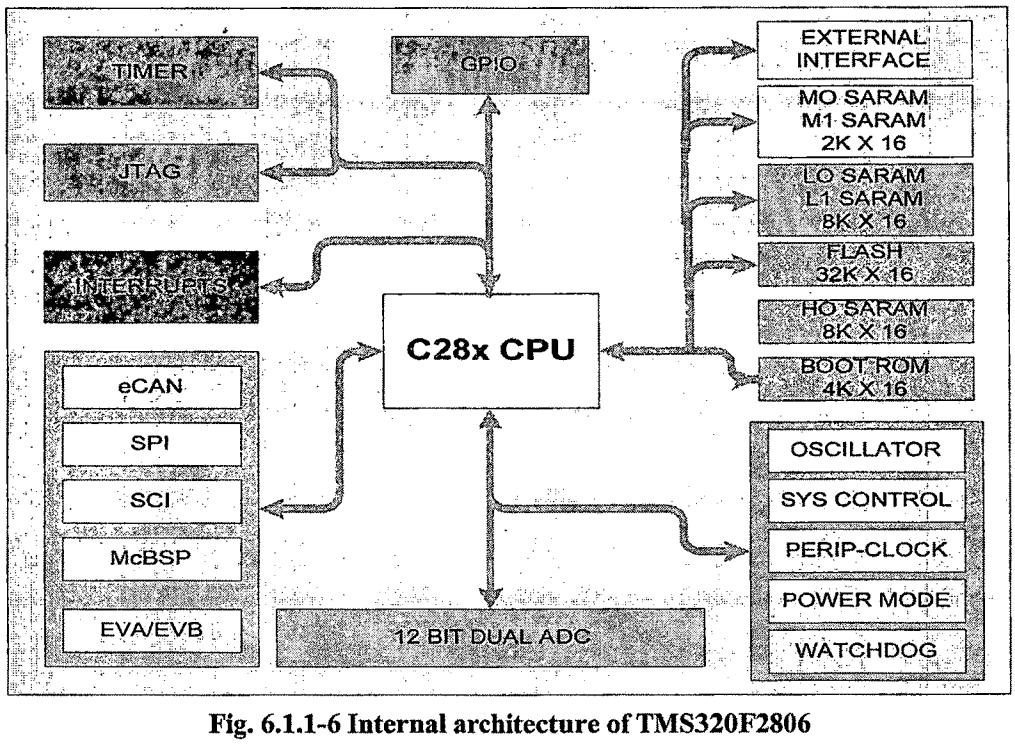

Fig. 6.1.1-6 Internal architecture of TMS320F2806

The high efficiency of digital signal processor (high performance, programming flexibility, reduced power consumption and low cost), along with the corresponding software tools (assemblers, linkers, debuggers and compilers), available to system and application programmers at moderate cost, recommended DSP's as the elegant solution for current signal processing systems.

6.2 Proposed Multiprocessor system

In order to compute various power quality parameters in real time, it was necessary to execute the core at the maximum frequency. It was found that even running the core at 150MHz a single DSP is not able to execute all the various power quality measurement in real time. Since the parameters are highly dynamic. The estimation of frequency require the implementation of the digital filters which require a sampling frequency of 10KHz . Similarly the implementation of the flicker requires to sample the data continuous for an interval of 10 minutes then only the flicker calculation can be performed. Similarly the case of Kalman filters for harmonic estimation and for power measurement.

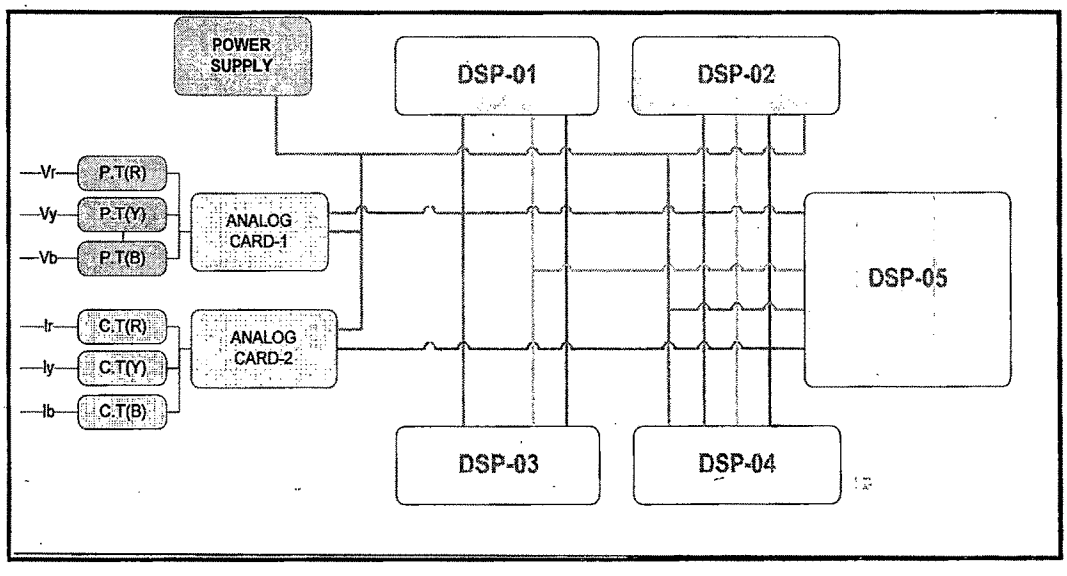

Fig. 6.2-1 Block diagram of multiprocessor system

Hence it was proposed to implement a multiprocessor based power quality measurement system, so as to meet the real time requirements. In this chapter a multiprocessor based architecture is proposed for measurement of power quality parameters. Five multiprocessor cards are interlinked with each other through high speed SPI interface as shown in Fig. 6.2-1. Each card is given three-phase voltage and current signals and the firmware of each card is programmed to execute a single task and to send the result to the master processor. The master processor samples the three phase voltage and current signals and simultaneously captures the data from the various processors and send the data to the PC.

As shown in the Fig. 6.2-2 DSP-01 is used for measuring frequency, DSP-02 is used for harmonic estimation, DSP-3 is used for flicker measurement and similarly DSP-04 is used for 4-quadrant power

measurement. The master DSP samples the voltage and current signals and communicates with the four DSP via a SPI interface. The master DSP communicates with the PC via a RS232 interface.

6.2.1 Schematic of the Signal Conditioning module

As described before the signal conditioning circuit is to be designed so that the actual signal is scaled down to a voltage level suitable to the DSP Analog to Digital converter. The actual signal in this case is the three phase voltage and current signal. Since the voltage level and current levels are very high voltage & current transducers are used here. The voltage transducers used in this case is potential transformer (240/1 Vrms) and for current it is the current transformer. (5/1 Amp). The output of the voltage and current transformers are bipolar signals. The ADC inside the DSP are unipolar hence the bipolar signals needs to be filtered and converted into unipolar signals. As shown in the Fig.6.2.1-1, the schematic diagram of analog signal conditioning circuit. In this circuit TL082 OPAMP is used for signal conditioning circuit. In order to protect the ADC from spikes and overvoltage we have used zener diode for protection.

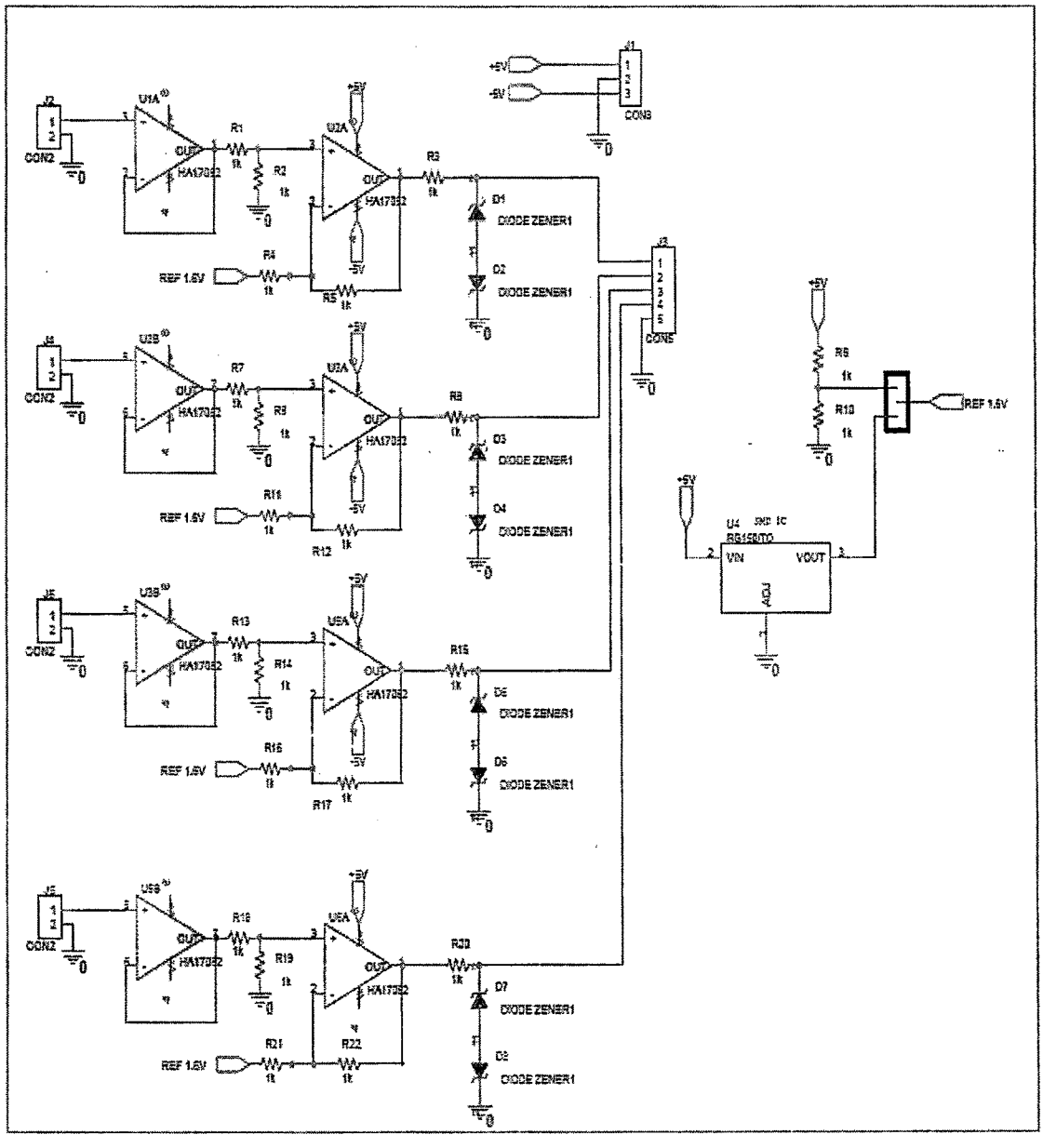

Fig. 6.2.1-2 Analog Signal conditioning circuit

The circuit was first tested on a general purpose board and then final PCB was developed. As shown in the Fig.6.2.1-2 the three individual

single phase transformer were connected with common point connected to ground. The output of the three transformers was then connected to the signal conditioning circuit. In the case of the current, C.T were used to scaled down the signal and then connected to the signal conditioning circuit.

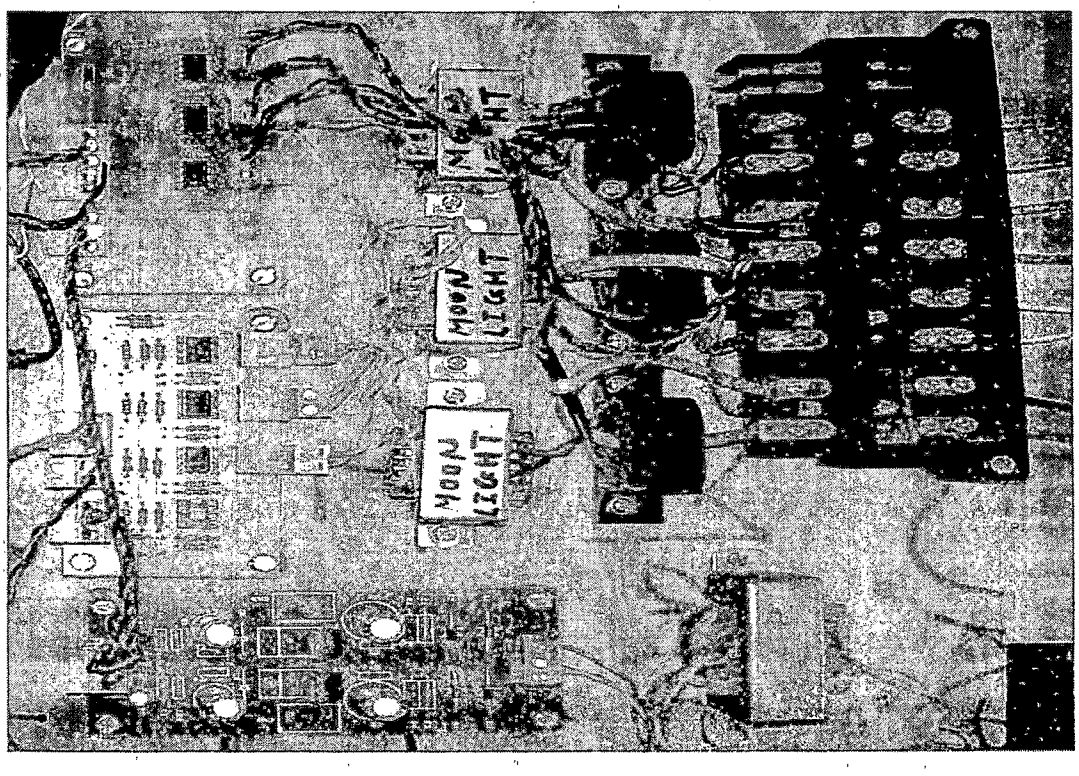

Fig. 6.2.1-3 Photograph of Signal conditioning circuit

In order to remove the complexity of connection three phase voltage and current signal. The three P.T's and the C.T's were enclosed inside a box and the terminals were pulled out for connection of the three phase voltage and current signals as shown in Fig. 6.2.1-3. With the help of the two connectors the scaled down voltage and current signals are connected to the signal conditioning circuit.

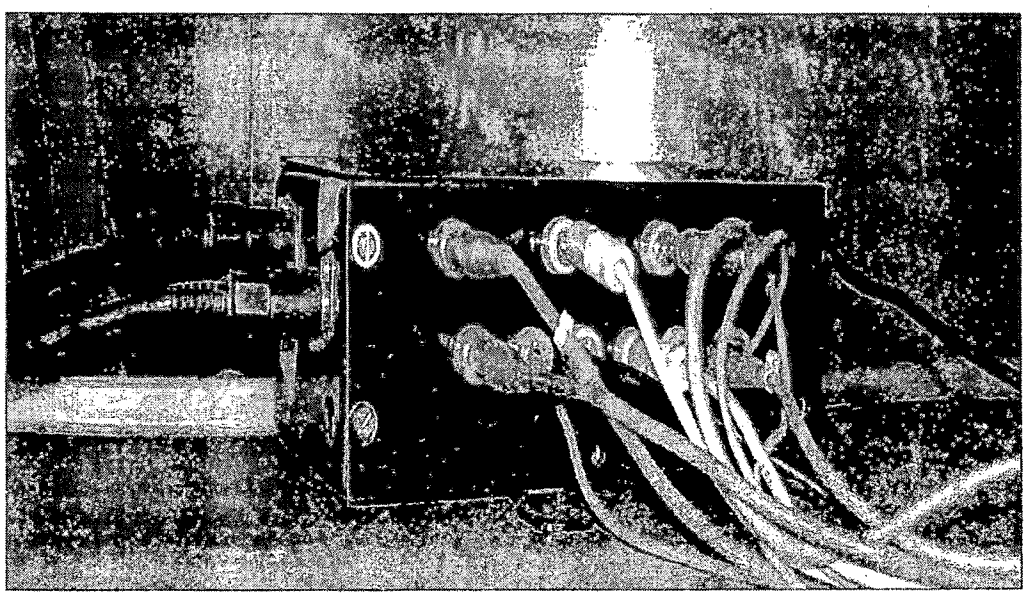

Fig. 6.2.1-4 Box for P.T and C.T

6.2.2 Schematic of Multiprocessor System

The circuit for the DSP board was to be designed with an expansion for the multiprocessor system. The flash memory should be sufficient present on the board for program and RAM memory for processing of data. At the same time the processor should have an expansion capacity and able to interact with other processor for real time acquiring of data and processing of various power quality parameters.

The schematic for the DSP board is designed in such manner so that it can be expanded and ale to accommodate any algorithm for processing of power quality parameters. The circuit for the same is as shown in Fig.6.2.2-1. The circuit is build across TMS320F280 core, with four SPI interface and 1 MB of EEPROM on I2C interface. The signals of two

inbuilt analog to digital converter are pulled out on two connectors, where three voltage and current signals are connected. The circuit also includes Real Time Clock (RTC) for time stamping of data, so as to synchronize the data used by master card. All clocks are synchronized by the master card at interval of 1ms. A JTAG interface is also included on-board for real time debugging and execution of program.

In order to use the card for master interface, an RS232 circuit is included on-board. The circuit uses MAX232 which is capable to drive at 3.3V supply, so a single card can be used for multiple processes and can be used to evaluate various power quality measurement algorithms. In this card RS232 pot is used for loading the program and is also used by master card for communicating with PC using the VB software.

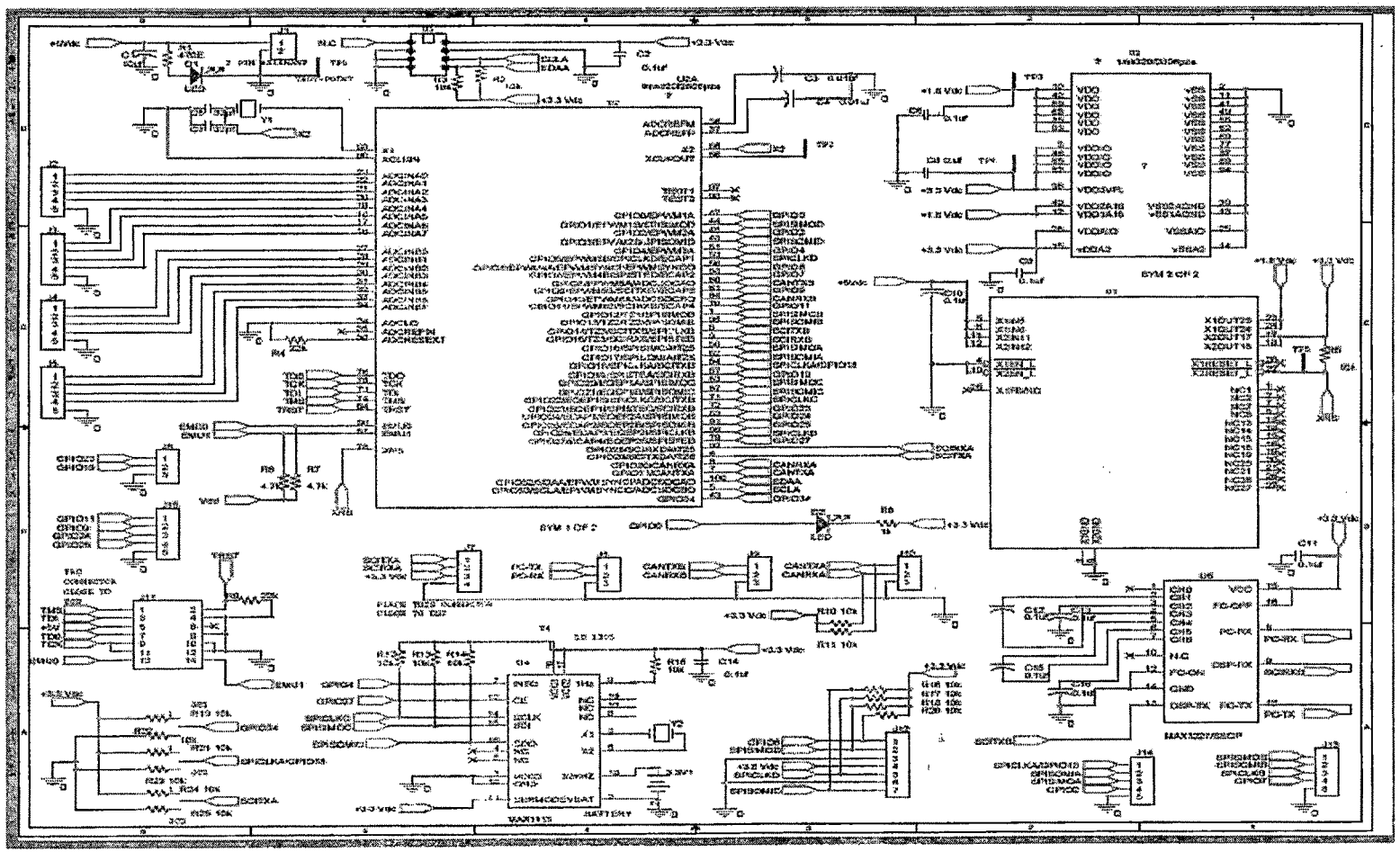

Fig. 6.2.2-1 Schematic for DSP board

The photograph of a single DSP card is as shown in the Fig.6.2.2-2. As shown in the board contains a single DSP core and peripherals are expanded out for communication with carious other cards. All the components used in this card are SMD 1206 in order to reduce the size and complexity of the card. The full card is developed in-house except the artwork and PCB fabrication.

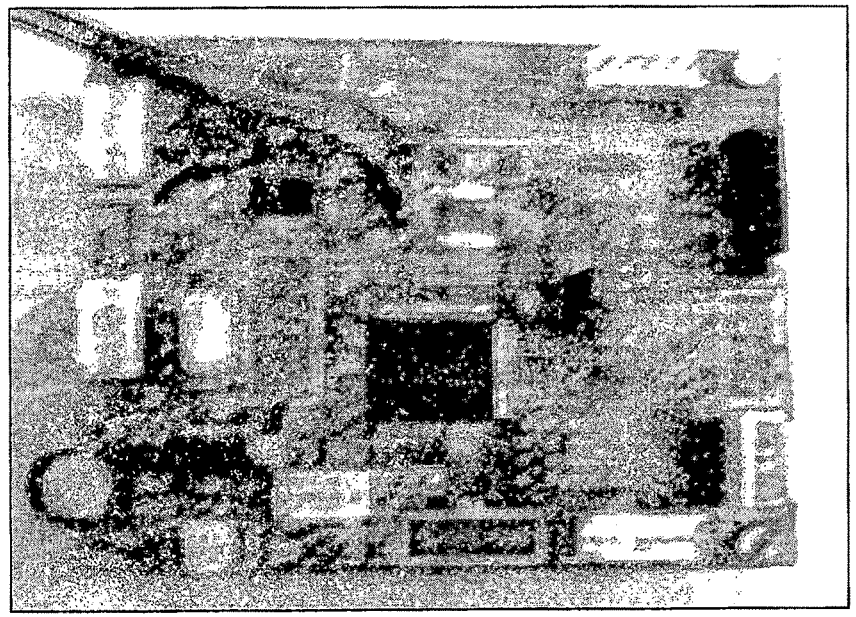

Fig. 6.2.2-2 Photograph of DSP board

6.2.3 Design of Multiprocessor System

The design of the multiprocessor system is planned in order to meet the real time criteria of implementing multitasking and performing calculations for multiple power quality parameters at the same time. Since the power quality parameters are dynamic and the calculation of each parameter depends on the algorithm used. Also the sampling rate at which voltage and current channels are sampled also pays a major role in performing calculations.

Hence the task of multitasking can be accomplish can be fulfill either by using multiple ADC and multiple processor, or multiple processor with in-built ADC. Since the second approach is cost-effective and reduces the complexity was chosen for this project. So, TMS320F2806 DSP with in-built ADC was chosen and a multiprocessor system was design as show in Fig.6.2.3-1. In this case all the cards are identical hardware wise and each executes a separate algorithm. Each card samples 3-phase voltage and current channels at a different rate and execute the specific algorithm loaded in the flash memory. Each card calculated the power quality parameter and store it in a circular buffer provided on board. The master card fetches the data from the circular buffer and transfers the data to the PC. Since all the four processor runs at 150MHz real time calculation of various power quality parameters is achieved.

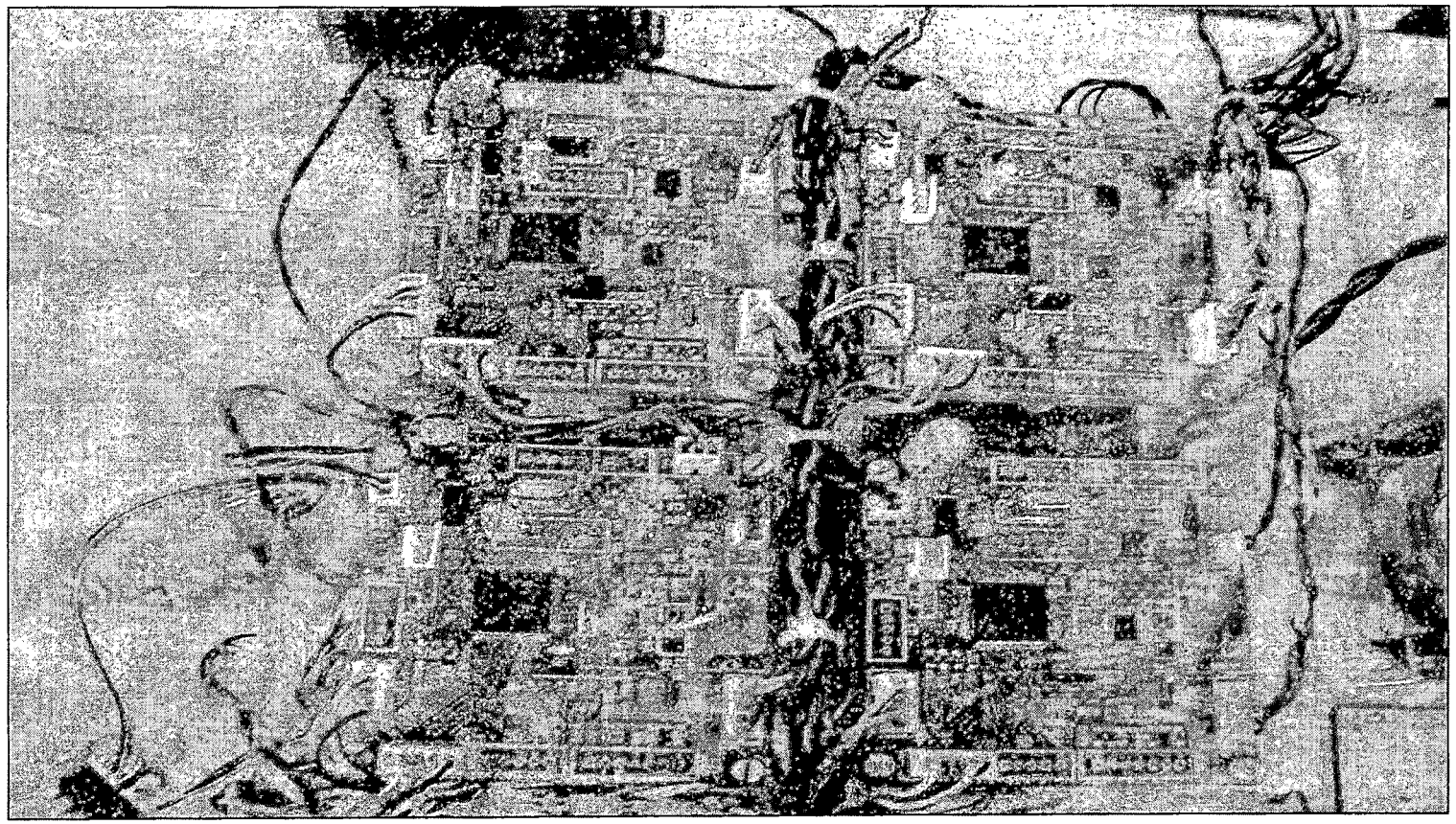

Fig. 6.2.3-1 Photograph of Multiprocessor cards

The output of the signal conditional circuit generates a three phase voltage and current signals in unipolar form. These unipolar signals are connected to each DSP card as shown in the Fig.6.2.3-1 To each card there are five connectors connected. The two five pins connectors are r,y,b voltage signals and grounds and similarly the other connector for current. The two pin connector is for power and control command from the master DSP card. The last five pin connector is for communication with each other i.e SPI interface. Hardware wise all the four cards are identical; any card can be used for computation of any power quality parameter. In this project card-1 is used continuous measurement of frequency, card-2 is for on-line tracking of harmonics, card-3 is for 4-quadrant power measurement and card-4 is for flicker measurement. The system is restricted to measure only these power quality parameters, however later the system can be expanded to measure further parameters.

In order to reduce the cost the cards are connected to each other through wires, this can be replaced in future with a back-plane card for interconnecting all the cards. The analog signal conditioning card is placed at the bottom and on the top of the cards are the four DSP cards.

In order to communicate with all the four card a master processor is required which can communicate with all the four DSP boards and communicate with PC for transfer of data from the PC to all the four cards and vice versa.

As shown in Fig. 6.2.3-2 with all the four cards and a master card at the top of all the four DSP cards. The master card hardware is same as all the four slave cards only the software is changed. As an additional

feature the master card also samples the three voltage and current channels and display on the PC.

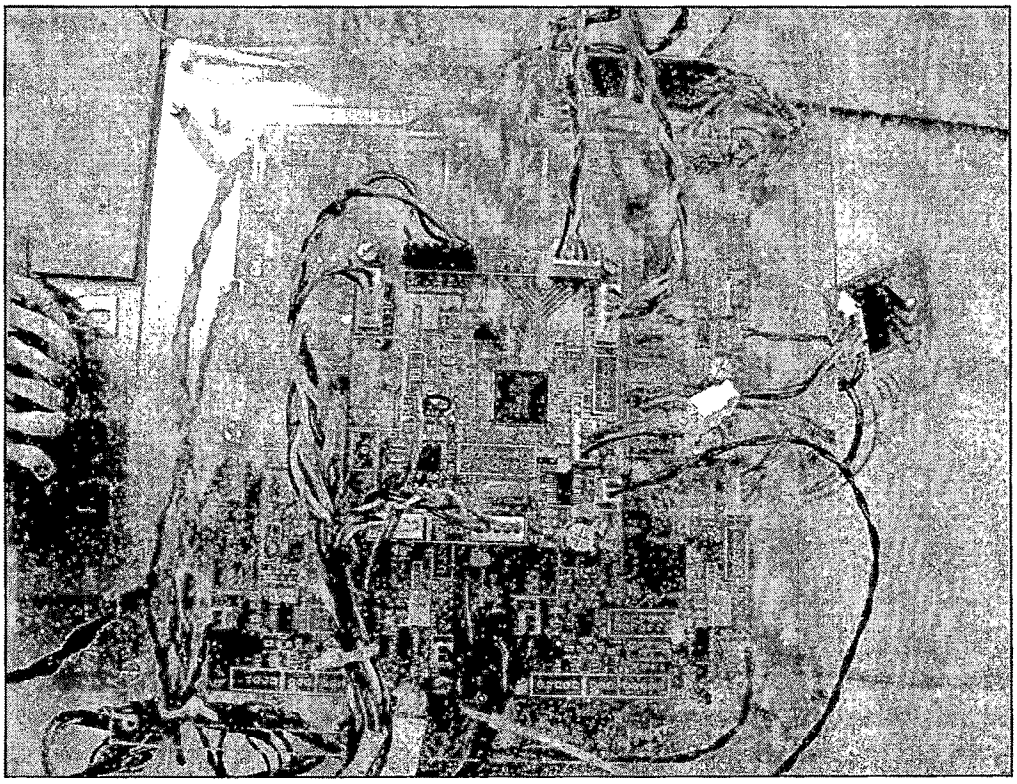

Fig. 6.2.3-2 Final photograph of the multiprocessor system

The main advantage of using the TMS320F2806 DSP is that the DSP have four SPI interface as a result all the four SPI of the master DSP are connected to the four SPI slave channels as shown in the Fig.6.2.3-2. Also the voltage and current channels are connected to con 2 and con 3 and the con3 for power supply. A fifth connector is placed for master control on all the five slave cards, using the master control the master DSP can generate a high priority to any of the slave card and request for data.

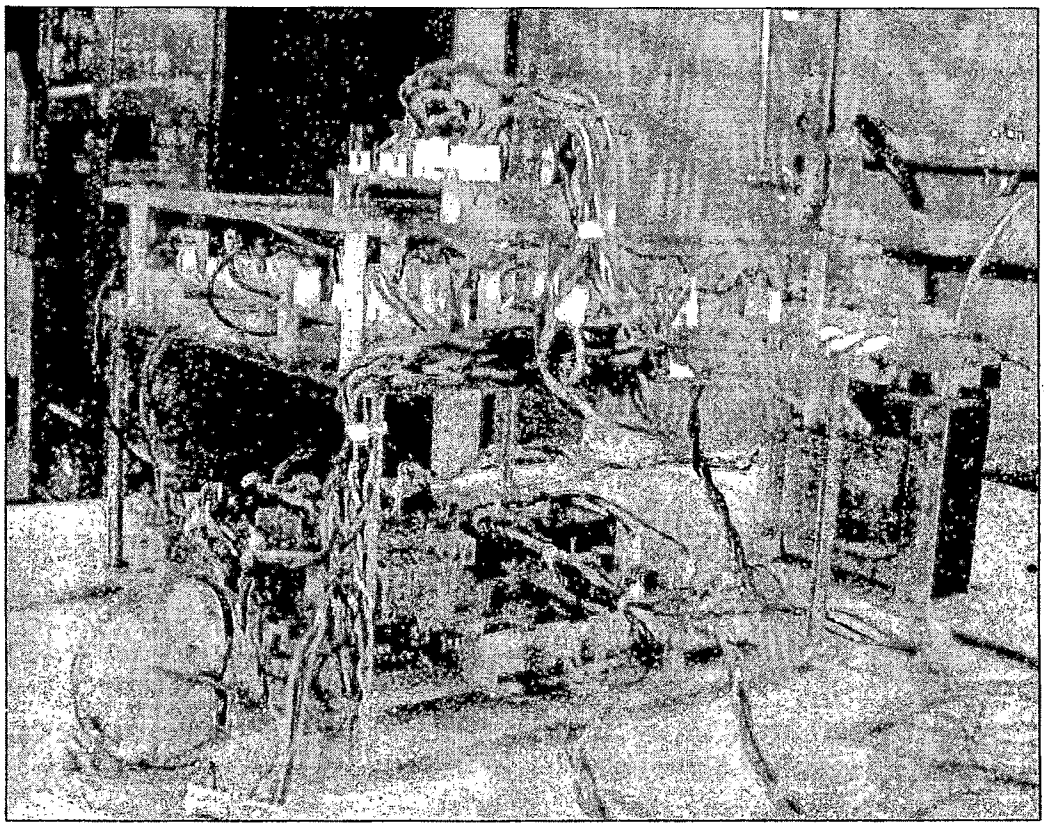

Fig. 6.2.3-3 Test set-up of the complete system

As shown in the Fig 6.2.3-3 it can be seem the analog signal conditioning circuit at the bottom, four DSP slave boards on the top and at the top-most is the master DSP. A separate transformer 240/9-0-9 is used to power all the cards through a power supply circuit.

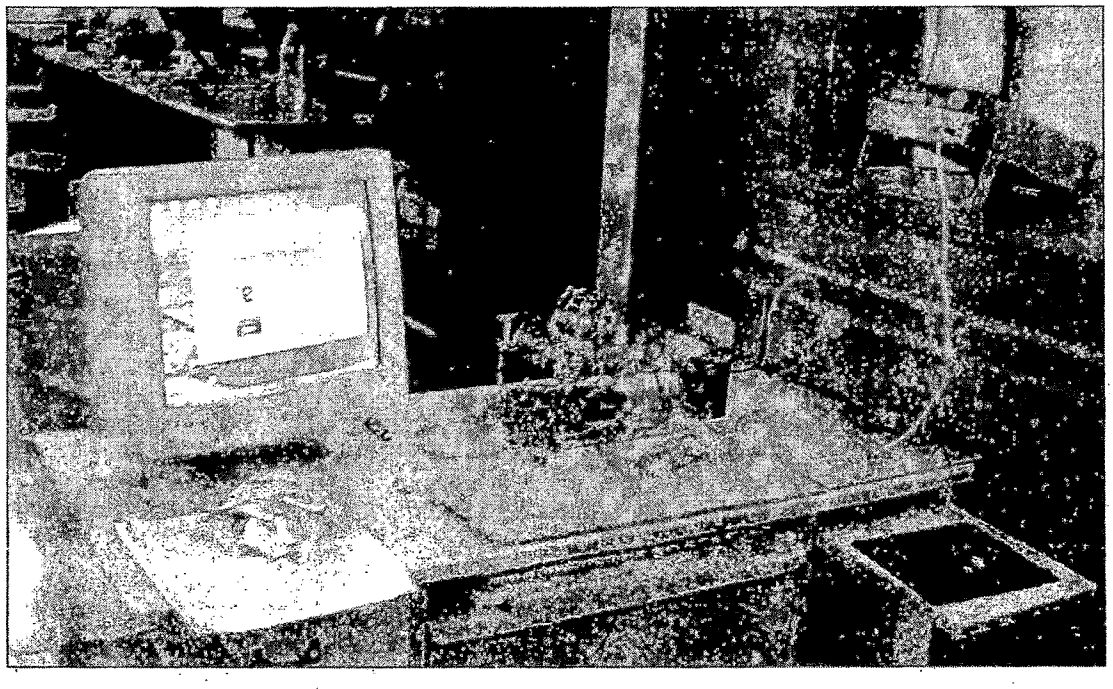

Fig. 6.2.3-4 Multiprocessor system with PC interface

As shown in the Fig 6.2.3-4 the complete development set-up taken during the development phase of the firmware. All the firmware were developed in-house and were tested using single phase and three phase source.

6.2.4 Real time Digital Signal Acquisition

DSP's deliver high performance provided the software running on the processor facilitates such performance. Programming with DSP's presents some unique issues because of the specialized architecture of the DSP's, and the nature of applications. In real-time applications, the best approach is to use a judicious mixture of high-level language (HLL) and assembly [8]. HLL code is used for initialization and non real-time

code [9]. Time-critical tasks are coded in assembly the framework for the power quality testing application was developed using C and the real-time data-collection, data analysis, and communication tasks were coded in assembly. The basic environment for processing is provided by the real-time processing (RTP) kernel [10]. The kernel provides a mixed environment, and supports multitasking to handle the tasks associated with data collection, data analysis, and communication.

A. Real-Time Tasks

The four fundamental tasks to be accomplished in real-time are as follows.

1) ***Data Acquisition:*** Samples of the test signal are acquired from the A/D converter which has a resolution of 0.1 mV. The timer interrupt rate is set such that approximately 64 samples are acquired in a 50 Hz cycle.

2) ***Data Buffering:*** A double buffer is implemented to manage real-time data. After acquisition of the sample the sample is processed in the mathematical equaltion so that before the next sample begins it compute the respective parameter.

3) ***Data Analysis:*** The master DSP captures the data from the slave DSP at an interval of one second and display the same on the PC.

5) ***Communication:*** In this thesis a propriety protocol is used for communication from the master PC to the DSP board. The protocol used in the thesis is described below and is common to all the cards used for measurement of PQ parameters.

Start Command	Source Add	Command	Data Length	Data	CRC	End Command
0x02	0x10 To 0x15	0x11 To 0x55				0x03

The address for each card is different to identify the source of the data, The command represent the purpose of sending the frame and is decoded in the software accordingly. The Data length represents the total length of the data and all the data is represented in ASCII format. The CRC is the summation of source address + command + data length + data and is verified both at the transmitter and the receiver end to validate the crash or receive of the frame.

Because the major task of the presented PQ monitor is to process various power quality parameters in real-time, significant optimization efforts have been taken when programming the DSP, in order to reduce the algorithm computation time.

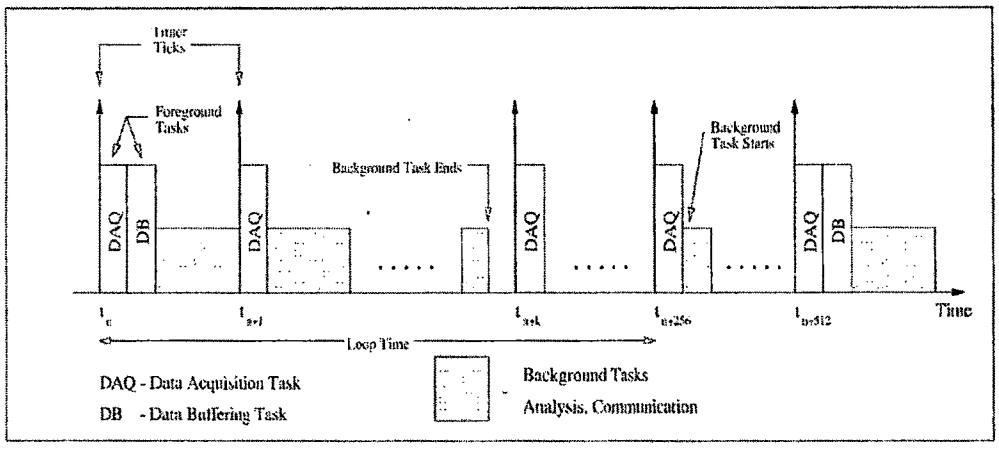

Fig. 6.2.4-1 Real time timing window

B. Real-Time Monitoring Capability

The classification process of window in each of the DSP board is mainly dependent on the execution time taken by the ADC. Since in all the DSP board the ADC used is common the error due to sampling constraints does not affect the performance of the algorithm. The time taken for execution of the algorithm varies in each of the DSP board. Each DSP board process the voltage signals and after processing the algoritm gives an interrupt command to the master DSP. The data is stored in a circular buffer so the master DSP fetches the data, while the slave DSP executes the algorithm and continue the process.

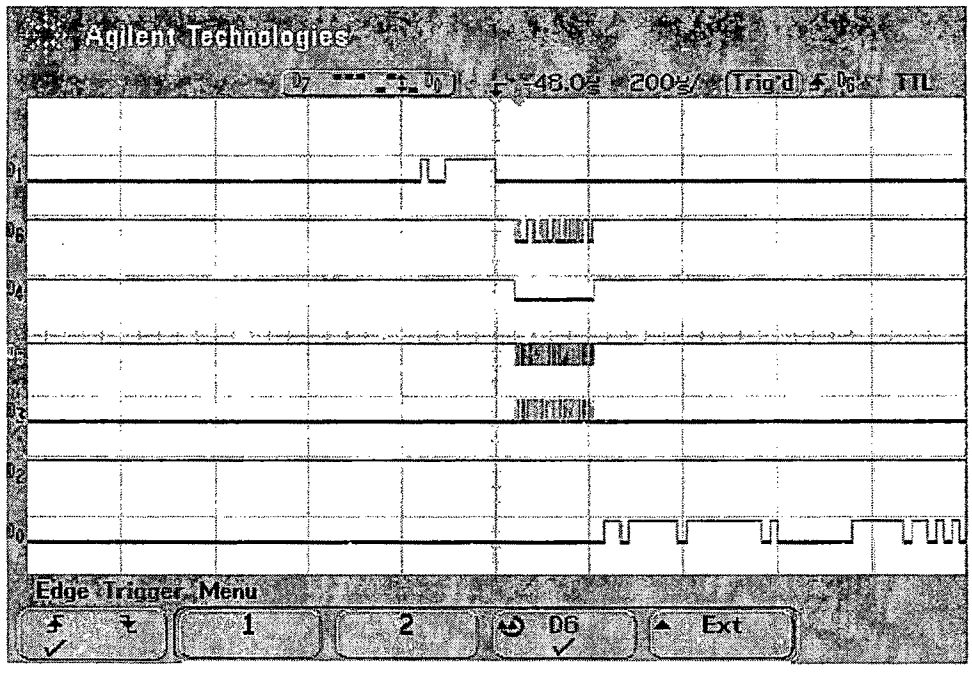

Fig. 6.2.4-2 Data transfer from slave to master and vice versa

As shown in the Fig 6.2.4-2 the D_1 is the request from the master to the slave, D_4 is the acknowledge from the slave to the Master, D_5 is the SCLK, D_6 is the data from the slave to the Master, D_5 is the data from the master to the slave. The entire transfer of data from the master to slave is completed in 172 μs.

As shown in the Fig 6.2.4-3, the zoomed version of data transfer from the master to the slave. As can be seen from the the master transfer the data to the slave at the rising edge and the slave transfer the data ot the master at the falling clock of the clock pulse D_4 in this case.

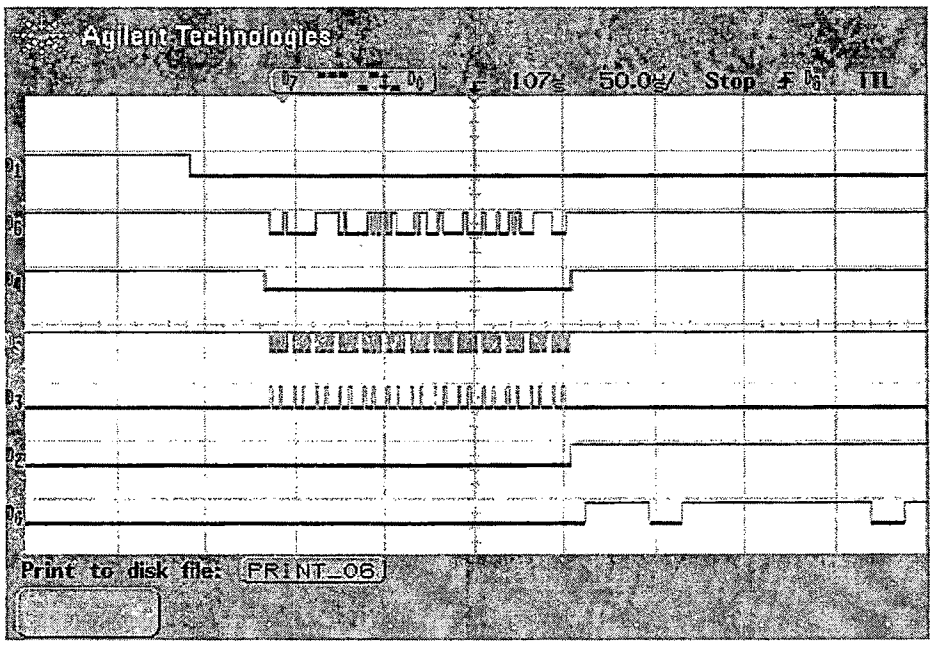

Fig. 6.2.4-3 Waveform zoomed for data transfer

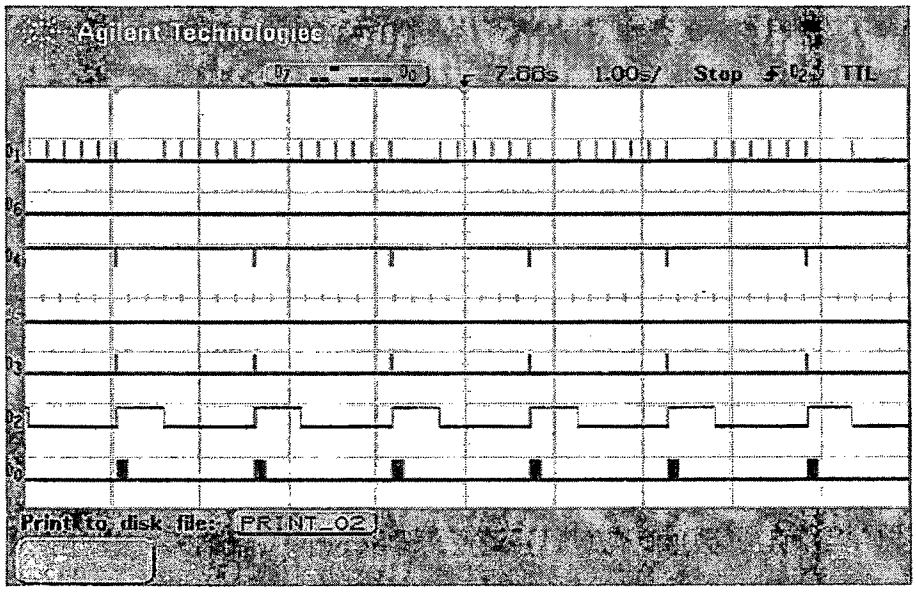

Fig. 6.2.4-4 Real time flow of data

As shown in the Fig 6.2.4-4 there is continuous flow of data from the slave to master and vice versa among the slave and master cards. As shown in fig 6.2.4-4 the resolution of 1second is achieved due to real time buffer technique along with the multiprocessor technique employed in deploying these applications.

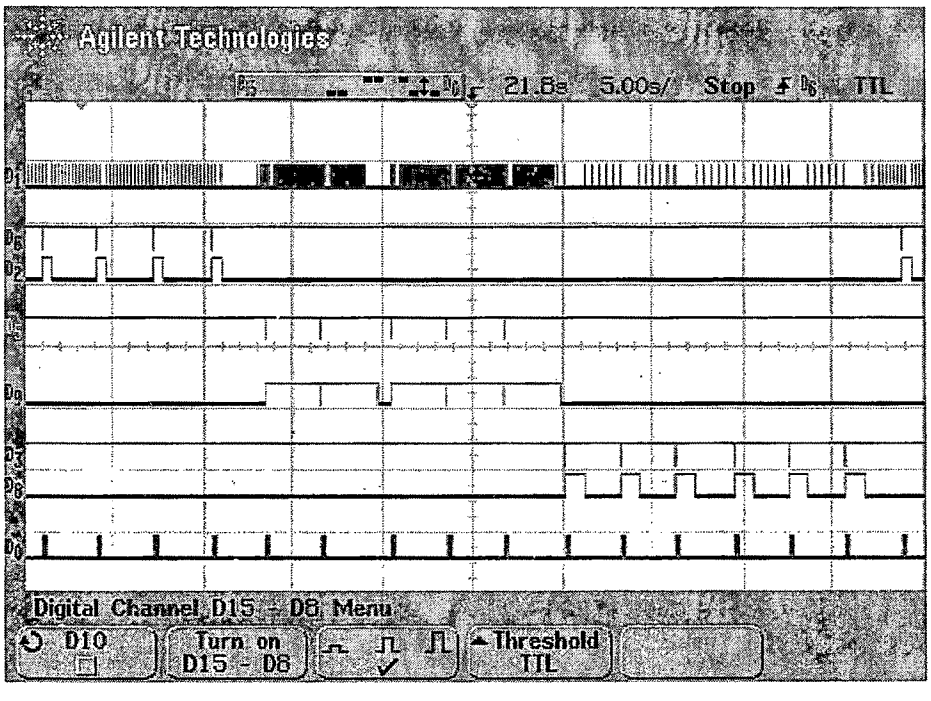

Fig. 6.2.4-5 Data transfer from three slave DSP to master DSP

As shown in the Fig 6.2.4-2 the real time data flow between the master and the slave devices. The above waveforms are captured using Agilent Oscilloscope 200Mhz digital analyzer. The data transfer from the Master DSP card to the other three DSP slave cards. As described earlier the three DSP cards perform the power measurement, frequency measurement and harmonic measurement data. The master DSP request each slave card and the slave cards transfer the data to the DSP board. D_0 represent the SCLK, D_2 represent the response from the slave and D_6 represent the data transfer from the slave to the master.

6.2.5 Design of PC Based Software

Visual Basic (VB) based software is developed for capturing and display of information from the multiprocessor hardware to the user. A screen view of the various modules developed for power, harmonic, frequency, flicker and waveform is as shown in Fig 6.2.5-1 to 6.2.5-4.

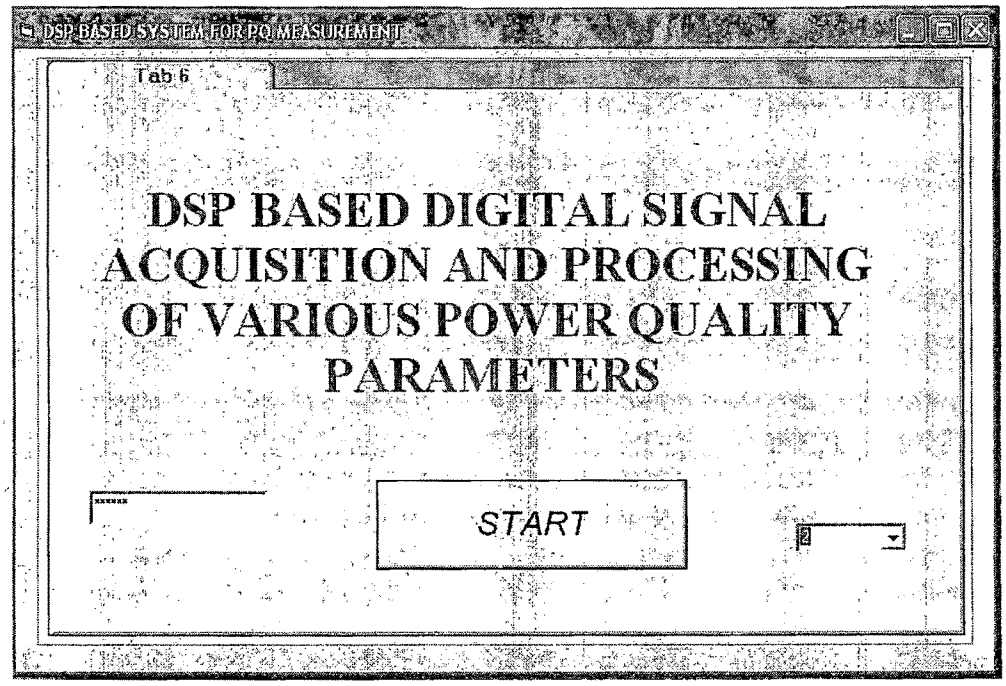

Fig. 6.2.5-1 Screen Shot of the main window

As shown in Fig 6.2.5-1, the initial screen of the VB based software for capturing the data.

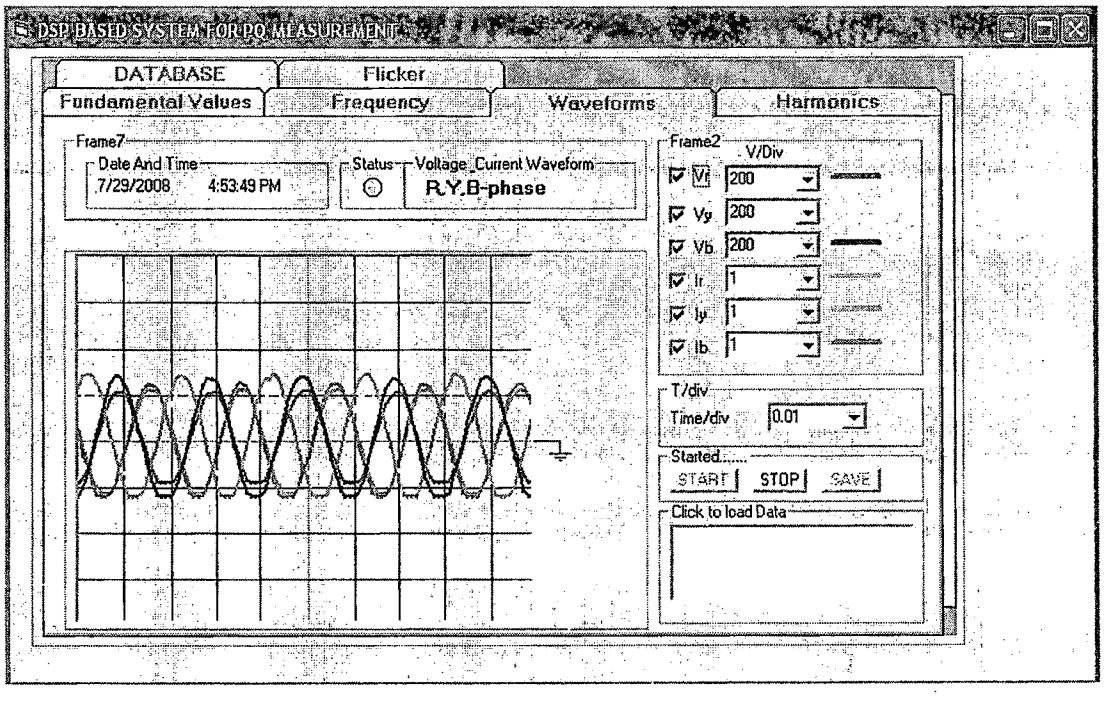

Fig. 6.2.5-2 Screen Shot of the waveform data

As shown in Fig 6.2.5-2, the three phase voltage and current waveforms screen of the VB based software for capturing the data.

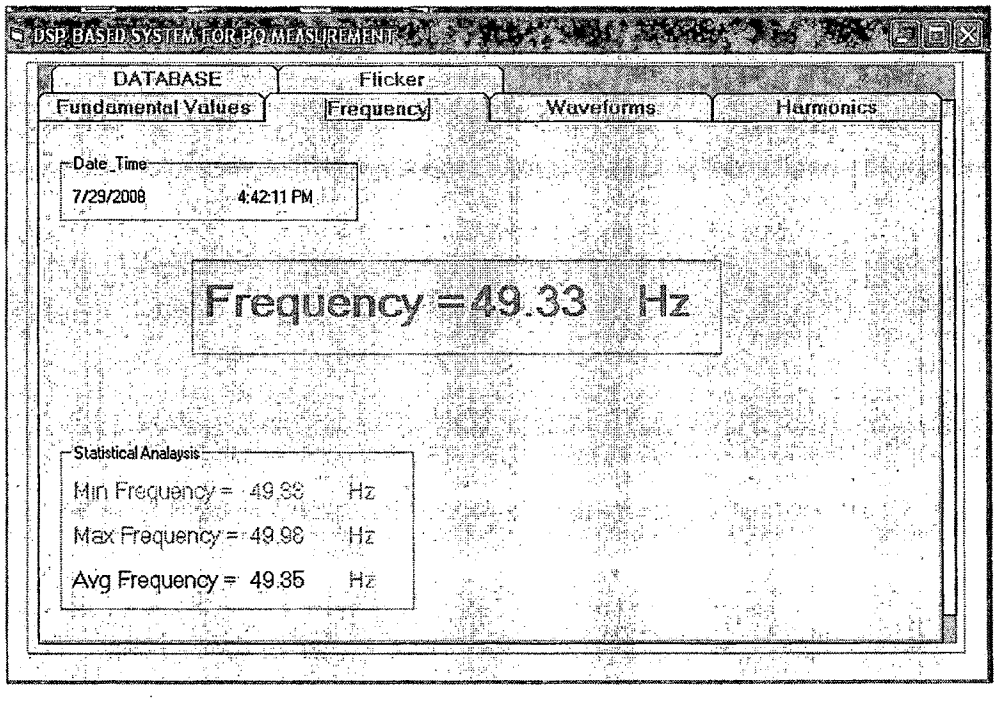

Fig. 6.2.5-3 Screen shot of the frequency data

As shown in Fig 6.2.5-3, the frequency data captured and displayed on VB based software.

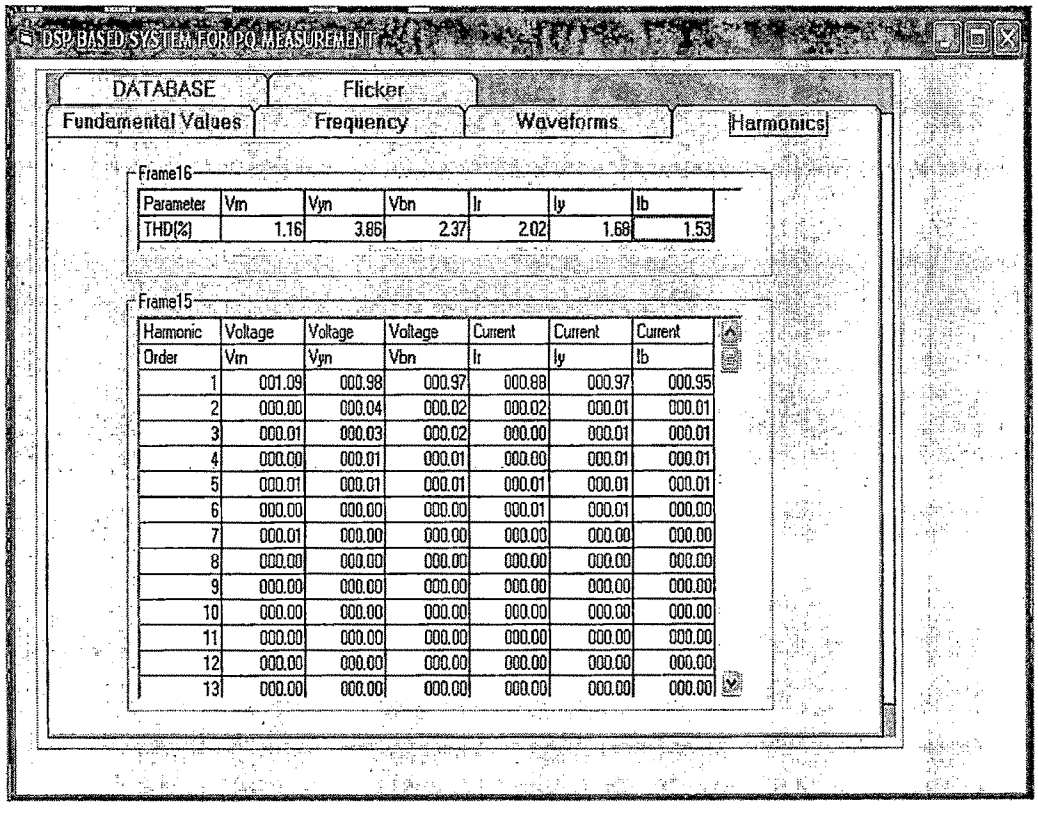

Fig. 6.2.5-4 Screen Shot of the Harmonic data

As shown in Fig 6.2.5-4, the harmonic data captured and displayed on VB based software.

6.3 Software Development for Real Time Measurement of PQ parameters

A complete high level design of the complete architectures as shown in Fig 6.3-1. The flowchart displays the various functions of the cards in brief and the detailed function are already covered in respective chapters.

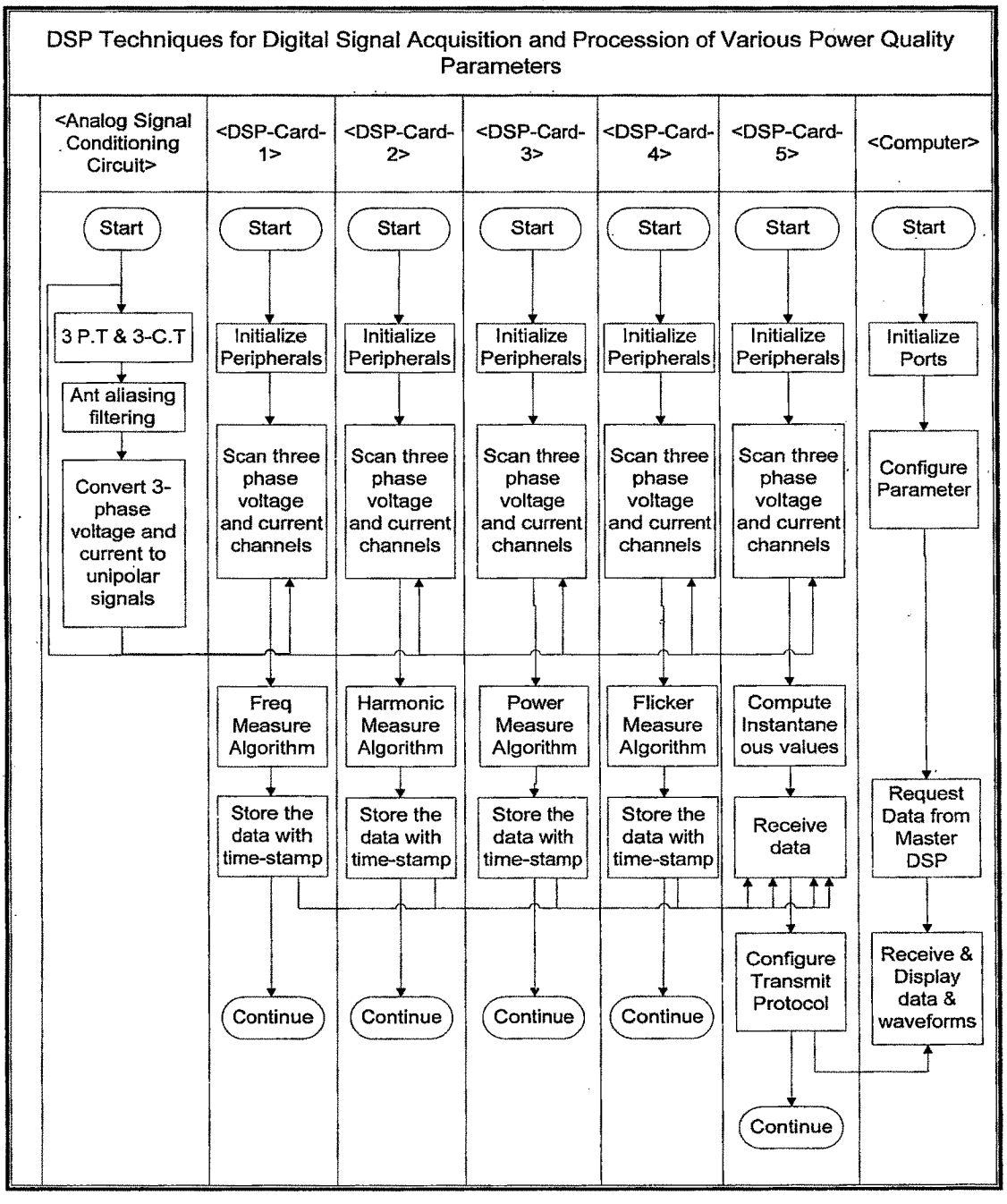

Fig. 6.3-1 Flowchart of Multiprocessor System

It can be seen that each card has been given a particular task in a predefined time interval, as a result the complete system is able to perform the task in real-time. Since the task given to each card varies the computation time is varied. Frequency, power and harmonics are calculated sample by sample but at different sampling frequency and flicker is calculated at interval of 10 min. Due to variation in the timing and in order to achieve real time performance, multiprocessor architecture is proposed using DSP to achieve the desired performance. It can be seen from the Fig 6.3-1 that if a multiprocessor system would not have been implemented then real time execution of various power quality parameters could not have been completed.

6.4 Interfacing of Multiprocessor system with PC

The multiprocessor system designed for real time measurement of various power quality parameters needs to be interface to a PC using a user interactive software for display of various power quality information useful to user. In order to achieve this master DSP card communicates with the PC using an RS232 interface. The communication setting is provided on the VB software and is as shown in the Fig. 6.4-1 . Once the communication is set-up the PC based software acts as a master and requests the master DSP card to send the information.

As shown in Fig 6.4-1 the VB software runs on a laptop and interface with the multiprocessor with USB/232 converter. The three phase voltage and current signals is given through three-phase variac and given to the hardware through voltage and current transducers.

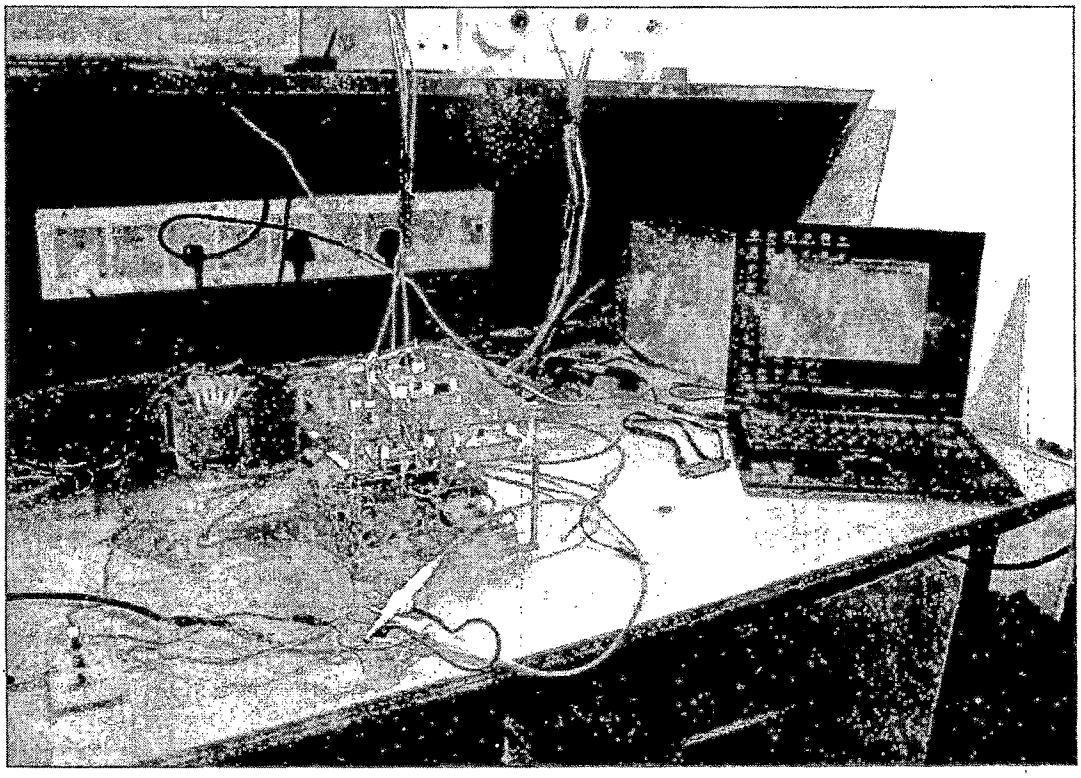

Fig. 6.4-1 Multiprocessor System with PC interface

6.5 .Conclusions:

This chapter covers the use of multiprocessor based architecture for continuous measurement of power quality parameter such as voltage, current, frequency, power, harmonics and flicker. The chapter also describes feasibility to capture data in real time and display on VB based software. Both the algorithm and the DSP make the real time data available to the user. The size of the hardware can be reduced further for commercial application of the proposed system.