# "CURRENT AND VOLTAGE CONTROL OF SINGLE-STAGE VOLTAGE SOURCE INVERTER FOR PHOTOVOLTIC SYSTEM"



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# DEPARTMENT OF ELECTRICAL ENGINEERING FACULTY OF TECHNOLOGY AND ENGINEERING THE MAHARAJA SAYAJIRAO UNIVERSITY OF BARODA, VADODARA MARCH 2022

# "CURRENT AND VOLTAGE CONTROL OF SINGLE-STAGE VOLTAGE SOURCE INVERTER FOR PHOTOVOLTIC SYSTEM"

A thesis submitted for the award of

Degree of

## **DOCTOR OF PHILOSOPHY**

in

## **Electrical Engineering**

By

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# DEPARTMENT OF ELECTRICAL ENGINEERING FACULTY OF TECHNOLOGY AND ENGINEERING THE MAHARAJA SAYAJIRAO UNIVERSITY OF BARODA, VADODARA MARCH 2022

## **CERTIFICATE OF GUIDE**

This is to certify that the thesis entitled "**Current and Voltage Control of Single-stage Voltage Source Inverter for Photovoltaic System**" submitted by Bhavik Arvindbhai Brahmbhatt in fulfillment of the degree of DOCTOR OF PHILOSOPHY in Electrical Engineering Department, Faculty of Technology & Engineering, The Maharaja Sayajirao University of Baroda, Vadodara is a bonafide record of investigations carried out by her under my guidance and supervision. In my opinion the standard fulfilling the requirements of the Ph.D. Degree as prescribed in the regulations of the University has been attained.

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## DECLARATION

I, Bhavik Arvindbhai Brahmbhatt declares that the thesis entitled "**Current and Voltage control of Single-stage voltage source inverter for photovoltaic system**" submitted by me for the degree of Doctor of Philosophy is the record of research work carried out by me during the period from 2014 to 2022 under the supervision of my guide Dr. Hina B. Chandwani. This work has not formed the basis for the award of any degree, diploma, associateship, and fellowship, titles in this or any other University or other institution of higher learning.

I further declare that the material obtained from other sources have been duly acknowledged in the thesis. I shall be solely responsible for any plagiarism or other irregularities, if noticed in the thesis.

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Date:	•••	•••	•••	•••	•••	••	••	
Place:						•••		

**DEDICATED TO MY FAMILY** 

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## ABSTRACT

The main aim of the thesis is to investigate the current and voltage control of Single-stage grid-tied voltage source inverter for photovoltaic system. To make low-voltage power generation flow bidirectional, Photovoltaic (PV) systems may be simply incorporated into residential infrastructures. This thesis emphases on a real and reactive power flow management in a single-stage photovoltaic system (PV) by performing various mode of operation such as active power injection, voltage regulation at point of common coupling(PCC), and power factor correction(PFC) at grid side. Grid-tied system needs the phase-locked loop (PLL) to synchronize converter operation with grid voltage, which has an impact on converter stability and performance. Synchronous Reference Frame-PLL (SRF-PLL) is a common grid synchronization technology since it is simple and reliable. To avoid fundamental frequency and phase oscillations, the SRF-PLL must include a DC offset suppression feature. The bandwidth of an irregular grid should be decreased to enable sufficient disturbance rejection without losing detection speed. The pre/in-loop filter was added to modern PLLs in order to improve phase-angle estimation speed and accuracy. It is critical that PLLs have the ability to increase dynamic responsiveness and shorten settlement time without sacrificing system stability or the ability to remove disturbances. The widely accepted phase-locked loop (PLL) algorithm has a complex architecture and requires a tedious tuning process to obtain a good stability margin. The SOGI-FLL (second-order generalized integrator-based frequency locked loop) was the most effective of the several control approaches tested. Even in the presence of harmonics, voltage changes, frequency fluctuations, and the like, it accurately monitors the grid voltage frequency. Dual-second order generalized integrator-based frequency-locked loop (DSOGI-FLL) is proven to have the most promising performance by eliminating both the negative and harmonic distorted components under nonideal grid voltage conditions. Moreover, even in the absence of any PI controller, when the grid voltage has characteristics such as dips, swells, harmonics, unbalance, and frequency changes, it can accurately track the frequency of the grid voltage Low-frequency oscillations are included into the frequency calculation in the case of a DC offset. Grid voltage anomalies of various kinds are addressed in this thesis, including DC offsets, using a modified dual second-order generalized integrator frequency-locked loop (MDSOGI-FLL). MDSOGI-FLL is employed using one of the approaches from this two different methods described in this thesis. The first approach is to eliminate DC offset by inserting an IIR-based DC blocker in each sensed signal from ADCs prior to the DSOGI-FLL/DDSRF-PLL. The second method is to modify the structure of DSOGI-FLL by adding a third integrator. The MSOGI-FLL is implemented by utilizing waijung block-set of Simulink/MATLAB and tested its performance in the presence of grid voltage anomalies. Experimental results validated that MDSOGI-FLL performs better during grid voltage anomalies. The term "multipurpose PV system" refers to an inverter that is capable of more than just producing electricity. For the reactive power compensation, this thesis presents an innovative control approach in multipurpose single-stage PV system for the PV inverter. There are three different modes of operation that may be achieved in multipurpose single-stage PV system control: Fully active power injection (PV mode), active power injection with reactive power support mode (Partial PV and Partial STATCOM); and fully reactive power support mode (Full STATCOM) depending on system requirements. In a daytime, the modified control approach in multi-purpose PV system can be utilized as Distributed generating station and partial STATCOM by providing active power injection and maintain unity power factor at grid side respectively. In a night time and also at critical day time, it can be operated as fully STATCOM. To maintain DC-bus voltage in a single-stage PV system, the voltage controller has to track the reference voltage provided by the MPPT algorithm using feedback linearization approach is presented. In this paper, Modified dual-Second order generalized integrator (MDSOGI) technique is used for grid synchronization to estimate precise phase-angle of grid during non-ideal grid conditions while DC-current sensor less MPPT algorithm is used for MPP tracking in control of single -stage grid tied PV inverter. One new number for MPPT for single-stage grid connected PV system without a DC current sensor is presented in this thesis. The PV current quantity( which is sensed by DC current sensor) is replaced with a new quantity, which is the d-axis current component of inner current control loop. This modified MPPT has presented a theoretical and implementation. The dynamic performance of presented control approach is proof evaluated based on simulation results obtained using a simulink/MATLAB environment and experimental results obtained from laboratory setup to confirm desired performance of presented control algorithm for single stage grid tied PV inverter during a different mode of operation.

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# LIST OF ABBREVIATION

DG	Distributed Generations
SCs	Shunt Capacitor Banks
OLTCs	On Load Tap Changer
SVR	Step Type Regulator
SVC	Static VAR Compensator
STATCOM	Static Synchronous Compensator
VSI	Voltage Source Inverter
VSC	Voltage Source Converter
PV	Photovoltaic
SOG	Second Ordered Generalized Integrator
SRF	Synchronous Reference Frame
DSRF	Double Synchronous Reference Frame
DDSRF	Decouple Double Synchronous Reference Frame
DSOGI	Dual Second Ordered Generalized Integrator
FLL	Frequency Lock Loop
PLL	Phase Lock Loop
TOV	Transient Over Voltage
PCC	Point Of Common Coupling

## CHAPTER 1 INTRODUCTION

Renewable energy has seen a spike in popularity in latest decades of environmental concerns about pollution and the finite supply of fossil fuels. Among the world's leading renewable energy sources, the photovoltaic system (PV) turns solar power into electricity. In the 1960s, the space programed adopted PV as a cost-effective power supply. Stand-alone PV power plants were widely used in rural and remote locations in the 1980s and 1990s as an attractive and cost-effective option for supplying electricity [1]. The solar energy sector has grown rapidly during the past two decades due to substantial advances in power electronics and solar panels. PV electricity generation costs are predicted to fall as a result of this growth. Since solar panel prices have fallen dramatically, the number of PV installations has increased significantly. The installed capacity of renewable energy for electricity generation in India reached 911.53 GW at the end of 2021, compared to 138.9 GW in 2014[2].India will have a total solar power generation capacity of 383 GW by 2020-21. Upwards of 42 GW of solar capacity has been installed in India in the previous seven years, an increase of more than 700%.

Rooftop and ground-mounted PV systems are available in a wide range of capacities, from a few kilowatts to hundreds of megawatts, depending on their location. On either hand, ground-mounted photovoltaic systems are installed on the ground while roof-type systems are installed on the roofs of institutional buildings, residential, or commercial. Both grid-connected and stand-alone solar power systems can be installed with on-grid/off-grid PV system. In the case of a grid-connected PV system, excess power generated by the PV system can be fed back into the grid [2]. PV systems can be categorized based on their power capacity from a small-scale to a utility. Between 1 MW and 10 MW, utility-scale PV is connected through one or more interconnection transformers to medium-voltage distribution feeders, such as the 27.6 kV feeders. PV systems [2]. They can be installed on both small and large buildings. Depending on the size of the PV system, medium or low voltage distribution feeders are used. Up to ten kilowatts is considered a small-scale PV system.

# 1.1 Electricity Generation through Distributed Generation (DG) System

The electric power system relies heavily on the distribution system to ensure that customers receive a steady supply of electricity[4]. As a result, poor power quality in the distribution system has a serious influence on other components of the power system, such as loads. This implies that the loss of any one component in the supply line causes the power supply to be cut off to the end customers in most distribution systems. Distributed Generation (DG) has become increasingly popular in recent years for a variety of reasons, including increased demand, technological and economic advancements, and environmental concerns [6]. IEEE defines DG as "the generation of electricity by facilities that are sufficiently smaller than central generating plants to allow interconnection at practically any point in a power system" [2-3][6]. In recent years, wind and solar energy-based DGs have emerged as the most popular.

## 1.2 Grid-Integration Challenges for Photovoltaic Systems

By using DGs, transmission network expansion will be less expensive. As a result of these advantages, new distribution system challenges have arisen. Harmonics, flickering voltage, and Temporary overvoltage (TOV) are some of the problems associated with utility[4][18]. The power of PV systems can rapidly fluctuate due to diverse sunlight availability and climatic circumstances (for example, the movement of clouds). It will degrade the dynamic and steady state behavior of system. As a result of the PV system's increased use of voltage regulators including load tap changers and capacitor banks, voltage profile alterations such as temporary overvoltage (TOV) and steady state overvoltage have been observed. Large PV systems connected to the grid, on the other hand, generated power flow in the opposite way, resulting in excess voltages at PCC, which could limit future DG installations [7][10-11]. Utilities mandate that PV systems adhere to IEEE Standard 1547, IEC 61727, and Standard 929-2000 in order to avoid any of these issues [14]. Traditionally, electricity distributors employed capacitor switching and under load tap changers to regulate voltage, but these devices failed in the presence of solar power systems and significant load changes. Overvoltage occurs at PCC when a solar

power system is integrated to the grid. This overvoltage is called steady-state overvoltage[14][18]. If these are higher than the electricity distribution companies' interconnection regulations, the solar power system is denied connection.

## 1.3 Shunt-connected Static Reactive Power Compensator (STATCOM)

Voltage regulation has become an essential issue in the integration of DG resources such as PV solar power systems since they may have a negative impact on voltage levels[4]. Voltage regulation in distribution systems has traditionally relied on the use of shunt capacitor banks (SCs), on-load tap changes (OLTCs), and step type regulators (SVRs). These devices, on the other hand, operate on the basis of unidirectional power flow and typical load changes. Traditional voltage regulators are unable to work properly because solar and wind power systems can generate reverse power flows. Controllers known as FACTS (Flexible AC Transmission Systems) can be used to overcome the limitations of electromechanically controlled transmission systems. With the development of the shunt connected static compensator (STATCOM)[35], controlled reactors and switched capacitors were replaced by the voltage source inverter (VSI). For example, STATCOMs have several advantages over conventional SVCs since they use self-commutated power semiconductor devices such as GTO, IGBT and so on. This is unlike variable impedance type SVC which uses thyristor devices. Traditionally, distribution systems use shunt capacitor banks, on-load tap changers, and step voltage regulators (SVRs)[37]. But these devices work with unidirectional power flow and usual load changes. Due to potential of reverse power flows from solar and wind power systems, typical voltage regulators fail. To manage the voltage, Flexible AC Transmission Systems (FACTS) devices such as Static Var Compensator (SVC) [36-38] or Static synchronous Compensator (STATCOM) [102] exchange reactive power at the feeder where solar power systems are attached. To compensate for reactive power loss, the STATCOM system utilizes a DC-bus capacitor, solid state switches, filter components and an interfacing transformer. In addition to power factor correction, the STATCOM can manage voltage flicker and transient over voltage (TOV). The voltage differential between STATCOM terminals and PCC promotes reactive power flow in both directions. When STATCOM's terminal voltage exceeds PCC's, it generates reactive power and acts as a shunt capacitor.

When its terminal voltage is lower than PCC, STATCOM absorbs reactive power like an inductor. In practice, the STATCOM's semiconductor switches are not lossless, so the DC capacitor's energy is lost due to internal converter loss. So the STATCOM must draw active electricity from the grid to keep the capacitor charged. Active power generation is possible if the STATCOM is equipped with an energy storage device or a DC source such as a photovoltaic panels.

#### 1.4 Multi-purpose Single-stage Photovoltaic system

The unbalance of the instantaneous DC input and AC output powers in single/threephase inverters causes double-line frequency voltage ripple on the DC-bus. This power mismatch requires a capacitor to store energy. The power pulse is stored in the capacitor as static energy. Using the two-stage inverter, the DC-bus voltage and capacitor size can be customized to meet the specific needs of the design. Electrolytic capacitors can be replaced with film caps to extend the DC-bus capacitance lifespan, as the capacitance of the DC-bus is lowered. However, the reduction in capacitance results in a high double-line frequency voltage ripple on the DC-bus, which results in a series of odd harmonics in the output current. It's the same voltage as the PV voltage in a single-stage inverter at MPP (MPP). Because of their huge capacitance, electrolytic capacitors are commonly utilized, yet they are also the main cause of inverter failure [3]. Using a film capacitor reduces the capacitance of the decoupling capacitor, reducing cost and increasing longevity. Active solutions using additional circuitry to separate the AC pulsing power have also been devised [4, 5]. These active approaches aim to reduce capacitance by raising the DC-bus voltageV<sub>DC</sub>. However, high voltage stress on power components and switching losses must be carefully managed. There is another way to handle this issue. Two-stage inverters allow for substantially higher voltage ripple on the DC-bus than single-stage inverters while maintaining MPPT efficiency. This double-line voltage ripple causes harmonic distortion in output current. These harmonics have a substantial impact on the power system, loads, and protective relaying [7, 8]. Multi-purpose PV systems are converters that can do more than only convert DC to AC power [36, 37]. Globally, multi-purpose PV systems are being developed and deployed in power systems [38-40]. This section discusses multi-purpose PV systems controls and applications, as well as the essential standards for DG integration.

#### 1.4.1 Functions of Multi-Purpose Single-stage PV systems

An important step forward in the integration of distributed energy resources has been made possible by the advancement in the PV system. PV converters are being reprogrammed with additional capabilities that can support electric grid and help improve the penetration of renewable energy in electric power systems through this approach. FACTS-like features for providing ancillary services have also been included in wind inverters [50, 51] as a parallel development. While PV systems convert DC power to AC power using a Voltage Source Converter (VSC), STATCOMs provide reactive power exchange utilizing a Voltage Source Converter (VSC). A main objective of the PV system act as STATCOM for the providing reactive power regulation during nighttime and also during the daytime, together with the production of real power. Reactive power assistance can be provided by existing PV systems without a significant increase in cost. To increase utility capacity, a multipurpose PV -STATCOM control for PV inverters has been presented here.

#### 1.4.2 Grid Synchronization

Using its voltage-regulated oscillator, the phase-lock loop extracts phase-angle from a grid voltage signal. An angular frequency and phase angle are determined for the grid-connected converter control block, preventing islanded mode, first used to synchronize grid-assist photovoltaic systems (PV), which use comparators to detect polarity deviations in the sensed grid voltage. Multiple zero-crossing detections complicate phase-angle extraction when abnormal grid voltage or weak grids occur. Because stationary frame PLLs only need one voltage signal to synchronize, they are more efficient than alternative techniques. The error signal for the low-pass filter (loop filter, i.e., LF) is provided by a multiplier phase detector (PD) (LF). It generates a 100Hz ripple error signal that proliferates through the LF [8][68-69]. A 100Hz ripple term can be lowered by inserting an additional low-pass filter, but at the expense of bandwidth, phase margin, and full synchronization speed[70] [76]. The DQ PLLs can convert grid parameters to DC quantity and estimate frequency and phase angle. DQ PLL computes frequency and phase angle using two signals, direct and orthogonal (quadrature). Using phase delay filters, differentiation of the input signal, Inverse Park's transform, Hilbert transform, and second-order generalized integrator (SOGI)[71][83], an orthogonal signal is generated from a direct signal, i.e.,

measured grid voltage. This eliminates the 100Hz ripple and increases the inherent synchronization speed and bandwidth over a conventional PLL. The commonly used phase-locked loop (PLL) technique requires complex design and tuning to attain a good stability margin. Inverters with single or three-phase grids can use SOGI-FLL to detect phase angle[72]. For the control system appropriately selected parameters, additional feedback selection will increase synchronization speed during grid irregularities, enhances robustness during grid irregularities and thus predicting appropriate phase angles[74]. SOGI-FLL has the best performance with distorted harmonic components but poor performance with unbalance grid due to negative sequence. Dual SOGI-FLL performs best with no DC offset in the detected grid voltage. DSOGI-FLL can track grid voltage dips, increases, harmonics, imbalance, and frequency fluctuations. It does so even if no PI controller is present. Modified DSOGI-FLL (MDSOGI-FLL) is efficiently designed to encounter DC offset along with all DSOGI-FLL features[74-75].

#### 1.4.3 Modeling & Simulation of Multipurpose PV system and Assessment

The Simulink/ MATLAB software was used to verify the validity of the study system and controller. It has been proposed in [61] to use a grid tied PV system for the compensation during a unbalanced and/or non-linear load. Using the MATLAB/Simulink, modeling of Photovoltaic panel has been modeled and characteristics observed by considering different scenario in context of irradiation and atmospheric temperature. The various grid synchronization techniques are simulated during ideal and non-ideal grid conditions. The Phase Lock loop(PLL), synchronous reference frame based phase lock loop, second order generalized integrator(SOGI) based PLL, second order generalized integrator (SOGI) with Frequency lock loop, dual SOGI-FLL, open loop PLL, modified DSOGI-FLL are simulated and carried out comparative analysis of them. An active shunt filter or reactive power compensation capability has been added to the typical PV system, as seen in[23][27][48]. The various Maximum power point tracking algorithm like Pertube & observed, Incremental conductance, current sensor less MPPT for singlestage grid connected inverter are simulated and discuss prone and cons of these techniques.

#### 1.4.3.1 Implementation using WAIJUNG block-set of Simulink/MATLAB

Model based programming using a WAIJUNG block-set of MATLAB/Simulink in real time offers more accurate views of controller performance than software studies. In a real-time research, actual sensed ADC signals, discrete control model and DAC signals carried out for observation are used in the control process. ARM Cortex M4 is 32 bit microcontroller with the capability of digital signal processing. A WAIJUNG block-set of MATLAB/Simulink is capable to generate C code or hex file for ARM Cortex M4 STM32F407VG microcontroller through KEIL IDE. The KEIL IDE provides hardware debugging for this real time application. A MPPT control, current control, and voltage control are implemented on ARM Cortex M4 STM32F407VG microcontroller using model based programming for grid connected PV system.

#### 1.4.3.2 Experimental Validation

The controller must be validated one last time in the laboratory using a hardware implementation. Now that the small-scale prototype of single-stage grid connected PV system has been established, controller of multi-purpose PV inverter with specific goals has been set up in a laboratory setup. To compensate for harmonics and/or reactive power in [18], the authors employed a grid-connected PV system that was tied to an actual lab setup. Reactive power correction is provided in [23] for the lab validation of a 5 kW solar system. The control system of 5kW multipurpose PV system is realized using a model based programming in the WAIJUNG block set of Simulink/MATLAB to achieve following control objective: PCC voltage regulation and power factor correction by providing the reactive power support to the grid. The control variables of PV arrays, PV inverter and grid are used in control system designing for the model based programming using a 32-bit ARM cortex microcontroller (STM32F407VG). The current sensor less MPPT is implemented and observed the performance. The results of this study were compared with simulation result.

#### 1.4.3.3 Standards for Grid Integration of Distributed Systems

Distribution systems frequently use DGs and DRs, or distributed generation stations (DGs), and distributed resource stations (DRs)[4]. The influence of distributed resources (DR) on the electric power grid makes their integration a critical resource

challenge (EPS). Integration consequences can be wide-ranging due to changes in DR interconnection location and power system characteristics. A few of the DRs impacts on the power system include poor control during reverse power flow, overvoltage, under-voltage, and voltage unbalance. Using IEEE standard 1547-2003, system designers can minimize lots of further potential harms for their systems and power grid. DRs are prohibited by IEEE standard 1547-2003 from actively controlling PCC voltage or causing other Local power system service voltages to deviate from Range A [14]. By this standard, DR voltage regulation may interact with other devices installed by the regional grid operator. IEEE has developed a new integration standard, IEEE Standard d 1547a-2014, due to various studies on voltage management by Distributed Resources. To actively engage in voltage regulation through active and reactive changes, regional grid operators and DR operators will need to be coordinated with and approved by "Standard 1547a-2014 says. The Area power system service voltage at other regional grids must not fall below the ANSI C84.1-2011 1995, Range A criterion as a result of the DR ", it's. As a result, even in the presence of extra voltage regulators, distributed resources like wind turbines, solar panels, energy storage systems, and fuel cells can regulate voltage[1-2][8][14].

#### 1.5 Control of Multipurpose PV System (PV-STATCOM)

For a traditional PV system, a STATCOM is a voltage source converter (VSC) that converts DC electricity to AC power. A STATCOM, on the other hand, exchanges reactive power while a PV system provides active power. These two principles together can enable both active and reactive power. A novel method for using a PV inverter as a STATCOM has been developed [36-38]. The PV system is clearly working below its rated power production for approximately 80% of the day, leaving the inverter capacity underutilized. Also, when the sun isn't shining, the PV inverter is inactive. The above unique STATCOM PV solar system design uses the remaining inverter to exchange reactive power with the grid to manage voltage. This revolutionary technology can provide several advantages at little cost. The leftover capacity of the PV inverter in "Partial STATCOM mode" exchanges reactive power with remaining capacity of the inverter. In this mode, PV converter generates active power first, and then exchanges reactive power with leftover inverter capacity [18].

However, the multipurpose PV system converts into a complete STATCOM automatically during transients or faults. In this situation, the multipurpose PV system disconnects the solar panels and swaps reactive power as a STATCOM for the grid. This method of operation is called "Full STATCOM mode". That is, the multipurpose system PV system decides dependent on system requirements, transient/disturbance kind, time of day, and remaining inverter capacity. Due to the unfavorable impact of DG systems on the voltage profile, utilities have restricted DG connectivity. These inverters can help increase the connection of DGs in distribution networks since they can fully regulate voltage with reactive power assistance. It remains to be seen if the multipurpose PV system control can assist increase PV system installation as DG units. Motivation and Scope of Thesis.The primary goals of PV systems are to reduce the cost of the power converter stage, raise the efficiency of both converters and PV arrays, and significantly improve converter dependability.

Since the characteristics of photovoltaic (PV) modules are affected by solar radiation and temperature, it is necessary to develop control logic for single-stage gridconnected photovoltaic (PV) systems that is simple, efficient, and reliable in order to collect as much power as possible at every operating point. The single-stage PV system should behave as multipurpose system by performing the active power injection along with reactive power exchange to the utility grid for the strengthening utility grid. Furthermore, to modify MPPT algorithm without using a current sensor for the single-stage grid interfaced PV-STATCOM.

#### **1.5.1** Experimental setup

An experimental setup consists of a three phase power card consisting IGBT, IGBT driver cards with S.C. (Short Circuit) protection, 32-bit DSP based microcontroller STM32F407VG, For DC side separate voltage hall sensor, for ac side 3 set of C.T. (Current Transformer) and P.T. (Power Transformer) with DC offset adjustment, unipolar ADC in a microcontroller, 8 set of series connected PV panel strings, three-phase inductive load, three-phase resistive bulb load of 200W, manual DPDT switch, and 3-phase VARIC as a utility grid. The inverter currents and PCC voltage are sensed and scaled into proportionally within 3V by 3-set of current transformer (CT) and power transformer (PT) and scaling circuits, respectively. It is to be taken care that microcontroller has uni-polar ADC pins with the limitation of maximum voltage 3.3V at ADC pins. Hence DC offset circuits are required to converter bi-polar signal into unipolar signal. The role of sensors circuit is sensed as well as scaled into 3V (for the

safety) and DC offset circuits add 1.5V DC into scaled ac signals to make unipolar signal, which is given to the ADC pins of microcontroller. The hall sensors are used to measure current and voltage of PV strings and scaled into 3V to be used in MPPT algorithm to generate active current reference for the control approach of presented PV system. The discrete model of control system of single-stage grid connected system is designed using WAIJUNG block set for STM32F407VG microcontroller in Simulink/MATLAB environment. Software coding and calculation of cycles for different measurement and control of different respective parameter, which must be compatible with the hardware, design of photovoltaic system. The sizing calculation work has been carried out. It includes below works:

- 1) Grid synchronization strategies
- 2) ADC count loop calculation
- 3) Control card design and selection
- 4) Current control loop and voltage control loop strategy implementation
- 5) Hardware protection strategies

Hence, to achieve these objectives, the research work reported in thesis are:

1. The goal of the work is to develop the complete hardware of voltage source inverter for photovoltaic system. Design and analysis the control logic based on inner current and outer voltage loop. It also incorporates MPPT based inverter control. [Single stage conversion].

a)To combine two independent control strategies (i.e. MPPT control for PV side and inverter control for grid side in two-stage grid interfaced system) into one control strategy for single stage operation of voltage source inverter for photovoltaic system.

b) To design and implement control strategy for the protection of photovoltaic system.

2. To modify the control strategy of single-stage grid connected system for the transforming into multi-purpose PV inverter, which is able to managed smartly active power injection along with fulfilling the need of reactive power at PCC of grid without oversizing inverter(which is also known as Partial PV- STATCOM).

3. It can regulate a reactive power current through quadrature – axis (i.e. q-axis) current control within 1-2 cycles during load variation.

4. The modified Dual-SOGI and tan-arc method is employed as grid synchronization techniques to detect phase angle of PCC voltage for the control system during non-ideal grid conditions including dc offset rejection, and also eliminates harmonics component

as well as negative sequence component for phase-angle computation in a tan-arc method.

5. A modified MPPT algorithm is employed to extract the maximum power during the PV intermittency without using a DC current sensor.

#### 1.6 Outline of Thesis

A chapter-wise summary of this thesis is given below:

Chapter 2 demonstrates brief overview of grid connected photovoltaic system (PV), topologies, and control structure of PV system. Discussion on two-stage grid connected PV system and single-stage grid connected PV system. It also gives survey on maximum power point tracking algorithms. It describes the overview of operating principle of STATCOM including mathematical analysis. It also gives survey on control strategy during abnormalities in grid.

Chapter 3 detailed discussion of the Grid Synchronization techniques in Three-Phase Power Converters under ideal and non-ideal grid situations. The comparative assessment of grid synchronization techniques discuss with simulation as well as experimental results.

Chapter 4 presents the modelling of grid connected PV system including current and voltage control. It also includes controller design of inner current loop and outer voltage loop. Mathematical analysis of reactive power support provided by single-stage grid connected PV system to the utility and presented modified MPPT without DC current sensor at PV side.

Chapter 5 provides detailed description of experimental set-up of hardware. It includes detailed description of model-based programming for single-stage grid connected inverter using WAIJUNG block-set in a Simulink/MATLAB and STM32F407VG ARM controller. It also includes about signal scaling for sensor and hardware protection code. It also discusses experimental results of the proposed single-stage grid connected PV system.

Chapter 6 sums up the thesis's findings and highlights its important points. Ongoing studies utilizing this multipurpose single-stage grid connected PV system are also being considered.

Thesis ends with a complete Bibliography.

## CHAPTER-2 OVERVIEW OF GRID CONNECTED PHOTOVOLTAIC SYSTEM

Now-A-Days, fossil fuels are the dominant source of energy for the global economy, but the knowledge of fossil fuels as a fundamental contributor to environmental concerns has prompted mankind to explore alternate energy sources. Additionally, the everyday growth in energy demand might cause challenges for power distributors, such as system instability and even blackouts. The need to create more energy, together with an interest in clean technologies, has resulted in an increase in the development of renewable energy-based power systems [1]. Renewable energy technologies such as photovoltaic (PV) are becoming more commonly accepted as a means of sustaining and enhancing living standards while minimizing environmental damage. The number of solar installations is expanding dramatically, thanks largely to government policies and utility company subsidies for grid-connected photovoltaic systems [3], [4]. Additionally, the standards for interfacing dispersed power generating equipment to the utility network emphasis to seamlessly inject power by overriding the grid disturbances. Both the grid synchronization mechanism and the current controller are crucial in the control system of distributed power generator. As a result, control strategies for dispersed power generating systems become highly intriguing. This chapter presents an overview of the various grid connected system structures, with interfacing photovoltaic (PV) panels as power generating source being covered first. This is followed by a study of grid-side converter control topologies in various reference frames. Moreover, the survey of various maximum power points tracking algorithm are also described in this chapter. This chapter also examines the major components of control mechanisms utilized in grid breakdown circumstances.

## 2.1 General control structure of grid tied PV system

The power controller unit (i.e. voltage source converter and/or DC –DC converter) configuration is directly interfaced to the input power source i.e. Photovoltaic panels,

which converts solar energy into electrical energy. Depending on where the generation equipment is connected, the electricity produced can either be provided to local loads or injected to the utility network for distribution. The control structure of a grid tied PV system is a crucial component of the system i.e. brain of system. A general control structure of grid tied PV system is depicted in Figure 2-1. The duties associated with control can be classified into two major categories.

 A DC Power controller: The primary function of DC voltage control loop is to extract the maximum amount of power possible from the input source i.e. PV panels. In this controller, protection of the input-side converter is, of course, also taken into consideration.



Figure 2-1: General control structure of grid tied PV system

 (ii) Coordinated Grid controller: It may perform the following functions: control of active power injected into the grid; exchange of reactive power between the voltage source converter and the grid; control of dc-link voltage; and grid synchronization.

In addition, auxiliary services such as local voltage and frequency regulation, voltage harmonic compensation, and active filtering may be requested by the grid operator,
depending on the situation. As previously stated, the power conversion unit has a variety of hardware structures, each of which is intimately tied to the type of the power being converted. A review of the technologies that are most commonly utilized nowadays in PV systems, as well as WT systems.

### 2.2 Topologies of Photovoltaic System

Despite the fact that the PV systems have a low-voltage input provided by the PV panels, a larger number of such units can be joined in the series or/and parallel configuration together to get the appropriate voltage, current and power. When it comes to providing typical customer load demand or dumping electricity into the grid, power conditioning systems, such as voltage source converter and DC-DC converters, are frequently employed in distributed power generating system.





The solar photovoltaic system based renewable power generating system is classified according to their structure as follow: (i) Grid interfaced solar photovoltaic system, and (ii) stand-alone solar photovoltaic system (i.e. without grid interconnection). The photovoltaic (PV) panels, in particular, have been designed to turn sunlight into electricity by using PV cells. The stand-alone solar photovoltaic system topologies consist of a DC-DC converter, an inverter (not connected to the grid), batteries,

charge controller, and fuses. The electric energy infrastructure is either very expensive or non-existent to maintain in remote locations; thus, this is the only option. Small-scale stand-alone PV systems are employed in numerous scenarios to provide off-grid power in isolated or rural areas. Their adaptability makes them perfect for any location that receives sufficient sunlight. The benefits and drawbacks of a stand-alone PV system must be considered. Grid-connected photovoltaic (PV) systems are typically deployed using single-stage PV system topology or two-stage PV system topology power conversion. Typically, single-stage PV systems just consist of a grid-tied (DC-AC) converter, in which current control and maximum power point tracking (MPPT) algorithm are employed on the DC-AC converter. The DC bus of grid-tied inverter is directly interfaced to the PV array in this scenario. MPPT is performed by the grid-tied inverter for single-stage PV systems, which has the added benefit of greater efficiency than two-stage PV systems. Additionally, PV systems can control active power injection, and/or reactive power compensation, and active power filtering using either three phase three wire system (3P3W) topology or three phase four wire systems (3P4W). The single-stage 3P4W grid-connected PV system is capable to perform as shunt connected active power filter with a neutral current compensation.

#### 2.2.1 Control Structure of Photovoltaic system

It is indeed usual for photovoltaic system control concerns to be divided into two categories: fundamental and auxiliary. In order to cease solar power generation in the event of abnormal conditions, the fundamental control consists primarily of the maximum power extraction algorithm, grid synchronization harmonic elimination ability and unity power factor (which achieved through current controller). In order to comply with standards, PV system tied directly tied to residential power grid should be established to fulfil necessary requirements of grid codes. However, nowadays, it can also be implemented to improve the efficiency and enhance the performance of the electrical system by providing "ancillary services": unity power factor at grid side, frequency and voltage support could be offered to local loads [25], [26], or to the electricity grid [27].Now-a-days, photovoltaic converter can be implemented successfully to provide reactive power support as ancillary services

for distribution grids [28–30]. It is possible to improve voltage profiles by injecting reactive power into the grid, which strengthens the utility grid and maintains the desired quality of supply without requiring further investments. This provides several evidence of how far the photovoltaic system perspective has shifted in recent decades, particularly when compared to surveys that have been compiled in the past that imply restrictions to the penetration of large number of renewable energy sources in order to prevent causing the false trips and voltage rise among other things. [31]. Ancillary service provided by Photovoltaic systems is not profit-free, as this fact must be taken into account. It is composed of two hardware units: the power circuit as heart of system and the control unit as brain of system. Taking into consideration the power circuit, the converter can be either a single-stage PV system (DC-AC converter) or a two-stage converter (DC-DC converter + DC-AC converter) with or without galvanic isolation [32]. A two-stage PV system is represented by the diagram in Figure 2-3. Once again, there are two methods for achieving isolation: (1) utilizing the DC-DC converter, and (2) employing an isolation transformer after the DC-AC stage, both of which are effective. Generally, the output voltage of the PV array is not high enough and varying with the changing environmental conditions.



Figure 2-3: General structure of two -stage grid tied PV system

Figure 2-3 shows a typical configuration for this system. PV panel voltage fluctuates during the day due to temperature changes, so a step-up DC converter is needed to keep the DC-bus voltage constant. An additional boost converter stage is used to maintain a constant DC-bus voltage regardless of fluctuating input voltage to extract the maximum power from Photovoltaic panels. Two-stage

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topologies have some advantages in controller design, but it also has some drawbacks. The overall energy transfer efficiency decreases as the number of circuit stages increases and the system's complexity increases; as a result, making the system less reliable. Normally, an LCL filter is used between the voltage source converter and the utility grid.



Figure 2-4: General structure of Single –Stage grid tied PV system

In addition to their high efficiency, single-stage converters have the advantages of being less expensive and being simpler to implement [33–35]. Figure 2-4 shows the basic block schematic of inverter topology without trans- former, which does not provide galvanic isolation with grid. The output filter is used to cut off the switching ripple that occurs during the switching process. The input power control, which is made of an MPPT algorithm and a DC voltage controller, provides the voltage/ current control reference signal for the outer voltage/ inner current control loop, respectively. In addition, in many countries, where such systems are built with the isolation between the input and output powers, which are essential to ensure proper operation and protection. Figure 2-5 shows the basic block schematic of grid connected PV inverter with transformer. The transformer shown here is low frequency transformer (LFT). It provides robust construction, galvanic isolation to grid, and protection to earth fault. It has drawback of high weight, decrease overall efficiency due to less efficiency of transformer, and increases size and cost of the structure due to DC-DC converter and transformer.



INVERTER Figure 2-5: General structure of single-stage PV system with Galvanic Isolation

It has advantage of less weight and cost of system, improvement in efficiency, and reduces the overall system structure due to elimination of transformer. It also increases the reliability due to less number of components. The overall system can be developed on single printed circuit board(PCB) so the system become compact and easy to mount below the PV panels itself. It has drawback of no electrical separation to grid, may arise leakage current and issue of Common mode voltage with sinusoidal pulse width modulation switching scheme.

#### 2.2.2 Survey on Maximum power point Tracking Methods

Temperature and solar radiation have a significant effect on the output of a PV module. As the temperature rises, output power from the solar panels is decreasing. As a result, the operating point must be constantly monitored using an MPPT algorithm [8]–[11] to extract maximum available power from the solar panels. The MPPT algorithm must immediately adjust the output power of the PV system to maximize performance for operating at MPP when the weather changes. Single-stage or Two-stage photovoltaic topologies necessitate various implementations of maximum power point tracking algorithms (MPPT). The maximum power point tracking algorithms is applied to the DC-DC converter for the extracting maximum power from the solar panels in a two-stage conversion system, while the MPPT is added to the control of the DC-AC converter in a single-stage conversion system. Direct control of AC current or DC voltage can be achieved by the MPPT; alternatively, a DC voltage controller can be used to regulate the AC current. The feed-forward power is used to improve the dynamic performance of the MPPT.

technology since mismatching results in a decrease in MPPT efficiency. A DC-DC converter within the photovoltaic modules [21], [22], [24] or a DC-AC converter unit incorporated into each PV module can be used to run the MPPT algorithm in this instance [21], [22], [24]. MIC stands for "module integrated converter" when the entire unit is treated as a PV -AC system directly interfaced to the main grid [23]. The article [8] reviews the main aspects of the different MPPT approaches, whereas article [20] provides an estimate of the costs. MPPT techniques include the Constant Voltage (CV), Perturb and Observe (P&O), and Incremental Conductance (INC) approaches. They are referred to as "hill-climbing" methods because they rely on the power characteristic, which increases step- size in MPPT when the derivative of PV power with respect to PV voltage is greater than zero, a decrease step- size when this derivative is less than zero, and MPPT reach to maximum power point increase when this derivative is zero. For the constant voltage MPPT algorithm, it is implemented based on the observation that the ratio between the measured voltages at maximum power to the open-circuit voltage of PV module are about 0.77. The operative voltage is set to 76 percent of the open-circuit voltage of PV module, and this value is preserved for the specified period before the measurements are repeated, because the voltage varies slightly with shifting solar irradiance.



Figure 2-6: Power-voltage PV characteristic

The following are some standard MPPT algorithms: Perturb and Observe (P&O), Incremental Conductance (IC), Constant Open Voltage (CV), a combined approach using the Incremental Conductance and Constant Open Voltage, ripple correction, and short-circuit current. These techniques differ in terms of ease, hardware implementation, convergence speed, number of sensors involved, affordability, effectiveness range, and requirement for parameterization





. Amongst the most popular MPPT methods is P&O, which is simple to implement on the microcontroller, digital signal processor, and an FPGA[13]. Figure 2-7 shows flowchart of perturb and observe(P&O) MPPT algorithm for the extraction of maximum power from PV panels in grid tied PV system. The P&O MPPT algorithm works as follow: when the voltage variation produces  $\frac{dP_{PV}}{dV_{PV}} > 0$ , the algorithm perturbs the PV voltage in the same direction, which implies it advances the set point toward the MPP. If  $\frac{dP_{PV}}{dV_{PV}} < 0$ , then its reverses the direction of perturb, since the set point is moving away from the MPP at this moment. This key benefit of P&O MPPT algorithm is its simplicity of implementation, which requires few sums, just one multiplication and comparisons. The drawbacks include swings in the vicinity of the MPP and a tendency to lose MPP tracking when the irradiance level changes rapidly.. The Incremental Conductance approach overcomes the limitation of the P&O MPPT algorithm in tracking peak power under varying air conditions. Incremental Conductance can be used to investigate whether the MPPT has achieved its Maximum PowerPoint and when it is wise to stop perturbing the operating point.



Figure 2-8: Flowchart of incremental conductance (INC) MPPT algorithm

The Incremental Conductance (IC) algorithm is based on the observation that the following equation holds at the MPP;

$$\frac{d P_{PV}}{d V_{PV}} = \frac{d (V_{PV} I_{PV})}{d V_{PV}} = I_{PV} + V_{PV} \frac{d I_{PV}}{d V_{PV}}$$
(2.1)

The equation (2.1) is simplified as:

$$\frac{1}{V_{PV}} \frac{dP}{dV_{PV}} = \frac{I_{PV}}{V_{PV}} + \frac{dI_{PV}}{dV_{PV}} = G + dG$$
(2.2)

Here,  $dG = \frac{dI_{PV}}{dV_{PV}}$  is the incremental conductance and  $\frac{I_{PV}}{V_{PV}}$  is the conductance.

At the maximum power point, the derivative of PV power with respect to voltage becomes zero and it gives:

$$\frac{\mathrm{d}\,\mathrm{I}_{\,\mathrm{PV}}}{\mathrm{d}\,\mathrm{V}_{\,\mathrm{PV}}} = -\frac{\mathrm{I}_{\,\mathrm{PV}}}{\mathrm{V}_{\,\mathrm{PV}}} \tag{2.3}$$

If equation (2.3) is fulfilled, the algorithm halts its efforts to change the set-point the algorithm. The algorithm determines which way to perturb the of voltage depending on the sign of  $\frac{d P}{d V_{PV}}$ . Figure 2-8 illustrates the basic sequence of the incremental conductance algorithm. Using this approach, the maximum power point may be tracked quickly and accurately while avoiding abnormal fluctuations around the MPP, which would take additional computational time. Instead of adjusting the voltage of the PV panel, an alternative approach to INC focuses on modifying the current. From the PV curve shown in Figure 2-6, change of voltage between two consecutive sampling times can be ignored because it is so slow and steady on the right side of the maximum power point in P-Vcurve. A linear relationship between  $\frac{dP}{dV_{PV}}$  versus  $I_{PV}$  and  $\frac{dP}{dV_{PV}}$  against  $V_{PV}$  has been hypothesized in this theory. As a result, the reference current is simple to calculate when  $\frac{d P}{d V_{PV}}$  changes linearly, while V<sub>ref</sub> is more complex to calculate when  $\frac{d P}{d V_{PV}}$  changes nonlinearly. In this scenario, the output of the INC method gives the current reference value instead of the voltage reference with minor modification

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Figure 2-9: Flowchart of modified incremental conductance (INC) MPPT algorithm

Figure 2-9 shows the flowchart of modified INC MPPT algorithm to compute current reference value. The derivative of PV power (i.e.dP<sub>PV</sub>) is not equal zero when the climatic situation has changed. As long as derivative of current (i.e.  $dI_{PV}$ ) is below zero, the set-point will be moved away from the maximum power point by increasing  $\frac{d P}{d V_{PV}}$  and the current reference value. As soon as derivative of current (i.e.  $dI_{PV}$ ) exceeds zero, the reversal is carried out. How quickly the maximum power point is maintained depends on the INC MPPT step-size. Following thumb rule should be observed when the value of step-size is chosen : with larger increments, faster tracking can be performed by the cost of poor performance of MPPT algorithm due to large oscillation around MPP, consequences, gives lower efficiency. When the MPPT has a smaller increment, the situation is reversed. For the fixed step-size MPPT, a trade-off must be made between dynamic and oscillatory dynamics. The single-stage grid tied PV systems gives grid side current control only, which

means the MPPT controls the active component of grid current. As a result, the reference value of voltage is computed by MPPT algorithm for extracting maximum available solar power, which is further given to outer DC voltage control loop of PV system.



Figure 2-10 Flowchart of ripple correlation MPPT algorithm

As seen PV curve in Figure 2-6, the PV acts as a current source on the left and a voltage source on the right side of the MPP. Performing near the MPP reduces ripple power on the PV side [18]. The desired performance is carried by adopting a variable step-size MPPT algorithm, which gives reference voltage angle extracting maximum power from the PV [25], and this approach is known as ripple correlation algorithm and flowchart of this MPPT algorithm is shown in Figure 2-10. A power-voltage PV characteristic shows that if it runs on the left side of the MPP, the voltage angle derivative should be decreased, which is given by side = -1. However, the region on the right side of the MPP has to increase (side=+1). The PV side power oscillations are measured to set the increment (Figure 2-10). For comparison, the

"ripple correlation control" approach has 99.7% efficiency in high irradiation environments [19], while P&O and INC have 98.7% and 99.1% efficiency [20]. However, due to concerns with consistency during MPP tracking studies, a consistent technique to examine MPPT algorithms is still lacking. In 2010, the BS EN 50530 European Standard [68] was published, which offers the sole process for measuring inverter MPPT efficiency. The impact of MPPT approaches on grid-side power quality is the final objective. The INC algorithm is much more appropriate for gridtied PV systems with only single-conversion stage.

## 2.3 VSC Based Solar Energy Conversion System with Indirect Cost Reduction

The solar PV system remains unutilized for more then 2/3rd of the day. During day time, the power converters is employed to inject active power from PV panels along with other ancillary functions like harmonic compensation, grid current balancing, neutral current compensation, and reactive power compensation, which will also indirectly reduce the cost of operation. During night time, the voltage source converter of PV system can be employed to provide the reactive power compensation for the grid.

#### 2.3.1 Operating Principle of STATCOM

Shunt-connected reactive compensation equipment like the Static Synchronous Compensator (STATCOM) can produce and/or absorb reactive power, and its output can be controlled to regulate certain electric power system variables. This type of compensator is similar to a rotating compensator without mechanical inertia because it uses solid-state power switching devices to alter the three-phase voltages quickly, both in magnitude and phase angle. The STATCOM consists of a three-phase voltage source converter, line filter, a step-down transformer ,and a DC-bus capacitor. The voltage source converter (VSC) is the core component of FACTS devices like a STATCOM. The leakage reactance enables reactive power transfer between the STATCOM and the grid so that the AC voltage at the bus bar can be controlled to improve the voltage profile of the grid, which is the prime objective of the STATCOM.



Figure 2-11: One-line diagram of a STATCOM

Figure 2-11 illustrates the underlying voltage-source inverter representation for reactive power compensation. The concept of STATCOM functionality is as follows. The VSC generates a controlled AC voltage behind the leaking reactance. The voltage of STATCOM is matched with the AC bus voltage of the grid if the magnitude of grid voltage is higher than the magnitude of the VSC; the STATCOM behaves as an inductor; otherwise, it acts as a capacitor. The net reactive power flow is zero if the magnitude of VSC and STATCOM are equal. The phase angle between STATCOM terminals and the grid can be used to control active power when STATCOM has a DC power or energy If the phase angle of the grid leads to the phase angle of STATCOM, then Active power is absorbed by the STATCOM; otherwise, it is supplied by the STATCOM. The distribution Static Compensator (DSTATCOM) device protects the distribution system against the impacts of voltage fluctuations, voltage sags, and voltage swells, as well as non-linear loads. It is also possible to use a dynamic voltage restorer (DVR) to shield a critical load from voltage fluctuations caused by the associated distribution system. A series and shunt controller called the Unified Power Quality Conditioner (UPQC) is used to correct supply voltage and load current faults in the distribution system. Reactive power compensation in Transmission networks

can be provided via the DSTATCOM, a flexible device. Similar to a normal synchronous compensator, which is just a synchronous generator where the field current is utilized to alter the regulated voltage; this device uses the field current to control the voltage.

#### 2.3.1.1 Concept of Reactive Power

The distribution Static Compensator (DSTATCOM) device protects the distribution system against the impacts of voltage fluctuations, voltage sags, and voltage swells, as well as non-linear loads. It is also possible to use a dynamic voltage restorer (DVR) to shield a critical load from voltage fluctuations caused by the associated distribution system. A series and shunt controller called the Unified Power Quality Conditioner (UPQC) is used to correct supply voltage and load current faults in the distribution system. Reactive power compensation in Transmission networks can be provided via the DSTATCOM, a flexible device. Like a normal synchronous compensator, which is just a synchronous generator where the field current is utilized to alter the regulated voltage, this device uses the field current to control the voltage. The DSTATCOM regulates the voltage using a voltage source converter (VSC). It is the ratio of real power to apparent power known as the power factor. Mathematically, this definition can be expressed as kW/kVA, where kW is the active (actual) power, and kVA is the active plus the reactive power. Even though reactive power has a straightforward definition, even those with a thorough understanding of technical concepts have trouble comprehending its complexities. Reactive power is explained as follows: in an AC power system, only actual power is transmitted when voltage and current rise and fall simultaneously (amplitude variation), while active and reactive power is transmitted when voltage and current shift in time(phase-angle variation). A net movement of power from one point to another can be seen when calculating the average active power over time; however, the average reactive power is zero regardless of network. Reactive power is when the energy pumped from one direction is precisely equal to the energy received in the other direction. As a result, no active energy is generated or used. Reactive power losses are measured and compensated for by introducing many reactive power compensating devices. An inductor stores reactive power since it stores energy in form of a magnetic field. Put another way, the

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magnetic field builds up over time, and the current reaches its full magnitude when voltage is supplied. This results in the current lagging behind the voltage. A capacitance generates reactive power since it stores energy in the form of an electric field.

In an inductive circuit, the instantaneous power is computed as:

$$p = V_{\max} I_{\max} \cos \omega t \cos(\omega t - \theta)$$
(2.4)

The simplification of equation (2.4) is described as:

$$p = \frac{V_{\max}I_{\max}}{2}\cos\theta \left(1 + \cos 2\omega t\right) + \frac{V_{\max}I_{\max}}{2}\sin\theta\sin 2\omega t$$
(2.5)

The instantaneous reactive power is given by:

$$Q = \frac{V_{\text{max}}I_{\text{max}}}{2}\sin\theta\sin2\omega t$$
(2.6)

A number of parameters are used here, including the instantaneous power 'p', maximum voltage and maximum currentV<sub>max</sub>, angular frequency ' $\omega$ ', and the angle ' $\theta$ '.

The average value of reactive power is null, and its instantaneous reactive power value pulsates at twice the system frequency. The instantaneous reactive power is given by:

$$Q = |V||I|\sin\theta \tag{2.7}$$

Although a zero average does not imply that no energy is moving, it does suggest that the actual quantity that flows in one direction for half a cycle and then returns in the next half-cycle means that no energy is moving. Variations in fundamental component voltages of the inverter are used to govern the reactive power transfer between the grid and compensators. By varying the switching angle of the semiconductor devices, the fundamental component of the inverter's voltage is driven to either lead or lag grid voltage by a few degrees. As a result, the inverter's output voltage and reactive power are affected by the amount of active energy flowing into or out of the inverter's DC capacitor. Active power is zero if the compensator solely provides reactive power; hence the DC capacitor has no effect. As a result, the capacitor's voltage remains constant. The capacitor, then, does not play a role in creating reactive power [2].

#### **2.3.1.2 Need for Reactive Power Compensation**

It is essential to use reactive power compensation to prevent voltage collapse and sag and improve the system's overall stability and better utilize the equipment connected to the system. System stability and transmission line impedance are both affected by the consumption of reactive power due to the impedance of transmission lines and the necessity for lagging VAR by most generators. Outages can occur due to excessive voltage dips because of the more significant losses that need to be provided by the source, resulting in additional stress on the system. As a result, it concludes that compensating reactive power alleviates these effects and aids in better transient reaction in the case of faults and disturbances. Since recently, there has been a rise in attention to approaches employed for compensation and the inclusion of more effective devices in technology. If the lines are to be freed from the burden of carrying reactive power, which is better delivered nearby the generators or the loads, it is imperative. A distribution substation or a transmission substation can use shunt compensation positioned close to the load. Increased transmission system losses, reduced power transmission capabilities, and significant amplitude voltage swings at the receiving end can be caused by reactive power. Voltage-amplitude oscillations caused by fast variations in the reactive power usage of loads can also be generated. As a result, power oscillations can be caused by voltage changes in the electric system

#### 2.3.1.3 Analysis of STATCOM

Figure 2-12 [53] depicts the STATCOM system's per-phase entire equivalent circuit, which helps illustrate the system's basic working principles. Assume, the grid voltage is  $V_{pcc}$ ,  $I_1$  is the fundamental component of the current, and output voltage of the inverter is  $V_{inv}$ . The STATCOM is connected to the grid by a reactor  $L_s$  and a resistor  $R_s$ . As a result of reactive coupling, the line current that flows in/out of the VSC is always at an 90° angle to the grid. Depending on the voltage of the DC side capacitor, the STATCOM absorbs or provides a certain amount of reactive power. This voltage can be controlled by adjusting the real power transmission between the grid and the STATCOM.



Figure 2-12: Per-phase fundamental equivalent circuit

The capacitor voltage drops when the inverter output voltage  $V_{inv}$  is ahead of the main voltage  $V_{pcc}$  by angle $\alpha$ , and it rises when the inverter output voltage  $V_{inv}$  is behind the main voltage  $V_{pcc}$ . Phase angle of inverter can vary the voltage levels of DC capacitors [102]. The phasor-diagram of voltage and current of VSC and grid is shown as in Figure 2-13, can be regulated in this way. The STATCOM is primarily responsible for controlling the power transmission voltage at the connection point. A regulated reactive current is drawn from the line to accomplish this. Statically controlled VAR generators do not have the capacity to interchange real power with a line, as the STATCOM does. For this reason, the converter and its DC-bus must be actively managed to maintain a value that is, on average, zero and only deviates from this value to account for system losses.



Figure 2-13: Phasor diagram for leading and lagging mode

To understand and control the behavior of the STATCOM, instantaneous real power is provided by:

$$\mathbf{p} = \mathbf{v}_{\mathbf{a}}\mathbf{i}_{\mathbf{a}} + \mathbf{v}_{\mathbf{b}}\mathbf{i}_{\mathbf{b}} + \mathbf{v}_{\mathbf{c}}\mathbf{i}_{\mathbf{c}} \tag{2.8}$$





Instantaneous reactive current can be thought of conceptually as part of a three-phase current system that can be removed at any time without affecting P.

A vector interpretation of the instantaneous values of the circuit variables yields the algebraic definition of instantaneous reactive current. As shown in Figure 2-14, a vector diagram can represent a combination of three instantaneous phase variables that add up to zero. Each of the three symmetrically oriented phase axes corresponds to the instantaneous value of the corresponding phase variable when a vector drawn from the origin to this point is projected vertically onto it. As shown in Figure 2-15, an orthogonal coordinate system with DQ components is used to extend the vector representation further.

The current vectors transformation from abc  $\rightarrow$ dq components are computed as:

$$\begin{bmatrix} i_{d} \\ i_{q} \\ 0 \end{bmatrix} = \frac{3}{2} \begin{bmatrix} 1 & \frac{-1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{a} \\ i_{b} \\ i_{c} \end{bmatrix}$$
(2.9)

Consequently, the constant 3/2 is selected so that the definition matches with the traditional phasor term in balanced steady-state conditions

In context of DQ reference frame, the instantaneous power can be computed as



**Figure 2-15: Definition of orthogonal coordinates** 

The phase angle between the voltage and current vectors can be seen in Figure 2-15. The current vector can only generate the instantaneous power in phase with the instantaneous voltage vector. The instantaneous reactive current is the remaining component of the current that can be withdrawn without affecting the power.

The definition for instantaneous reactive power can be derived from these findings:

$$Q = \frac{3}{2} (v_d i_q - v_q i_d)$$
(2-11)

They follow the trajectory of the voltage vector and the d and q coordinates within this synchronously rotating reference frame are given by the following time-varying transformation: Figure 2-16 illustrates how the vector coordinate frame can be manipulated further to separate variables, which is used to control the flow of real power in/out of grid. In the synchronous reference frame, the instantaneous active power and the instantaneous reactive power are computed as :

$$P = \frac{3}{2} |v|i_d; Q = \frac{3}{2} |v|i_q; \qquad (2.12)$$



Figure 2-16: Definition of rotating reference frame

The vectors of current and voltage in the DQ reference frame have constant coordinates when the system is in balanced steady state.

## 2.4 Control system of grid connected system

The grid connected voltage source converter is controlled by two cascaded loops i.e. internal current control loop and outer voltage control loop. A quick internal current control loop governs grid current, whereas an outer voltage control loop regulates dc-link voltage [17–22]. Because the current control loop is responsible for ensuring power quality and ensuring current protection, the current controller must have harmonic correction and dynamic properties. Figure 2-17 shows the control structure of grid tied PV system in synchronous reference frame. System power flow can be balanced by using the dc-link voltage controller. The system stability with modest dynamics is often the goal of this controller design. A DC-bus voltage loop cascading with an inner power loop may be used to operate the grid-side controller in some works, rather than a current loop.



#### 2.4.1 Synchronous Reference Frame Current Control



A reference frame transformation module, such as  $abc \rightarrow dq$ , is used in synchronous reference frame control, also known as dq control, to transform grid current and voltage waveforms into a reference frame that rotates in synchronous with the grid voltage. It is possible to filter and control more easily [25] by converting the control variables to DC values. In this design, the DC bus voltage is regulated to meet the output power requirements. Active current controllers use this as their output, but the reactive current controllers often use zero as a reference if reactive power controls are not allowed. A reactive power reference must be imposed on the system in order to manage the reactive power. Proportional-integral (PI) controllers are commonly connected with the dq control structure due to their ability to regulate DC variables. Because the controlled current must be in phase with the grid voltage, the  $abc \rightarrow dq$ transformation module must extract the phase- angle from the grid voltages. Filtering the grid voltages and extracting the phase angle using the arc-tangent function may be a solution. [26]–[28]. For grid connected system, the phase-locked loop (PLL) technique [29-33] has become standard for obtaining the phase angle of grid voltages. Cross-coupling terms and voltage feedforward are commonly employed to improve PI controller performance in Figure 2-17 [17], [19], [25], [34], [35]. Despite these advancements, low-order harmonic correction in PI controllers is still weak, posing a severe problem in grid-connected systems.

#### 2.4.2 abc Frame Control

Natural (abc) frame control is based on the principle that each grid current should have its own controller, but still the alternative approaches to integrate three-phase systems, such as star or delta connection, without or with an neutral wire, must be taken into account when developing the control system.



Figure 2-18 : Current Control loop of grid tied PV system for stationary reference frame(PR controller)

Additionally, it is viable to have three distinct controllers, which includes additional considerations for the dead- band technique or hysteresis technique. The dead- band technique or hysteresis technique are frequently used in natural (abc) frame control systems during non-linear loads because of the high dynamics they provide. Digital systems like high-speed microcontroller, field-programmable gate arrays (FPGA), and digital signal processors(DSP) are efficient since the efficiency and capability of these controllers is directly related to the sampling frequency. The three reference currents aregenerated without PLLsystem. These reference currents are compared to th e matching sensed currents, and theerrors are logged in the controller for the gating signal generation. The modulator is no longer required if dead beat controllers or hys teresis are used in the current loop. The PWM modulator is required to generate gating signals when the PI or PR controllers are employed. It is possible to implement the PR controller in the abc frame as shown in Figure 2-18[35]. PI

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controller is often used in the synchronous reference frame, as shown in Figure 2-17. Because the control system is already in a stationary frame, the implementation of a PR controller is simple in abc. Hysteresis control requires an adaptive band to be developed for a fixed switching frequency in the case of an adaptive controller. Various approaches and strategies to achieve fixed switching frequencies are discussed in [67].



Figure 2-19: Current Control loop of grid tied PV system for dead-beat controller

Using a dead-beat controller, the control system adds unit sample delay. An observer can be added to the controller to mitigate for the unit sample delay [46], as shown in Figure 2-19, to adjust the current reference.

The discrete transfer function of controller is describe as :

$$G_{DB} = \frac{1}{A} \frac{1 - e^{-\frac{R_f}{L_f} T_s} z^{-1}}{1 - z^{-1}}; \quad A = \frac{1}{R_f} \left( e^{-\frac{R_f}{L_f} T_s} - 1 \right)$$
(2.13)

The observer of dead-beat controller is given as:

$$F_{\rm DB} = \frac{1}{1 - z^{-1}} \tag{2.14}$$

Hence, reference current is computed as:

$$i^{*'} = F_{DB} (i^* - i)$$
 (2.15)

An effort was made by the controller to eliminate the anomaly by adding one sample delay. As a result, a controller with a very fast response time and no delay has been created. Another benefit of using a microprocessor is that the dead-beat controller and observer algorithms are simple.

# 2.4.2.1 Survey of Control Structures for reference current generation

One of the key limitations of the synchronous reference frame based control system is the requirement for cross-coupling terms and voltage feedforward. In addition, the grid voltage phase angle is crucial in this approach. Figure 2-20 and Figure 2-21 show hypothetical application of abc frame control in which reference current for active power is determined by the output DC-bus voltage controller. The gating pulses for the voltage source converter are generated using either hysteresis current controller or sinusoidal pulse width modulation , as shown in Figure 2-20 and Figure 2-21.





While complexity of the control of reference current generation using PR controllers in a stationary reference frame becomes lower than when using synchronous reference frame based control system. Moreover, the inclusion of the grid voltages template for reference current generation eliminates the necessity of PLL or phase angle information. Due to the sheer nature of the abc or stationary reference frame, a great degree of complexity can be achieved using a hysteresis controller with an adaptive band . Implementing a dead-beat controller, on the other hand, results in a more straightforward control strategy. Just as with stationary frame control, it is not necessary to know the phase angle or need of PLL. If grid voltages are employed to create the current reference, this control structure allows for individual control of each phase.



Figure 2-21: Control structure of grid tied PV system using sinusoidal pulse width modulation

# 2.5 Survey of Control Strategy during the abnormality in grid

Power grid instability may occur in some countries when large amounts of distributed power generation are interconnected. Because of this, dispersed power generation requires more stringent grid connecting regulations. Distributed power generation is becoming increasingly popular as a means of addressing with grid disturbances including sudden changes in voltage and frequency. Grid faults can be divided into two categories. [55]:

- Balanced voltage sag: It arises when all three grid voltages drop equally, but the system as a whole remains stable. This type of failure is extremely rare in power systems.
- Unbalanced voltage sag: This occurs when the phases have unequal amplitude drops and phase shifts between them. Shorting one or two phases to ground or to each other causes this issue.

Second harmonic oscillations migrate across the system and cause ripples in the DClink voltage. The control variables of the system are also affected. It is possible to tune the PLL system to obtain the precise phase angle of the grid voltage and to filter out the negative sequences. ([57–59]).

If the PLL system is not designed to be immune to imbalance, second-harmonic oscillations can affect the phase angle of grid voltages. The generation of current reference is also affected by second harmonic oscillations in the DC-bus voltage. Ride-through ability for distributed power generating system requires that the consequence of the unbalance be mitigated when performing in abnormal conditions.

Under faults, a control strategy can be implemented in one of four ways.

#### 2.5.1 Unity Power Factor control approach

While grid faults occur, grid tied system has the ability to maintain unity power factor by employing various control strategies. Distributed power generation systems are stable during balanced grid voltages, but the negative sequence component of a grid fault causes oscillations at double the fundamental frequency of grid voltage phase angle oscillations. Because the injected currents will no longer have a sine-like waveform, they will instead have high-order components in their waveforms. There is no reactive power being injected into the grid since the current vector is directly proportional to the voltage vector at all times. Thus, during the fault duration, both active and reactive instantaneous powers remain constant.

#### **2.5.2** Control approach of the Positive sequences detection (PSC)

Another control strategy that can be employed in a fault event is the positive sequence of grid voltages. In contrast to unity power factor management, a precise phase-angle extraction from grid voltages is necessary during unbalance grid voltage situation. Decouple double synchronous reference frame -PLL (DDSRF-PLL) are desirable for the detection of Positive voltage sequences of grid voltage and elimination of and negative voltage from the grid voltages. However, it gives precise phase-angle of grid voltages to the control system of grid tied system by the cost of complexity in implementation as well as slower down the performance of PLL. To encounter above issue, the dual-second ordered generalized integrator -frequency lock loop(DSOGI-FLL) is employed to extract precise phase-angle of grid voltage without compromising the reduction in bandwidth of PLL. There are identical reference currents generation for the distributed power generating system using a control structure like a dq-SRF using either DDSRF-PLL or DSOGI-FLL, and natural frame control using either DDSRF-PLL or DSOGI-FLL. Here, the only problem is the DC-bus voltage ripple, which has an impact on the current flowing. Using a digital filter such as delay signal cancellation [17], this can be eliminated without causing any delay to the system. Second-harmonic ripple can cause device failure if the DC-bus capacitor is not large enough. The amplitude of grid currents will increase, but they will stay sinusoidal and balanced if there is a defect in the grid. Double-frequency oscillations will appear in all power during the fault.

#### 2.5.3 Control approach for constant Active Power Management

Under abnormal grid conditions, a third control method may be to preserve constant active power injection to the grid by distributed power generating system. In the event of an imbalance in the grid voltages, both positive as well as negative sequences will be present. In the same manner, the grid current will become unbalanced, resulting in double-harmonic oscillations for both active and reactive powers. PI controllers are used to regulate the current in the control structure, however extra controllers are required for the elimination of negative sequence from the current of distributed power generating system[17], [61]. This controller has the ability to regulate both  $+\omega$  and  $-\omega$  currents, making it a clear benefit from an implementation perspective in the event of a system of control based on the PR controller. While a disturbance is occurring, the grid currents really aren't balanced when using a constant power regulation technique. Furthermore, the reactive power oscillates at a significant rate.

#### 2.5.4 Control approach for constant reactive Power Management

An analogous expression can be found for reactive power to eliminate the doublefrequency oscillations, much like for constant active power management. It is also possible to find a current vector that is orthogonal to the grid voltage vector, giving the distributed power generating system the ability to independently manage its reactive power output. It is necessary to alter the reference for reactive power from zero to the corresponding value when a grid fault is recognized in this situation. By utilizing one of these control strategies, it is possible to comply with the impending grid rules regardless of what demands are placed on it by the power system controller when the distributed power generating system is interfaced to the grid

#### 2.6 Conclusion

There is an overview of control structures that can be employed in a gridconnected system. The main aspects of various implementation structures, such as natural frame, stationary frame, and synchronous frame control structures, were highlighted. A control techniques for the grid-tied distributive generating system during the imbalanced grid disturbances were also categorized. Single-stage

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PV systems often use an INC-based MPPT method, while power derivative (dP)-INC MPPT, which monitors the power oscillations, has shown the superior efficiency as compared to the other techniques.

## CHAPTER-3 GRID SYNCHRONIZATION FOR THREE-PHASE GRID-TIED CONVERTER

The power grid is a complex dynamic system that is affected by a variety of events, such as continuous variation in the connection of electrical loads, interference and resonance due to harmonic currents flowing through the line, faults caused by lightning strikes, and errors in the operation of electrical equipment. Therefore, when the power converter is connected to the power grid, the grid variable cannot be regarded as a constant amplitude and constant frequency, but it should be continuously monitored to ensure the desired performance of the grid connected power converter. The basic amplitude, frequency, and phase-angle information become the key controllable parameters for the effective operation of the gridconnected converter (GCC) [67]. For this reason, the control algorithm based on the concept of grid synchronization is very important for estimating the grid voltage parameters required for GCC control, protection and synchronization. The phaseangle of the grid voltage is critical and essential parameter for the control system of grid-connected power converters, because popular control strategies (for example, direct power control, vector oriented control) strongly depend on the phase angle of the grid voltage to achieve Park transformation (dq reference frame conversion). The synchronous frame voltages (voltages at dq reference frame) are key parameter for the control system to decouple the current control loop under the dq reference frame[68]. Therefore, the grid synchronization technology is a basic component of the grid-connected converter control strategy, and it is very important to ensure the satisfactory performance of the converter. In order to achieve precise and fast synchronization, many different grid synchronization technologies have been intensively studied and proposed [67-69]. It should be noted that the grid voltage during grid synchronization may be under normal or abnormal conditions (i.e.  $1-\Phi$ phase grid voltage,  $3-\Phi$  phase unbalanced grid voltage,  $3-\Phi$  phase distortion grid voltage, phase-angle jump, frequency shift), and in the above method, PLL and FLL are crucial techniques to compute the utility grid parameters. However, interrelated feedback can be observed in these technologies, which may affect the tuning process

as well as the stability margin and of the entire control scheme [8][70]. The conventional three-phase PLL, commonly known as synchronous reference frame (SRF), has excellent performance during the ideal grid situation (i.e. balanced grid voltage). However, if the measured grid voltage signal is unbalanced or distorted, it will give oscillatory response of computed fundamental frequency [70-72]. The decouple synchronous reference frame PLL (DDSRF-PLL) technique reported in the literature [8] improves the poor performance of the traditional SRF based PLL. The DDSRF-PLL extracts positive and negative sequence components from the nonideal grid voltages to compute the frequency. However, the performance of DDSRF-PLL will decrease during the highly distorted grid voltages. It can be found that under this distorted grid signal condition, the phase detector (PD) structure based on the generalized integrator (GI) has better performance and reliability [8][74-75]. Thus, the second-order generalized integrator based PLL (SOGI-PLL) is superior over the above-described PLLs and gives fast and accurate frequency and phaseangle estimation under the adverse grid conditions. Instead of the estimated frequency signal from the SOGI-PLL feed-backed to the SOGI block structure, this frequency can be computed adaptively by the frequency-locked loop (FLL) structure, added in SOGI structure and combination is known as SOGI-FLL, to obtain excellent performance over the SOGI-PLL[76]. Instead of PLL, tan-arc phase-angle computation is used to compute the phase-angle and the adaptive feature of FLL improves performance [77]. Two SOGI blocks connected in parallel form a dual SOGI-FLL (DSOGI-FLL) structure, which can provide good transient response even in the presence of grid abnormalities (harmonics distortions, voltage imbalances, frequency changes, voltage imbalances). The performance of the DSOGI-FLL is analyzed in the presence of different grid voltage abnormalities. The DSOGI-FLL is not able to extract precise phase-angle in presence of DC-offset

## 3.1 Phase Lock Loop

Figure 3-1 depicts the components of a digitally implemented PLL, as shown in the block diagram: Relying on the PI controller and linear integration, the Loop Filter acts as a low-pass filter, while the Phase Detector is accomplished by means of the multiplier.



Figure 3-1: Phase lock loop block diagram[8]

The output of Phase detector is given as:

$$v_{pd} = V_{peak} \sin \theta * \cos \theta' = V_{peak} \sin(\omega t + \emptyset) * \cos(\omega' t + \emptyset')$$
$$= \frac{V_{peak}}{2} [\sin((\omega - \omega')t + (\emptyset - \emptyset')) + \sin((\omega + \omega')t + (\emptyset + \emptyset'))]$$
(3.1)

The phase error signal  $\varepsilon_{PD}$  can be expressed as follows:

$$\varepsilon_{\rm PD} = \frac{v_{\rm peak}}{2} K_{\rm pd} \left[ \underbrace{\sin((\omega - \omega')t + (\emptyset - \emptyset'))}_{\rm Low-frequency term} + \underbrace{\sin((\omega + \omega')t + (\emptyset + \emptyset'))}_{\rm high-frequency term} \right]$$
(3.2)

Due to the low-pass filter and VCO being tuned to input frequency i.e., $\omega \approx \omega'$ , the DC component of  $\varepsilon_{PD}$  signals is presented as an example.

$$\widetilde{\epsilon_{\rm PD}} = \frac{V_{\rm peak}}{2} K_{\rm pd} \sin(\emptyset - \emptyset')$$
(3.3)

Non-linear phase detection is the result of the sinusoidal function in equation (3.3). For phase detection purposes, however, when the  $\varepsilon_{PD}$  is extremely tiny, the output of the multiplier PD becomes linear in this way:  $\sin(\phi - \phi') \approx \sin(\theta - \theta') \approx (\theta - \theta')$ , and is supplied as a linear function of the phase error, expressed as:

$$\widetilde{\varepsilon_{\rm PD}} = \frac{V_{\rm peak}}{2} K_{\rm pd}(\theta - \theta') \tag{3.4}$$



Figure 3- 2 Phase lock loop Linearized block diagram in the complex frequency domain

Figure 3-2 illustrates the Laplace transformation being used to transform the above equation from the continues-time domain to the complex frequency domain. For the second-order transfer functions for PLL from the Figure 3-2, the H<sub> $\theta$ </sub>(s) the average frequency of VCO ( $\tilde{\omega}'$ ), and E<sub> $\theta$ </sub>(s) are expressed as functions:

$$H_{\theta}(s) = \frac{\theta'(s)}{\theta(s)} = \frac{K_{p}s + \frac{K_{p}}{T_{i}}}{s^{2} + K_{p}s + \frac{K_{p}}{T_{i}}} \qquad ; \qquad H_{\theta}(s) = \frac{2\zeta\omega_{n}s + \omega_{n}^{2}}{s^{2} + 2\zeta\omega_{n}s + \omega_{n}^{2}} \qquad (3.5)$$

$$E_{\theta}(s) = \frac{E_{pd}(s)}{\theta(s)} = \frac{s^2}{s^2 + K_p s + \frac{K_p}{T_i}} \qquad ; \qquad E_{\theta}(s) = \frac{s^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \qquad (3.6)$$

$$\widetilde{\omega}' = (\omega_0 + \Delta \,\widetilde{\omega}') = (\omega_0 + k_{vco} \widetilde{v_{lf}}) \tag{3.7}$$

Where  $\omega_0$  is the centre frequency of the VCO as a feed-forward,  $\omega_n = \sqrt{\frac{K_p}{T_i}}$ , and

$$\zeta = \frac{\sqrt{K_p T_i}}{2}.$$

Using the given frequency range, the signal's phase should be determined, as follows:  $\tilde{\theta}'(t) = \int \tilde{\omega}' dt = \int k_{vco} \tilde{v_{lf}} dt$ (3.8)

The output signal is sent back to the input side of the multiplier PD, which implies that the average output must be zero. It might be achieved by adjusting the center frequency to match the output signal's frequency. With two poles at origin, this form of system can track continual slope without having to deal with the steady-state error. The settling time of a second-order system may be estimated by the time it takes to settle within 1% of its steady state response for a given step input, and mathematically is describe as:

$$t_s = 4.6 \tau$$
 ; where  $\tau = \frac{1}{\xi \omega_n}$  (3.9)

Pull-in ranges  $\Delta \omega_p$  merely the frequency at which a PLL will always be locked into a stable state. A pull-in process begins after an input frequency change, and the time it takes for the PLL to achieve a locked state may be expressed as:

$$t_{\rm p} \approx \frac{\pi^2 \Delta \omega_{\rm in}^2}{16 \, \xi \omega_{\rm n}^3} \tag{3.10}$$

The bandwidth of PLL can be express as:

 $\omega_{-3dB} = \omega_n [1 + 2\xi^2 + \sqrt{(1 + 2\xi)^2 + 1}]^{\frac{1}{2}}$ (3.11) As demonstrated in Figure 3-2, the PLL in Figure 3-3 performs well with single phase grids at 50Hz with settling time  $t_s=100ms$  and  $\xi = 1/\sqrt{2}$ . At t = 150 ms, the frequency shifts from 50Hz to 45Hz and the phase angle from 0° to +45°. The grid frequency is quite close to the PLL cut-off frequency.

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Figure 3- 3 Step response of Phase lock loop

One restriction is that  $\omega_{in} - \omega_{vco}$  must be less than  $\omega_{p}$  and input signal frequency must be larger than the PLL bandwidth. Thus, higher frequency term of PD can be removed while examining PLL dominating dynamic response. As seen in equation (3.11), the PLL  $\omega_{-3dB} = 21.3$  Hz has a bandwidth close to the grid frequency, which is 50Hz. PLL locking results in a high frequency term in the phase-angle error ( $\varepsilon_{PD}$ ) of only twice the input frequency, which is 100Hz in this case For a single-phase grid-tied system, a PLL design based on an in-quadrature signal should be utilized in order to eliminate the 100Hz oscillation in the phase-angle error signal.



Figure 3- 4 Block diagram of PLL with quadrature signal generator and two phase detector

The in-quadrature phase detector of the PLL yields the phase-angle error signal  $\varepsilon_{PD}$ , which is given by

$$\epsilon_{PD} = V\{\sin(\omega t + \emptyset) * \cos(\omega' t + \emptyset') - \cos(\omega t + \emptyset) * \sin(\omega' t + \emptyset')\}$$
  
=  $V((\omega - \omega')t + (\emptyset - \emptyset')) = V\sin(\theta - \theta')$  (3.12)

A steady-state oscillatory term is not generated when the PLL is well-synchronized, as shown in equation (3.12). This implies that the PLL bandwidth may be increased and the aforesaid anomalies in the computation of PLL key parameters can be eliminated.

## 3.1.1 Synchronous Reference Frame based Phase Look Loop (SRF-PLL)

To implement a PLL for a three-phase system, there are typically two approaches to use it. The first approach is to utilize three single phase PLLs for each phase to extract the phase angles. This structure does not necessitate the conversion from 3phase abc space to dq space.



Figure 3- 5 Block diagram of SRF- PLL

The Clarke transformation (abc/ $\alpha\beta$ ) transforms the three-phase grid voltages  $v_{abc}$  into the stationary frame's two-phase voltage $v_{\alpha\beta}$ .

The accompanying voltage vector can be used to represent the transformation:

$$\mathbf{v}_{(\alpha\beta)} = \begin{bmatrix} \mathbf{v}_{\alpha} \\ \mathbf{v}_{\beta} \end{bmatrix} = \mathbf{V} \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix}$$
(3.13)

$$\mathbf{v}_{(\mathrm{dq})} = \begin{bmatrix} \mathrm{sin}\,\theta' & \cos\theta'\\ \mathrm{cos}\,\theta' & -\sin\theta' \end{bmatrix} \begin{bmatrix} \mathrm{V}\,\mathrm{sin}\,\theta\\ \mathrm{V}\,\cos\theta \end{bmatrix}$$
(3.14)

$$v_{d} = V \sin \theta \sin \theta' + V \cos \theta \cos \theta' = V \cos(\theta - \theta')$$
(3.15)



Figure 3- 6 Simulation results of SRF-PLL during Phase Jump of 90° at t=0.1 second


Figure 3- 7 Simulation results of SRF-PLL during voltage Imbalance of 10% on phase-B

The PI controller is used as a low-pass filter in the system. The low-pass filter accepts the q-axis component of grid voltage as an input (similarly as quadrature PLL in Figure 3-4), whereas the PI controller outputs the grid voltage angular speed. In order to accomplish dq axis decoupling, the PI controller adjusts the q-axis component of the grid voltage to zero, thus the grid voltage may be aligned with the d-axis and the q-axis component of the grid voltage to zero, thus the grid voltage may be aligned with the d-axis and the q-axis component of the grid voltage is eliminated. An integrator is then used to acquire the phase angle of the grid voltage. A high bandwidth for the SRF-PLL feedback mechanism is necessary to quickly and precisely detect the phase angle and amplitude of the grid voltage under ideal grid conditions(i.e. balanced grid voltages for three phase system), that is, when unbalances and harmonic distortion have no effect on the grid voltage. Figure 3-6 (a) shows 3-phase grid voltage in per unit (p.u.) measurement. Figure 3-6(b) shows alpha –beta voltage waveform in stationary frame in per unit (p.u.) measurement by applying Clark transformation. Figure 3-6 (c) shows direct- quadrature voltage waveform in synchronous reference frame in per unit (p.u.) measurement by applying Park transformation. Figure 3.6 (d)

& (e) show the output voltage signal of PLL locked with input voltage signal and

error signal from phase detector. Figure 3-6 depicts the response of an SRF-PLL tuned with a high gain, i.e. a wide bandwidth, to a 90° phase jump at t=0.1 second. By setting  $v_q$ = 0, as shown in Figure 3-5, the SRF-PLL instantaneously recognizes the balanced input voltage vector's amplitude and phase angle, virtually.When the grid voltage encountered a 10% voltage imbalance on phase B, the response of an SRF-PLL is depicted in Figure 3-7. The control loop bandwidth of this SRF-PLL was sufficiently high to make  $v_q \approx 0$ (Figure 3-7(c)), which means that the SRF-PLL could track the evolution of the unbalanced voltage vector applied to its input in real time. In this case, the measured phase angle causes oscillations to occur at a frequency twice as high as the input.



Figure 3-8: Simulation results of SRF-PLL during 5th Harmonic content in grid voltages (5%)

Figure 3-8 depicts the SRF-reaction PLL when a fifth-order harmonic is introduced to the three-phase voltage. As a result,  $v_q \neq 0$  occurs when the SRF-PLL commits an

error (Figure 3-8(d)) while tracking the current position of the input voltage vector. Using pre-filtering in PLL or a method that matches the d-axis average voltage to the amplitude of the fundamental voltage in the positive-sequence, PLL automatically eliminate the fifth-order harmonic effect on dq angular position. As a result, a little reduction in the PLL bandwidth increases its performance, almost eliminating the influence of high-order harmonics on PLL output signals.



Figure 3- 9 Simulation results of SRF-PLL during balanced voltage change (Voltage Sags and Dips)

As shown in Figure 3-9, an SRF-PLL tuned for high gain, or wide bandwidth, responds to the presence of a three-phase balanced sag. As illustrated in Figure 3-9, the SRF-PLL immediately identifies the amplitude and phase angle of the balanced input voltage vector by setting  $v_q = 0$  (Figure 3.9 (c)), virtually. It is not possible to

adequately analyze the positive-sequence component using typical filtering techniques to get the average value of  $v_d$ . SRF-PLL output signals may lead to a significant reduction in PLL bandwidth, as was previously discussed. A similar level of fifth harmonic distortion, as seen in Figure 3-8, affects the grid voltage. Figure 3-8(c) shows the oscillating error signal on both axes of the dq reference frame when the PLL is unable to instantaneously track the position of the fifth-order component. As a result, an average value of voltage on the d-axis (i.e.  $v_d$ ) may be computed using a simple low-pass filter with a cut-off frequency of 20 Hz. When synchronizing with three-phase voltages polluted by high-order harmonics, reducing the PLL bandwidth is an effective method to obtain high-quality signals at the SRF-PLL output. It is not viable to adequately analyze the positive-sequence component using traditional filtering methods to get the average value of v<sub>d</sub>.When synchronizing with three-phase voltages polluted by high-order harmonics, reducing the PLL bandwidth is an effective approach to generate high-quality signals at the SRF-PLL output, as shown in Figure 3-6, Figure 3-7, Figure 3-8, and Figure 3-9. However, the wind generating power station and PV power station use positive-sequence current injection at the fundamental frequency and eliminating injection of negativesequence and harmonic currents for avoiding power fluctuations which cause damage in the power converter or inserts unbalanced reactive currents for grid compensation at a point of common coupling. A grid-connected three-phase power converter's major responsibility is to correctly detect the positive sequence component at the fundamental frequency of three-phase grid voltage.

# 3.2 Decouple Double Synchronous Reference Frame PLL (DDSRFPLL)

On the basis of rotation at both positive and negative synchronous frequencies, this section proposes an enhanced three-phase synchronized PLL. Even under unbalanced grid fault conditions, accurate grid synchronization can be achieved by using a double-synchronous reference frame, which decouples negative-sequence voltage components from positive-sequence voltage components. Variations in the grid circumstances cause phase voltage imbalances. Unbalanced three phase systems can be reduced to two symmetrical systems with zero components: one revolving in the

positive direction called the positive sequence and the other reversing it, or in the opposite direction called negative sequence (Figure 3-10). Park and Clarke transform imbalanced voltages are examined in the following section.



Figure 3- 10: Voltage vectors of unbalanced three phase system

$$\mathbf{v} = \mathbf{v}_{abc}^{+1} + \mathbf{v}_{abc}^{-1} + \mathbf{v}_{abc}^{0} \tag{3.17}$$

$$v = V_{+1} \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t - \frac{4\pi}{3}) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(\omega t) \\ \cos(\omega t - \frac{2\pi}{3}) \\ \cos(\omega t - \frac{4\pi}{3}) \end{bmatrix} + V_0 \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$
(3.18)

The voltage vector on a stationary reference frame can be expressed using the Clark transformation with respect to the positive sequences:

$$v_{\alpha\beta} = V_{+1} \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-\omega t) \\ \sin(-\omega t) \end{bmatrix}$$
(3.19)

#### **3.2.1 Double Synchronous Reference Frame**

The unbalanced voltage vector's positive and negative sequence components are shown in Figure 3-11, along with a double synchronous reference frame (DSRF) composed of two rotating reference frames:  $dq_{+1}$ , rotating at a positive angular frequency(+ $\omega$ ) and with an angular position of  $+\theta_1$ , and  $dq_{-1}$ , rotating at a



negative angular frequency( $-\omega)$  and with an angular position of  $-\theta_1$  .

Figure 3-11: Voltage vector on stationary and synchronous reference frame

It has also been found that any negative sequence component occurs twice frequently on the positive sequence rotational frame axis and vice versa, using Park's transform.

$$V_{dq+} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \sin(-\omega t) & \cos(\omega t) \end{bmatrix} \times \begin{bmatrix} V_{+1} \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-\omega t) \\ \sin(-\omega t) \end{bmatrix} \end{bmatrix}$$

$$= \begin{bmatrix} V_{+1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{bmatrix} \end{bmatrix}$$

$$V_{dq-} = \begin{bmatrix} \cos(\omega t) & \sin(-\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \times \begin{bmatrix} V_{+1} \begin{bmatrix} \cos(\omega t) \\ \sin(\omega t) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-\omega t) \\ \sin(-\omega t) \end{bmatrix} \end{bmatrix}$$

$$(3.20)$$

$$= \begin{bmatrix} V_{+1} \begin{bmatrix} \cos(-2\omega t) \\ \sin(-2\omega t) \end{bmatrix} + V_{-1} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \end{bmatrix}$$

$$(3.21)$$

This results in estimated errors for the phase angle of grid, which must be considered while design a phase locked loop for three phase utility attached applications. The equations (3.20) and (3.21) demonstrate that the DC values upon that  $dq_+$  and  $dq_-$  frames correspond to the amplitudes of the sinusoidal signals  $V_{+1}$  and  $V_{-1}$ , respectively, and that the oscillations at  $2\omega$  represent the coupling between axes caused by the voltage vectors rotary in opposite directions. Rather than employing any filtering approach to attenuate oscillations at  $2\omega$ , the next section presents a decoupling network that totally cancels out the influence of these kinds of oscillations on the PLL synchronous reference frame voltages.

#### **3.2.2 Decoupling Network**

The decoupling network employed in the DSRF can be explained in general terms by assuming a voltage vector with two generic components revolving at  $+\omega t$  and  $+\omega t$  frequencies, respectively. Thus, the voltage vector is given by this generic voltage vector.



Figure 3-12: Voltage vector representation

It is clear from (3.20) and (3.21) that AC amplitudes in  $dq_+$  axes are directly proportional to DC amplitudes of signals in  $dq_-$  axes. Decoupling block can be designed to cancel out the oscillations generated by the negative sequence voltage vector(v\_)on  $dq_+$  axes signals after identifying the coupling terms between both reference frames, as shown in the Figure 3-12. As a further consideration, two rotating reference frames,  $dq_+$  and  $dq_-$  are examined. It is possible to represent the voltage vector as described as:

$$v = V_{+1} \begin{bmatrix} \cos(\omega t + \varphi_{+1}) \\ \cos(\omega t - \frac{2\pi}{3} + \varphi_{+1}) \\ \cos(\omega t - \frac{4\pi}{3} + \varphi_{+1}) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(\omega t + \varphi_{-1}) \\ \cos(\omega t - \frac{2\pi}{3} + \varphi_{-1}) \\ \cos(\omega t - \frac{4\pi}{3} + \varphi_{-1}) \end{bmatrix} + V_{0} \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}$$
(3.21)

The simplification of voltage vectors of DDSRF-PLL are represented as:

$$\begin{aligned} v_{\alpha\beta} &= \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = v_{\alpha\beta_{+1}} + v_{\alpha\beta_{-1}} \end{aligned} \tag{3.22} \\ &= V_{+1} \begin{bmatrix} \cos(\omega t + \varphi_{+1}) \\ \sin(\omega t + \varphi_{-1}) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-\omega t + \varphi_{+1}) \\ \sin(-\omega t + \varphi_{-1}) \end{bmatrix} \end{aligned} \tag{3.23} \\ v_{dq_{+}} &= \begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} = \begin{bmatrix} \bar{v}_{d+} \\ \bar{v}_{q+} \end{bmatrix} + \begin{bmatrix} \tilde{v}_{d+} \\ \bar{v}_{q+} \end{bmatrix} \end{aligned} \tag{3.23} \\ V_{dq_{+}} &= \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ \sin(-\omega t) & \cos(\omega t) \end{bmatrix} \times V_{+1} \begin{bmatrix} \cos(\omega t + \varphi_{+1}) \\ \sin(\omega t + \varphi_{-1}) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-\omega t + \varphi_{+1}) \\ \sin(-\omega t + \varphi_{-1}) \end{bmatrix} \end{aligned} \tag{3.24} \\ &= \begin{bmatrix} V_{+1} \begin{bmatrix} \cos(\varphi_{+1}) \\ \sin(\varphi_{+1}) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-\omega t + \varphi_{-1})\cos(\omega t) + \sin(-\omega t + \varphi_{-1})\sin(\omega t) \\ -\cos(-\omega t + \varphi_{-1})\sin(\omega t) + \sin(-\omega t + \varphi_{-1})\sin(\omega t) \end{bmatrix} \end{bmatrix} \end{aligned} \tag{3.25} \\ V_{dq_{+}} &= \begin{bmatrix} V_{+1} \begin{bmatrix} \cos(\varphi_{+1}) \\ \sin(\varphi_{+1}) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(-2\omega t + \varphi_{-1}) \\ \sin(-2\omega t + \varphi_{-1}) \end{bmatrix} \\ V_{dq_{+}} &= \begin{bmatrix} V_{+1} \begin{bmatrix} \cos(\varphi_{+1}) \\ \sin(\varphi_{+1}) \end{bmatrix} + V_{-1} \begin{bmatrix} \cos(\varphi_{-1})\cos(2\omega t) + \sin(\varphi_{-1})\sin(2\omega t) \\ \sin(\varphi_{-1})\cos(2\omega t) - \cos(\varphi_{-1})\sin(2\omega t) \end{bmatrix} \\ V_{dq_{+}} &= \begin{bmatrix} V_{+1} \begin{bmatrix} \cos(\varphi_{+1}) \\ \sin(\varphi_{+1}) \end{bmatrix} + V_{-1}\cos(\varphi_{-1}) \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} + V_{-1}\sin(\varphi_{-1}) \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \end{bmatrix} \end{aligned} \tag{3.26} \\ V_{dq_{+}} &= \begin{bmatrix} V_{+1} \begin{bmatrix} \cos(\varphi_{+1}) \\ \sin(\varphi_{+1}) \end{bmatrix} + V_{-1}\cos(\varphi_{-1}) \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} + V_{-1}\sin(\varphi_{-1}) \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \end{bmatrix} \end{aligned} \tag{3.26} \\ V_{dq_{+}} &= \begin{bmatrix} V_{-1} \begin{bmatrix} \cos(\varphi_{-1}) \\ \sin(\varphi_{-1}) \end{bmatrix} + V_{+1}\cos(\varphi_{-1}) \begin{bmatrix} \cos(2\omega t) \\ -\sin(2\omega t) \end{bmatrix} + V_{+1}\sin(\varphi_{-1}) \begin{bmatrix} \sin(2\omega t) \\ \cos(2\omega t) \end{bmatrix} \end{bmatrix}$$

$$v_{d+(decouple)} = v_{d+} - (v_{d-} \times \cos(2\omega t)) - (v_{q-} \times \sin(2\omega t))$$
 (3.28)

$$\mathbf{v}_{q+(\text{decouple})} = \mathbf{v}_{q+} + (\mathbf{v}_{d-} \times \sin(2\omega t)) + (\mathbf{v}_{q-} \times \cos(2\omega t))$$
(3.29)

#### **3.2.3** Mathematical analysis of DDSRF-PLL

To better comprehend the DDSRF's performance during unbalanced grid disturbances, this part will describe a more intuitive analysis on the complex-frequency domain, which has been previously presented in reference [17]. The dq<sub>+</sub> and dq<sub>-</sub> signals are re-written after rearranging equation (3.26) and equation (3.27).

$$\mathbf{v}_{dq+} = \begin{bmatrix} \mathbf{v}_{d+} \\ \mathbf{v}_{q+} \end{bmatrix} = \mathbf{V}_{+1} \begin{bmatrix} \cos\varphi_{+1} \\ \sin\varphi_{+1} \end{bmatrix} + \mathbf{V}_{-1} \begin{bmatrix} \cos(2\omega t) & \sin(2\omega t) \\ -\sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos\varphi_{-1} \\ \sin\varphi_{-1} \end{bmatrix}$$
(3.30)

$$\mathbf{v}_{dq-} = \begin{bmatrix} \mathbf{v}_{d-} \\ \mathbf{v}_{q-} \end{bmatrix} = \mathbf{V}_{-1} \begin{bmatrix} \cos\varphi_{-1} \\ \sin\varphi_{-1} \end{bmatrix} + \mathbf{V}_{+1} \begin{bmatrix} \cos(2\omega t) & -\sin(2\omega t) \\ \sin(2\omega t) & \cos(2\omega t) \end{bmatrix} \begin{bmatrix} \cos\varphi_{+1} \\ \sin\varphi_{+1} \end{bmatrix}$$
(3.31)

It is evident from these equations that the AC terms in the dq + axis arise as a result of a rotating transformation matrix at twice frequency having an effect on the DC terms in the dq –axes. It is possible to draw a similar result for AC signals in the reference frame of dq –.

Here, it is assumed that:

$$\left[\mathsf{M}(2\omega)_{\mathrm{dq}}\right] = \left[\mathsf{M}(-2\omega)_{\mathrm{dq}}\right]^{\mathrm{T}} = \begin{bmatrix}\cos(2\omega t) & -\sin(2\omega t)\\\sin(2\omega t) & \cos(2\omega t)\end{bmatrix}$$
(3.32)

Hence, substituting equation (3.32) into the equations (3.30) and (3.31) and simplified equations are expressed as:

$$\mathbf{v}_{dq+} = \begin{bmatrix} \mathbf{v}_{d+} \\ \mathbf{v}_{q+} \end{bmatrix} = \bar{\mathbf{v}}_{dq+} + \begin{bmatrix} \mathbf{M}(2\omega)_{dq} \end{bmatrix} \bar{\mathbf{v}}_{dq-}$$
(3.33)

$$v_{dq-} = \begin{bmatrix} v_{d-} \\ v_{q-} \end{bmatrix} = \bar{v}_{dq-} + \left[ M(-2\omega)_{dq} \right] \bar{v}_{dq+}$$
(3.34)

It corresponds to the amplitude of sequence components given to the DDSRF's input signal. In this manner, equations (3.33) and (3.34) demonstrate that the interrelationship between signals on the positive and negative coordinate systems is described by the equation.

Here,  $v_{dq+}$  and  $v_{dq-}$  are derived as:

$$\bar{\mathbf{v}}_{dq+} = \begin{bmatrix} \bar{\mathbf{v}}_{d+} \\ \bar{\mathbf{v}}_{q+} \end{bmatrix} = \mathbf{V}_{+1} \begin{bmatrix} \cos\varphi_{+1} \\ \sin\varphi_{+1} \end{bmatrix}$$
(3.35)

$$\mathbf{v}_{dq-} = \begin{bmatrix} \mathbf{v}_{d-} \\ \mathbf{v}_{q-} \end{bmatrix} = \mathbf{V}_{-1} \begin{bmatrix} \cos \varphi_{-1} \\ \sin \varphi_{-1} \end{bmatrix}$$
(3.36)

Here, equations (3.33) and (3.34) are rearranged as:

$$\bar{v}_{dq+} = (v_{dq+}) - [M(2\omega)_{dq}]\bar{v}_{dq-}$$
(3.37)

$$\bar{v}_{dq-} = (v_{dq-}) - \left[ M(-2\omega)_{dq} \right] \bar{v}_{dq+}$$
(3.38)

Therefore, the computed component at the DDSRF's output can be expressed as follows:

$$\overline{v^*}_{dq+} = [K_{\text{filter}}]\{(v_{dq+}) - [M(2\omega)_{dq}]\overline{v^*}_{dq-}\}$$
(3.39)

$$\overline{v^*}_{dq-} = [K_{\text{filter}}]\{(v_{dq-}) - [M(-2\omega)_{dq}]\overline{v^*}_{dq+}\}$$
(3.40)

Here, [K<sub>filter</sub>] is nothing but either low-pass filter or moving average filter and transfer function of low-pass filter is defined as:

$$[K_{\text{filter}}] = \begin{bmatrix} \frac{\omega_{\text{k}}}{s + \omega_{\text{k}}} & 0\\ 0 & \frac{\omega_{\text{k}}}{s + \omega_{\text{k}}} \end{bmatrix}$$
(3.41)

As a result, by substituting equation (3.32)and(3.41) into (3.35), it can be rewritten as  $\overline{v^*}_{dq+} = [K_{filter}]\{(v_{dq+}) - ([M(2\omega)_{dq}][K_{filter}]\{(v_{dq-}) - [M(-2\omega)_{dq}]\overline{v^*}_{dq+}\})\}$  (3.42) By applying  $v_{dq-} = [M(-2\omega)_{dq}]v_{dq+}$  and  $v_{dq+} = [M(2\omega)_{dq}]v_{dq-}$  in equation (3.42), it is re-written as:

$$\overline{v^{*}}_{dq+} = [K_{filter}] (v_{dq+} - \{ [M(2\omega)_{dq}] [K_{filter}] \{ [M(-2\omega)_{dq}] v_{dq+} - [M(-2\omega)_{dq}] \overline{v^{*}}_{dq+} \} )$$
(3.43)

$$\overline{v^*}_{dq+} = [K_{\text{filter}}] \times (v_{dq+} - \{ [M(2\omega)_{dq}] [K_{\text{filter}}] [M(-2\omega)_{dq}] \times \{ v_{dq+} - \overline{v^*}_{dq+} \} \}$$

$$(3.44)$$

For the simplicity,

$$[K] = \left[ M(2\omega)_{dq} \right] [K_{filter}] \left[ M(-2\omega)_{dq} \right]$$
  
$$= \frac{1}{2} \begin{bmatrix} \frac{\omega_{k}(s+\omega_{k})}{s^{2}+2s\omega_{k}+\omega_{k}^{2}+(2\omega)^{2}} & \frac{\omega_{k}\omega}{s^{2}+2s\omega_{k}+\omega_{k}^{2}+(2\omega)^{2}} \\ \frac{\omega_{k}\omega}{s^{2}+2s\omega_{k}+\omega_{k}^{2}+(2\omega)^{2}} & \frac{\omega_{k}(s+\omega_{k})}{s^{2}+2s\omega_{k}+\omega_{k}^{2}+(2\omega)^{2}} \end{bmatrix}$$
(3.45)

Equation (3.45) is re-written as:

$$\overline{v^*}_{dq+} = [K_{filter}] \times (v_{dq+} - \{[K] \times \{v_{dq+} - \overline{v^*}_{dq+}\})$$
(3.46)

The computed positive sequence component is describe as

$$\overline{v^*}_{dq+} = (\{ [I] - [K][K_{filter}]\}^{-1} \times [K_{filter}] \{ [I] - [K] \} )v_{dq+}$$
(3.47)

The transfer function is expressed as:

$$\frac{\overline{\mathbf{v}^*}_{dq+}}{\mathbf{v}_{dq+}} = \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ -\mathbf{B} & \mathbf{A} \end{bmatrix}$$
(3.48)

Here A and B are derived as:



Figure 3- 13: Dynamic performance of DDSRF-PLL during balanced grid voltages, unbalanced in phase B of grid voltages, and distorted grid voltages

Figure 3-13 indicates the dynamic performance of DDSRF-PLL during balanced grid voltages till t = 0.1 second, further encounter to unbalance in Phase –B of grid voltages from t = 0.1 seconds to t = 0.2 seconds, and further balance grid voltages distorted by harmonics from 0.2 seconds to t = 0.3 seconds. The DDSRF-LL is used to extract phase-angle as well as positive sequences i.e.  $v_{\alpha}^{+},\,v_{\beta}^{+}$  (Figure 3-13 (b)) and both are used to generate  $v_d$  and  $v_q$  (see Figure 3-13 (c)) for the control system of grid connected system. Figure 3.13(d) shows phase-A of grid voltages and ac voltage generated using extracted phase- angle. The error signal is generated by computing difference between zeros and  $v_q^+$  or multiplying gain of -1 to  $v_q^+$  signal as per convenience. Figure 3-14 indicates the dynamic performance of DDSRF-PLL during balanced grid voltages till t = 0.1 second, further encounter to unbalance (i.e. swell) in Phase -B of grid voltages as well as distortion in grid voltages from t= 0.1 seconds to t =0.2 seconds, and further unbalance (i.e. sag) in phase-B of grid voltages distorted by harmonics from 0.2 seconds to t =0.3 seconds. The DDSRF-PLL is used to extract phase-angle as well as positive sequences i.e.  $v_{\alpha}^{+},\,v_{\beta}^{+}$  (Figure 3-14 (b)) and both are used to generate  $v_d$  and  $v_q$  (Figure 3-14 (c)) for the control system of grid connected system. To get a negative-sequence component and its transfer function, just transpose the matrix indicated in (3.48), similarly as for a positive-sequence DDSRF. Because it is a sequence separator, the DDSRF may be used to manage voltage and/or current in three-phase systems during unbalanced grid disturbances, making it a particularly useful for the control technique. The cut-off frequency ( $\omega_k$ ) of the low-pass filter is chosen at design time to achieve desired system performance. Setting  $\omega_k = \omega/\sqrt{2}$  rad/s [17] provides an acceptable balance between temporal responsiveness and damping. An effective synchronization technique for three-phase power converter controllers, especially if they have low-voltage ride-through capabilities under unbalanced grid failures, can be achieved using the DDSRF-PLL. However, resonant controllers can also be used to create power converter controllers on the stationary reference frame. The most essential synchronization variable in this scenario is the grid frequency, not the grid voltage phase angle. As the grid frequency is a more stable variable than the grid phase angle, it is logical to assume that grid fault controllers based on grid frequency detection will show a more robust performance. Adaptive filters functioning with a stationary reference frame are used

in the next section i.e. second order generalized integrator –frequency lock loop to demonstrate a synchronization system suited for use with resonant controllers for three-phase converters.



Figure 3- 14: Dynamic performance of DDSRF-PLL during balanced grid voltages, and unbalanced in phase B of distorted grid voltages

# 3.3 Dual Second-order generalized Integrator-FLL(DSOGI-FLL)

Our interest here is on a widely used enhanced PLL known as a DSOGI-PLL (dual second-order generalized integrator-phase locked loop). The DSOGI-PLL can be seen as a combo of the DSOGI and the traditional SRF-PLL entities to some extent.

In order to avoid the negative and harmonic sequence during phase-angle extraction, 63 | P a g e its primary principle of good performance against unbalanced grid voltage and harmonic distortion is able to deliver the pure, balanced, and sinusoidal grid voltage into the traditional SRF-PLL.

#### 3.3.1 Second-Order Generalized Integrator (SOGI)

The second-order generalized integrator (SOGI), whose schematic diagram is illustrated in Figure 3-15, must be introduced before the DSOGI-PLL can be described. The structure of SOGI, as depicted in Figure 3-15, and the transfer function of SOGI in equations (3.49) and (3.50) are two imaginary complex conjugated poles located at  $\pm j\omega_0$  that functioned like a resonator oscillating at angular frequency  $\omega_0$ .





Figure 3- 15: (a) Basic structure of Second-order generalized integrator<sup>[11]</sup>, (b) Bode diagram of transfer function (Y(s) / Vin (s))and (Y'(s) / Vin (s))of SOGI, and (c) Step response of SOGI

The transfer functions of SOGI from the Figure 3-15(a) are written as:

$$\frac{Y(s)}{v_{in}(s)} = \frac{\omega_0/s}{1 + \frac{\omega_0\omega_0}{s-s}} = \frac{s\,\omega_0}{s^2 + \omega_0^2}$$
(3.49)

$$\frac{Y'(s)}{v_{in}(s)} = \frac{Y'(s)}{Y(s)} * \frac{Y(s)}{v_{in}(s)} = \frac{\omega_0}{s} * \frac{s\,\omega_0}{s^2 + \omega_0^2} = \frac{\omega_0^2}{s^2 + \omega_0^2}$$
(3.50)

The step response of the SOGI is given as:

$$y(t) = L^{-1}[Y(s)] = L^{-1} \left[ \frac{s \,\omega_0}{s^2 + \,\omega_0^2} * v_{in}(s) \right]$$

$$= L^{-1} \left[ \frac{s \,\omega_0}{s^2 + \,\omega_0^2} * \frac{\omega_0}{s^2 + \,\omega_0^2} \right] = \frac{1}{2} [t \,\omega_0 \sin \omega_0 t]$$

$$y'(t) = L^{-1}[Y'(s)] = \frac{1}{2} [\sin \omega_0 t \, t \,\omega_0 \cos \omega_0 t]$$
(3.52)

Figure 3-15 (c) depicts the step time response of a SOGI structure as a function of equations (3.51) and (3.52). In the presence of a unitary step, the amplitude of the output signals increases, resulting in an unstable system. Weighted k of the difference between grid voltage  $v_{in}(s)$  and unity feedback of output signal Y(s), illustrated in Figure 3-16(a) is used to modify the input to the SOGI structure in order to prevent the system from being unstable.



Figure 3-16 :(a) Block diagram of SOGI-OSG, (b) Bode Diagram of  $D_v(s)$ , and (c) Bode Diagram of  $Q_v(s)$  with different value of k

The transfer functions for  $D_v(s)$  and  $Q_v(s)$  are rewritten as:

$$D_{v}(s) = \frac{Y(s)}{v_{in}(s)} = \frac{k s \omega_{0}}{s^{2} + k \omega_{0} s + \omega_{0}^{2}}$$
(3.53)

$$Q_{v}(s) = \frac{Y'(s)}{v_{in}(s)} = \frac{k \, s \, \omega_{0}}{s^{2} + k \omega_{0} s + \omega_{0}^{2}}$$
(3.54)

Figure 3-16 (b) indicates the band-pass equivalent nature of the output Y(s) and the low-pass similar nature of the output Y'(s)(Figure 3-16 (c)), while the phase responses of curves at 50Hz suggest that Y(s) is having a 90° phase lead to Y'(s). Furthermore, Bode's magnitude responses retain 0 dB level at the fundamental frequency of 50 Hz while decreasing the amplitude at the 5<sup>th</sup> and 7<sup>th</sup> harmonics harmonic frequencies of 250 Hz and 350 Hz, respectively. A second-order band-pass

filter is shown in Figure.3-16(b) to be capable of extracting only the fundamental components of utility grid yet rejecting harmonics.

#### 3.3.2 Frequency Lock Loop (FLL)

However, SOGI has an intrinsic resonant nature that may be employed as a voltagecontrolled oscillator, which stresses to create a simple and reliable single feedback control loop for an auto-adapting center frequency of SOGI resonator as per the input grid frequency.



Figure 3-17: (a) Block diagram of SOGI-FLL, and (b) the Bode diagram of transfer functions,  $E_v(s)$  and  $Q_v(s)$ (dotted line shows the SOGI resonance frequency ( $\omega'$ ))

Figure 3-17 shows a simple and reliable extension of the SOGI structure, which is Frequency Locked Loop, (FLL). The voltage error signal  $E_v$  (s), which is nothing but the difference between input  $v_{in}$  (s) and output Y(s) and behave as a notch filter with zero dB gain and a 180° phase-angle jump at the center frequency as observed from a bode diagram in the Figure 3-16, must be taken into consideration in order to make an auto-tunable SOGI-Quadrature Signal Generator (QSG) for single phase grid tied inverter.

#### GRID SYNCHRONIZATION FOR THREE-PHASE GRID TIED CONVERTER

Transfer function is expressed as:

$$E_{v}(s) = \frac{\varepsilon_{v(s)}}{v_{in(s)}} = \frac{s^{2} + \omega_{0}^{2}}{s^{2} + k\omega_{0}s + \omega_{0}^{2}}$$
(3.50)

The transfer function of  $E_v$  (s) and  $Q_v$  (s) gives worthy information for auto-tunable frequency control system by taking common bode diagram of transfer function  $E_v$  (s) and  $Q_v$  (s), as depicted in Figure.3-17(b). The Bode diagram of transfer functions,  $E_v$  (s) and  $Q_v$  (s), reveal that the signals  $E_v$  (s) and  $Q_v$  (s) are in a phase when input frequency ( $\omega$ ) is lower than SOGI resonance frequency ( $\omega'$ ) i.e.  $\omega < \omega'$ and out of a phase (180° phase difference) when  $\omega > \omega'$ , as indicated in the Figure.3-17(b).

Hence, a frequency error variable is derived from product of  $E_v(s)$  and  $Q_v(s)$ , which remain positive when input frequency is lower than SOGI resonance frequency ( $\omega'$ ), and remain negative  $\omega > \omega'$  in the SOGI-FLL. Moreover, the frequency-locking loop can be designed using frequency error variable,  $\varepsilon_f$  and a negative value of frequency loop controller gain,  $-\gamma$  as shown in Figure 3-17 (a). The frequency loop controller gain is used to achieve DC component of frequency error variable  $\epsilon_f$  equal to zero by changing SOGI resonance frequency,  $\omega',$  until equal to the input frequency,  $\omega$ . A feed-forward variable,  $\omega_c$  i.e. nominal value of grid frequency is provided in frequency locking loop to speed up the initial synchronization process. The SOGI-QSG and Frequency locking loop combined structure diagram known as SOGI-FLL for single-phase grid synchronization system, as shown in Figure 3-17. The transient and steady state behavior of the SOGI –FLL mainly depends on a suitable value chosen for control parameters y and k in order to obtain desired response in the estimation of the frequency and amplitude of input signal. Figure 3-16 shows two different transfer functions, k=0.1 and  $\omega$ =100 $\pi$ rad/s, which we can consider second-order band-pass filters that can only retrieve AC signals propagating at the fundamental angular speed while excluding all other AC harmonics (for example, the fifth and seventh harmonic components). It is possible to eliminate harmonics by using a single SOGI for three phase system, and also generate quadrature signal for single phase system only, but the negative sequence will remain present in three phase system during abnormity in grid. Instead of single

SOGI,  $v_{\alpha}$  and  $v_{\beta}$  signal applied to the two separate SOGI for the both signal. To eliminate harmonics and negative sequence from the  $v_{\alpha}$  and  $v_{\beta}$  signal, two SOGI are used independently to form the direct/quadrature signal for  $v_{\alpha}$  and  $v_{\beta}$ , which is referred to as the Dual-Second Order generalized integrator.



Figure 3-18: Schematic diagrams of the Dual SOGI and phase-angle computation

The functional diagram shown in Figure 3-18 illustrates a dual-second order generalized integrator (DSOGI) in association with a frequency lock loop (FLL) and tangent-based phase-angle computation block. Figure 3-19 depicts a four-phasor diagram, with the first and second phasor diagrams representing the positive direct/quadrature components of  $v_{\alpha}$  and  $v_{\beta}$ , respectively, and the third and fourth

phasor diagrams representing the negative direct/quadrature components of  $v_{\alpha}$  and  $v_{\beta}$ , respectively.



Figure 3-19:Phasor diagram of direct/quadrature components of  $v_{\alpha}$  and  $v_{\beta}$  grid voltage

As seen in Figure 3-16, the direct component is 90° phase leading phase leading in relation to the quadrature components, whereas the negative component rotates in the opposite direction of -50Hz.

From Figure 3-18 and Figure 3-19, following result are obtained ( $v'_{\alpha+} = (-qv'_{\beta+})$ and  $v'_{\beta+} = (-qv'_{\alpha+})$ ) as:

$$v'_{\alpha} - qv'_{\beta} = (v'_{\alpha+} + v'_{\alpha-}) - (qv'_{\beta+} + qv'_{\beta-}) = v'_{\alpha+} - qv'_{\beta+} = 2v'_{\alpha+}$$
(3.51)

$$qv'_{\alpha} + v'_{\beta} = (qv'_{\alpha+} + qv'_{\alpha-}) + (v'_{\beta+} + v'_{\beta-}) = qv'_{\alpha+} - qv'_{\beta+} = 2v'_{\beta}$$
(3.52)

$$\varepsilon_{\rm f} = \frac{\varepsilon_{\rm f(\alpha)} + \varepsilon_{\rm f(\beta)}}{2} = \frac{1}{2} (\varepsilon_{\alpha} q v_{\alpha}' + \varepsilon_{\beta} q v_{\beta}') \tag{3.53}$$

In SOGI-QSG, a frequency adaptive FLL is included to achieve grid synchronization in a changing frequency environment. Additionally, the normalized gain of the FLL is calculated by dividing the amplitude of positive sequence components by two, i.e.  $(v_{\alpha}^{+})^{2} + (v_{\beta}^{+})^{2}$ , in order to linearize the frequency lock loop response. While technically valid, the usage of two separate FLLs in the DSOGI-FLL may seem unusual conceptually due to the fact that its two input signals have the same frequency. Due to the fact that both inputs,  $v_{\alpha}$  and  $v_{\beta}$ , have the same frequency, the DSOGI employs a single FLL (Figure 3-18) in which the frequency error signals created by calculating an average error signal, i.e.  $\varepsilon_{f(\alpha)}$  and  $\varepsilon_{f(\beta)}$  of the QSGs, have been combined in the equation (3.53). The state-space equations of DSOGI can be written as:

$$\begin{bmatrix} v_{\alpha}^{+} \\ v_{\beta}^{+} \end{bmatrix} = \frac{1}{2} * \begin{bmatrix} D(s) & -Q(s) \\ Q(s) & D(s) \end{bmatrix} \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} = \frac{1}{2} * \frac{k \times \omega'}{s^{2} + k \times \omega' \times s + \omega'^{2}} \begin{bmatrix} s & -\omega' \\ -\omega' & s \end{bmatrix} \begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix}$$
(3.54)

The frequency response of the DSOGI can be described as

$$\begin{bmatrix} \mathbf{v}_{\alpha}^{+} \\ \mathbf{v}_{\beta}^{+} \end{bmatrix} = \frac{1}{2} * \frac{\mathbf{k} \times \omega'}{\mathbf{k} \times \omega \times \omega' - \mathbf{j}(\omega^{2} + \omega'^{2})} \begin{bmatrix} \mathbf{j}\omega & -\omega' \\ -\omega' & \mathbf{j}\omega \end{bmatrix} \begin{bmatrix} \mathbf{v}_{\alpha} \\ \mathbf{v}_{\beta} \end{bmatrix}$$
(3.55)

Assuming balanced positive-sequence voltage vector at the grid frequency, steadystate analysis gives following relationship:

$$\mathbf{v}_{\boldsymbol{\beta}}(\mathbf{s}) = -\mathbf{j} \, \mathbf{v}_{\boldsymbol{\alpha}} \, (\mathbf{s}) \tag{3.56}$$

Hence, the Steady-state frequency response of the DSOGI is re-written as:

$$\begin{bmatrix} \mathbf{v}_{\alpha}^{+} \\ \mathbf{v}_{\beta}^{+} \end{bmatrix} = \frac{1}{2} * \frac{\mathbf{k} \times \boldsymbol{\omega}'(\boldsymbol{\omega}' + \boldsymbol{\omega})}{\mathbf{k} \times \boldsymbol{\omega} \times \boldsymbol{\omega}' - \mathbf{j}(\boldsymbol{\omega}^{2} + \boldsymbol{\omega}'^{2})} \begin{bmatrix} \mathbf{v}_{\alpha} \\ \mathbf{v}_{\beta} \end{bmatrix}$$
(3.57)

The transfer functions gives the relation between the amplitude of the positive sequence component detected by the DSOGI and the actual amplitude of a given positive sequence voltage vector applied to its input. The transfer function  $\frac{|v_{\alpha\beta}^+|}{|v_{\alpha\beta}^-|}$  obtained by substituting  $\omega$  by  $-\omega$ . The bode plot of transfer function is shown in Figure 3-20.



Figure 3-20: Bode plot of transfer functions  $\frac{|v_{\alpha\beta}^+|'}{|v_{\alpha\beta}^+|}$  and  $\frac{|v_{\alpha\beta}^+|'}{|v_{\alpha\beta}^-|}$  in the Dual-SOGI



Figure 3-21 :Step response of Frequency Estimation (a) different value of k , constant value  $\gamma$ =5000, (b) different value of k ,constant value  $\gamma$ =10000, (c) different value of  $\gamma$  ,constant value k=1, and (d) different value of  $\gamma$  ,constant value k=0.5

In spite of this, it is difficult to determine the advantages and disadvantages of these structures, particularly in contrast with the SOGI-FLL and high-order PLLs. The high-order PLLs and FLLs knowledge provides fast and accurate phase angle extraction by paying cost of hardware implementation complexity. Using a -5 Hz frequency step change (i.e. frequency leap (50Hz to 45Hz) and phase angle shift (0<sup>0</sup> to45<sup>0</sup>) at 200msec, the dynamic performance of frequency estimation in SOGI-FLL is investigated. The starting frequency value, i.e.  $2\pi * 50$ , is used as the feed-forward value. The dynamic response of frequency estimation is observed in the Figures 3-21 (a) and (b) by taking a progressive value of k and a constant value of  $\gamma$ , while the dynamic response of frequency estimation is observed by taking a progressive value of  $\gamma$  and a constant value of k, as depicted in the Figures 3-21(c) and (d). The table 3-1 contains the results of an impact study of the parameters k and  $\gamma$  in SOGI-FLL based on the Figures 3-21 (a)-(d) of the figure. Amplification of the signal ( $\varepsilon_v$ ) is accomplished by the use of the parameter k, which has an effect on the transient responsiveness and bandwidth of SOGI-FLL. A good signal filtering performance

and a dynamic response of the system are compromised while choosing the gain k for the system (Figure.3-17 & Figure 3-21). It is necessary to choose a value that represents a trade-off between the precision of frequency estimate and the dynamics of SOGI-FLL.

Parameter	Progressive change	Transient response	Steady-state response	Filtering	Settling Time
k	Increasing	Good	Good	Good	Reduce
	Decreasing	Poor	Poor	Poor	Increase
γ	Increasing	Poor	moderate	No effect	Reduce
	Decreasing	Good	Good	No effect	Increase

Table 3-1: Impact Analysis of SOGI-FLL

The applicability of DSOGI-FLL is demonstrated by simulation results obtained in the MATLAB/Simulink programming environment. These are the control variables that are utilized in the simulation model: k=1,  $\gamma=-2000$ . To achieve the simulation findings, four situations were considered, which are as follows: (i) balanced grid voltages; (ii) unbalanced sag in grid voltage; (iii) unbalanced swell in grid voltage; and (iv) harmonic distorted grid voltage. Figure 3-22 (a) depicts the situation I in which balanced three phase grid voltages are provided to DSOGI-FLL for a period of time equal to 0.1 seconds. Following that, voltage sag and swell are introduced into the phase A of grid voltage from t = 0.1 seconds to t = 0.15 seconds and from t = 0.15 seconds to t=2.0 seconds, respectively, in the phase A of grid voltages. This block is critical in the design and implementation of a control system for a grid-connected converter because it allows the converter to be synchronized with the grid. The  $v_d$  and  $v_q$  are generated for the control system of grid-connected systems using the dq-abc transformation and DSOGI-FLL, which is employed to extract phase-angle as well as positive sequences, i.e.  $v_{\alpha}^{+}$  and  $v_{\beta}^{+},$  and both are utilised to generate  $v_d$  and  $v_q$  for the control system of grid-connected systems. DSOGI-band-pass FLL filtering capabilities are demonstrated in Figure 3-22(b), which depicts positive sequences of grid voltages ( $v_{\alpha}^{+}$  and  $v_{\beta}^{+},$  FLL) that are devoid of the effects of sag, swell, and harmonics distortion, and which also confirms the

band-pass filtering capabilities of DSOGI-FLL. Figure 3-22(c) depicts the synchronism of grid voltages and phase-angle retrieved using DSOGI-FLL when all simulation situations are taken into consideration.



Figure 3-22. Simulation result of grid connected PV inverter using dual-SOGI-FLL :(a)PCC voltages with grid abnormalities,(b)positive component of stationary frame voltages, (c)comparative results of phase-angle and PCC voltages, and (d)frequency extraction

According to Figure 3-22 (d), the transient response of estimated frequency in DSOGI-FLL does not show any fluctuation or minimum change at the time in which either sag or swell encounter in the three-phase voltages and swiftly settles down to the desired value after settling down to the desired value. Figure 3-23 gives the comparative analysis of frequency extraction of different grid synchronization techniques when subjected frequency shifted from 50Hz to 45 Hz at the t= 0.25 seconds. The dynamic parameters are chosen for analysis as follow:  $\omega_n = 2\pi 50$  rad/s,  $\zeta = 0.707$ . Table 3-2 presents settling time of frequency extraction, negative Sequence Components detection, and harmonics detection for the different grid

synchronization techniques. Hence, DSOGI-FLL gives superior performance over the other grid synchronization techniques.



Figure 3-23: Time responses of frequency extraction in different grid synchronization techniques

Different grid	Observed	Negative	Harmonics	
synchronization	Time	Sequence	Detection	
techniques	(ms)	Components		
		detection		
SRF-PLL	60	NO	NO	
SOGI-FLL	54	NO	YES	
DDSRF-PLL	50	YES	Required	
			decoupling	
			term	
DSOGI-PLL	50	YES	YES	
DSOGI-FLL	35	YES	YES	

 Table 3-2: Time response of frequency extraction and performance

 assessment of different grid synchronization techniques.

An FLL is used to adaptively obtain frequencies in SOGI-FLL, whereas the SOGI-PLL uses a SOGI-OSG block to provide feedback on the estimated frequency [6]. [15-18]. When the power grid fails, a DC-offset is produced by a variety of factors, including transformer nonlinearity, A/D converter error, abnormal temperature in

analogue devices, and zero drift[7-8]. The DC-offset in SRF-PLL can be reduced using a variety of methods. Cascaded-SOGI-PLL was recommended in the article [9] as a way to eliminate the DC quantity, although it has several drawbacks, such as segregation. The DC-offset in SRF-PLL can be reduced in a number of methods, including a cascaded SOGI-PLL, which uses many SOGI structures, although the additional computational cost is significant [10]. Cascade delay signal cancellation PLL (CDSC-PLL) and adaptive filter delay signal cancellation-PLL (APF-DSC-PLL) techniques were devised by the authors of an article [10] and an article [11], respectively, to speed up DC-offset removal. However, the complex structure of the system reduces the dynamic performance of the system. It was also reported in an article [12] that a PLL using modified delay signal cancellation-PLL can improve dynamic performance by minimizing DC-offset but requires design modification. As well as five more methods for removing the DC-offset in the PLL (NF) based on PLL and dq-DSC-PLL. However, the dynamic performance of these phase detection approaches is sluggish (articles [13-15]). While conventional low-pass filters have their limitations, these new techniques have the potential to improve dynamic performance while overcoming those drawbacks. Even so, the process of selecting and calculating the sliding window's width might be time-consuming. For singlephase or three-phase systems, a modified SOGI-FLL (MSOGI-FLL) is recommended to reduce frequency estimate errors due to DC quantity and other grid irregularities. Consequently (e.g. harmonics, frequency fluctuation, magnitude variation), MSOGI-FLL estimates the DC-offset by using the third integrator as a DC-offset cancellation block, which does not affect frequency estimation in the FLL. Under various circumstances, it is described how the MSOGI-FLL gives superior performance over other higher ordered FLL or PLL techniques without increasing computation burden.

#### 3.3.2.1 DC-offset effect in SOGI-FLL

A DC-offset is produced by a variety of factors, including transformer nonlinearity, A/D converter error, and nonlinearity of op-amp in current or voltage sensor circuitry, abnormal temperature in analogue devices, and zero drift. One of the phase voltages of three phase system or alpha or beta voltage component including DC-offset, which has amplitude  $V_0$  are expressed as:

$$v_{in}(t) \{ \operatorname{orv}_{\alpha}(t) \operatorname{orv}_{\beta}(t) \} = V_0 u(t) + V_1 \sin \omega t$$
(3.58)

The frequency transformation of the equation (3.58) can be described as:

$$v_{in}(s) = \frac{V_0}{s} + \frac{V_1\omega}{s^2 + \omega^2} = \frac{V_0\left(s + \frac{V_1}{V_0}\omega + \frac{\omega^2}{s}\right)}{s^2 + \omega^2}$$
(3.59)

From the block diagram of SOGI-FLL and equation (3.50), transfer function of error signal in SOGI-FLL can be expressed as:

$$\frac{E_{v}(s)}{v_{in}(s)} = \frac{s^2 + \omega^2}{s^2 + k\omega s + \omega^2}$$
(3.60)

$$E_{v}(s) = \frac{s^{2} + \omega^{2}}{s^{2} + k\omega s + \omega^{2}} v_{in}(s) = \frac{s^{2} + \omega^{2}}{s^{2} + k\omega s + \omega^{2}} \frac{V_{0}\left(s + \frac{V_{1}}{V_{0}}\omega + \frac{\omega^{2}}{s}\right)}{s^{2} + \omega^{2}}$$
(3.61)

$$= \frac{s^2 + \omega^2}{s^2 + k\omega s + \omega^2} \frac{V_0 \times \frac{1}{s} \times \left(s^2 + \frac{V_1}{V_0} \omega s + \frac{\omega^2}{s}\right)}{s^2 + \omega^2} = \frac{V_0}{s}$$
  
The error signal in time domain can describe as:  
 $e_v(t) = V_0 u(t)$  (3.62)

As a parameter of the resonance frequency, the SOGI system has to be constantly updated to keep it in sync. Continuous-to-discrete transformations in practical applications are required for the real-time calculation of coefficients. A major drawback of SOGI-FLL is that it is unstable if the input signal has a DC component. A high-pass filter should be applied to the input signal to eliminate DC-offset.

#### **3.3.3** DC-offset due to Analog to Digital Conversion (ADC)

The DC-offset presents due to the analog to digital conversion(ADCs) and signal conditioning and the SOGI structure is inefficient to eliminate the DC-offset as observed from the bode diagram, shown in Figure 3-16(b). Bode diagram of the SOGI presents the inability to attenuate low-frequency components especially the dc signal from the grid voltage. It is very well common that integration of DC value yields step signal, further integration produces a ramp signal. Because of the analogue to digital conversion (ADCs) and signal conditioning, a DC-offset is introduced, and the SOGI structure is inefficient in eliminating the DC-offset, as per the previous derivation and equation (3.62). Because of this inability to attenuate low-frequency components, particularly DC signals from the grid voltage, the SOGI's Bode curve is shown in Figure 3-16. The existence of a DC-offset in the measured grid voltage degrades the performance of a SOGI by reducing its efficiency. The conversion of a continuous-time input signal into digital values results in the generation of an error, which is referred to as the quantization error.

This error occurs as a result of the ADC conversion process increasing the number of digits in the input signal by a set number of digits. If a normalized sinusoidal signal (i.e., one whose amplitude changes between +1 and -1) is to be converted into a digital ADC, (b+1) bits, including sign bits, must be used in the conversion. The number of levels and the size of the quantization step are  $2^{b+1}$  and  $\frac{2}{2^{b+1}} = 2^{-b}$  for the b+1 level, respectively. The quantization error is caused by rounding, which is the process of reducing the size of a binary number with a finite word size of b bits so that the rounded b-bit number is as close as possible to the original un-quantized input signal. Rounding is performed on binary numbers with a finite word size of b bits. The quantization error, denoted by the letter e(n) is given by

$$e(n) = x_q(n) - x(n)$$
;  $x_q(n) = x(n) + e(n)$ ; (3.63)

Where  $x_q(n)$  and x(n) are the sampled quantized value and the sample un-quantized value of the input signal to the ADCs respectively. Due to the rounding, the error signal obeys the following relations:  $\frac{-q}{2} \le e(n) \ge \frac{q}{2}$ . In signal processing, a quantization error is commonly viewed as an unwanted discrete noise signal. Therefore, the output signal from the ADC is the sum of input signal x(n) and error signal e(n) as described in equation (8). The variance or power of the error signal e(n) is given by:

$$\sigma_{e}^{2} = \left\{ E(e^{2}(n)) \right\} - \left\{ E^{2}(e(n)) \right\} = \left\{ \frac{q^{2}}{12} - (0) \right\} = \frac{2^{-2b}}{12}$$
(3.64)

Here, E(e(n)) is the mean value of e(n) and its zero while  $E(e^2(n))$  is the average value of  $e^2(n)$  and p(e) is the probability density function.

The average value of  $e^2(n)$  is mathematically described as:

$$E(e^{2}(n)) = \int_{-\infty}^{\infty} e^{2}(n) p(e) de = \frac{1}{q} \int_{-q/2}^{q/2} e^{2}(n) de = \frac{q^{2}}{12};$$
  

$$p(e) = \frac{1}{q} \text{ for } \frac{-q}{2} \le e(n) \le \frac{q}{2}$$
(3.65)

The output signal of an ADC converter is passed through a first-order filter and described by:

$$y(n) = ay(n-1) + x(n)$$
 (3.66)

Besides, the transfer function of the system and impulse response of the system is given as:

$$H(z) = \frac{Y(z)}{X(z)} = \frac{z}{z-a}; \quad h(n) = a^{n} u(n)$$
(3.67)

The steady-state variance of a noise or quantization noise presents in the input signal is given as:

$$\sigma_{\epsilon}^{2} = \sigma_{e}^{2} \sum_{k=0}^{\infty} h(n)^{2} = \sigma_{e}^{2} \left[ \frac{1}{1-a^{2}} \right] = \frac{2^{-2b}}{12} \left[ \frac{1}{1-a^{2}} \right]$$
(3.68)

Generally, digital signal processors have 10-bit or 12-bit ADCs. To eliminate the steady-state variance or quantization noise in the input signal, value of 'a' is preferably chosen from the range  $0.5 \le a \le 0.99$  (ideally a lies between 0 < a < 1 to remain Region of convergence (ROC) inside the unit circle for the stability). Assume a=0.98 and 12-bit digital signal processor, the quantization noise at the output of the filter is  $4.2088e-22 \approx 0$ .

#### 3.3.3.1 IIR Filter for DC-offset elimination

The IIR based high pass filter is employed to eliminate DC-offset from sensed voltage/ current signals. Job of sensor card is to sense as well as scale the signal within range of digital signal processor (0 to 3.3 V). The digital signal processor have unipolar analog to digital converter, therefore, ac voltage/current signal must be converted from bipolar (i.e. -1.5 to +1.5 volt) to unipolar (i.e.0 to 3V) by adding offset value of 1.5V in hardware using analog electronics circuit (using op-amp).The block diagram of IIR based high pass filter is depicted in the Figure 3-24.



Figure 3-24: DC-offset elimination IIR high-pass Filter

The difference equations of IIR filter are described as:

$$x'(n) = x(n) - x'(n-1) \quad ; \quad y(n) = x'(n) + ky(n-1)$$
(3.69)

The Z-transform of the above difference equations are expressed as:

$$\frac{X'(Z)}{X(Z)} = \frac{1}{1+Z^{-1}} ; \quad \frac{Y(Z)}{X'(Z)} = \frac{1}{1-kZ^{-1}}$$
(3.70)

The transfer function of IIR filter is defined as:

$$\frac{Y(Z)}{X(Z)} = \frac{Y(Z)}{X'(Z)} \quad \frac{X'(Z)}{X(Z)} = \frac{1}{1-kZ^{-1}}$$

$$\frac{1}{1+Z^{-1}} = \frac{1}{1+Z^{-1}-kZ^{-1}-kZ^{-2}} = \frac{1}{1+(1-k)Z^{-1}-kZ^{-2}}$$
(3.71)

By applying inverse Z-transform, the difference equation can be described as:

$$y(n) = -(1+k)y(n-1)+ky(n-2) + x(n)$$
(3.72)



Figure 3-25: Bode plot of IIR high pass filter by taking different value of k

Bode diagram gives information regarding selection of value for parameter k. The value of parameter k for IIR high pass filter should be selected between 0.85 to 0.99, as shown in bode diagram 3-25.

## 3.4 Modified –Second order generalized Integrator – FLL



The fundamental structure of the SOGI-FLL is depicted in Figure 3-16.







Figure 3-26: Functional diagram of MSOGI-FLLL

When the third integrator determines the DC-offset, it subtracts it from the signal in order to improve the system's DC-offset rejection capabilities, as shown in Figure 3-26. The proposed

MSOGI-FLL structure, seen in Figure3-26, includes a DC signal cancellation (DSC) block as well as a SOGI-FLL structure, which is shown in Figure 6. DC-offsets can be injected into the grid signal by signal conditioning or measuring equipment, as well as other factors such as half-wave rectification, which are all common. As a result, the pre-filtering stage has a DC signal cancellation (DSC) block that provides superior DC-offset rejection, as well as a SOGI-FLL block that rejects the low-order harmonic. By integrating the DSC operator in the band-pass DSOGI-FLL (Figure ) filter [24], [32], an extended modification of the band-pass SOGI-FLL filter [24], [32] designated as MSOGI-FLL can be presented. For the purposes of comprehension, a grid signal contaminated with a DC-offset and MSOGI transfer functions is represented as follows:

$$D_{\text{MSOGI-FLL}}(s) = \frac{Y(s)}{v_{\text{in}}(s)} = \frac{k\omega' s^2}{s^3 + k\omega'^{s^2} + k'\omega'^{s^2} + \omega'^2 s + k'\omega'^3}$$
(3.73)

$$Q_{\text{MSOGI-FLL}}(s) = \frac{Y'(s)}{v_{\text{in}}(s)} = \frac{k\omega's}{s^3 + k\omega's^2 + k'\omega's^2 + \omega'^2s + k'\omega'^3}$$
(3.74)

$$E_{MSOGI-FLL}(s) = \frac{V_{dc}(s)}{v_{in}(s)} = \frac{k'\omega'^{s^2} + k'\omega'^3}{s^3 + k\omega's^2 + k'\omega's^2 + \omega'^2 + k'\omega'^3}$$
(3.75)

Using Routh hurtiz criteria, the gain k is given as:

$$k = \frac{9.2}{\omega' t_s}$$
;  $t_s = 4.6 * \tau$ ; and  $\tau = \frac{1}{\zeta \omega_n}$  (3.76)

To effectively filter out low and high-frequency components in the input signals, the gain k parameter must be carefully calibrated. Because of this,  $D_{SOGI-FLL}(s)$ ,  $Q_{SOGI-FLL}(s)$  attenuate low frequency components, leaving just the DC-offset, as depicted in Figure 3-26 and 3-27. MSOGI-FLL transfer functions/characteristic equation MSOGI- FLL( $D_{MSOGI-FLL}(s)$ , and  $Q_{MSOGI-FLL}(s)$ ) are chosen from the roots of the denominator of the transfer functions/characteristic equation MSOGI-FLL(s), and  $Q_{MSOGI-FLL}(s)$  with equal real parts (Figure 3-27)(all three poles have equal natural frequency of oscillation). To determine the gain k and k', on the other hand, the equation  $\omega_{n1} = \omega_{n2} = 2*pi*50$  rad/s (the same as for tuning SOGI-FLL) is employed, which is the same as for tuning SOGI-FLL. The bode graphs in Figure 3-27 demonstrates the impact of both gain adjustments as well as performance assessment of SOGI-FLL and MSOGI-FLL using magnitude plots of transfer functions from equations (3.48)-(3.49) & (3.73)-(3.74), respectively.



Figure 3-27: Bode diagram of MSOGI-FLL by choosing the value of k and k'.

Figure 3-27(a) and (b) show magnitude bode graphs of  $D_{MSOGI-FLL}(s)$  and  $Q_{MSOGI-FLL}(s)$  (equation (3.73)-(3.74)), below 0dB for low frequency components, indicating attenuation of low frequency and dc components. It is clear that a positive gain  $Q_{SOGI-FLL}(s)$ , which does not reduce the dc signal. Due to presence of third generalised integrator, the magnitude of the transfer function  $E_{MSOGI-FLL}(s)$  is close to 0dB. Moreover,  $Q_{MSOGI-FLL}(s)$  has negative gain at frequencies over 50Hz, which

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reduces higher order harmonics. But it's considerably lower than 50Hz. With the third integrator, the fundamental component (and higher order frequencies) is greatly attenuated, leaving only the low order frequencies to pass, as seen below. It aids in estimating and eliminating the DC-offset from grid voltage. It's feasible to estimate the peak errors in the basic grid's parameters (e.g. amplitude, phase and frequency information), and  $t_r$  stands for the settling time performance.

Cases	Peak	SRF-	SOGI-	MSOGI-
	Errors	PLL	FLL	FLL
Voltage	$\Delta \mathbf{A_g}$	-	-	-
Drops	$\Delta \mathbf{f_g}$	-	-	-
	$\Delta \mathbf{ heta}_{\mathbf{g}}$	-	-	-
	t <sub>r</sub>	$\approx 80$	≈ 55	≈ 45
Freq.	$\Delta \mathbf{A_g}$	≈ 2	-	-
Step	$\Delta \mathbf{f_g}$	≈ 9	≈ 5	$\approx 4$
change	(during			
	oveshoot)	0	0	0
	$\Delta \mathbf{\theta}_{\mathbf{g}}$	$\approx 5^{\circ}$	$\approx 1.5^{\circ}$	$\approx 1.5^{\circ}$
	t <sub>r</sub>	≈ 80	$\approx 40$	≈ 34
DC-offset Elimination		NO	NO	YES
Harmonics Attenuation		NO	YES	YES
Steady-state A	ccuracy	Average	Good	Good
Control param	eters	2	2	3
PI Tunning Re	quired	YES	NO	NO

Table 3-3 : Highlights of Comparative Performance Assessment

The suggested technique takes roughly 2.4 times as long to compute the grid's parameters as the existing standard. With the SOGI-QSG and dc signal cancellation block, MSOGI-FLL can achieve improved immunity to DC-offset and harmonic noise. Both the SOGI–FLL and the SRF-PLL have frequency information that is modified by the phase angle change. However, in the instance of the provided approach, the anticipated frequency has a maximum overrun of 4 Hz. With a net settling time of 34 ms, the recommended single-phase system has demonstrated to

have good harmonics reduction and DC-offset rejection characteristics. There is **84** | P a g e

therefore tremendous potential for the described technology to recognise harmonic and fundamental grid voltage characteristics selectively. Table 3-3 summarizes the experimental findings for the single- phase grid voltage test scenarios.

### 3.5 Conclusion

The MSOGI-FLL technique can be used to obtain good rejection of DC-offset and harmonics, as well as extraction of frequency and phase-angle information. With the exception of the presence of a DC-offset, SOGI-FLL is capable of accurately estimating the frequency of the grid signal. Because of a DC-offset in grid voltage, the anticipated frequency has a low frequency component of 100Hz due to the DCoffset. When harmonics are present, the distortion on this 100Hz ripple is increased, increasing the overall distortion. As a result of the inaccuracy of the frequency estimate, the synchronization and control of the DG-based inverter may be impaired. In order to achieve the best balance between dynamic responsiveness, filtering capabilities, and the requisite precision in detecting frequency and phase angle for single-phase grid-tied inverters under less than ideal grid conditions, the control parameters of SOGI-FLL must be chosen with care. When the anticipated synchronized frequency is used, there is no ripple in the expected synchronized frequency. This structure is comprised of two fundamental blocks: a standard SOGI-QSG design block that has been updated with a DC-offset cancellation block, and a FLL that is used to compute grid frequency in an adaptive manner. When compared to the regular SOGI-FLL structure, the DC-offset cancellation block (i.e. third integrator) in MSOGI-FLL reduces the DC-offset by a significant amount. Additionally to the advantages of conventional SOGI-FLL, the proposed technique is capable of rejecting DC-offset and, as a result, accurately tracking the fundamental grid-voltage component frequency under all grid abnormalities, hence outperforming the standard technique. The proposed technology is also robust to voltage sags and surges as well as frequency changes in the power grid. The findings of the experiments have revealed that the suggested MSOGI-FLL appears to be more precise and has a higher transient stability than the traditional SOGI-FLL, as demonstrated by the results of the experiments.

# CHAPTER-4MODELINGANDCONTROLOFMULTIPURPOSESINGLESTAGEGRIDTIEDTHREE PHASEPHOTOVOLTAICSYSTEM

With the advancement in technology, the recent past has seen the increasing use of photovoltaic (PV) generation in the power grid, ultimately resulting in reducing costs of power electronic devices in addition to various subsidies and encouragement schemes to promote solar generation. [1]. As increased nonlinear loads on the Distribution end of power sector have resulted in adversely affecting the operation and control of power grid along with higher instability [2]. In order to address these difficulties, grid tied PV system has introduced enhanced control techniques in frequency and time domain to control fluctuating load current thereby improving power quality. The frequency control technique deployed more computation burden as well as one cycle delay due to a window sampling method [3]. Hence, it is not appropriate for real time control application. A detailed analysis of the basic SRFT based control technique in a PV system reveals satisfactory results during balanced loading conditions [4]. However, in case of unbalanced load, dominance of third harmonic component was observed due which the performance of SRFT decreased drastically [4-5]. Hence to obtain a steady state response during unbalanced load, very low frequency is to be set for Low -pass filter (LPF) which in turn decreases the dynamic response of the PV system thereby giving it a stable condition [6]. To confront earlier mentioned issues, researchers have presented simple to complex various control approaches to ensure desire steady state as well as transient response [7]. References [5][9-12] have presented compressive and comparative review on a PV system with different control approaches to ensure superior steady state and dynamic response during ideal and non-ideal grid situations. Hence, by feeding maximum active power and minimum reactive power, grid reliability is obtained. Also an abrupt change in the solar irradiance causes DC-bus voltage fluctuations. To counter balance this, Feedback linearization technique is used to keep the DC voltage derivation within the acceptable limit.
The active power injected into the grid is proportionate to the availability of solar irradiance [16]. Reactive power control strategies such as frequency control, voltage regulation at PCC, power factor control at grid side etc. are accentuated due to modified control strategies of PV system which is described in [16-17]. Some of the important characteristics of grid tied PV system are simple design, efficient control mechanism, improved efficiency and reliable operation with the reduced cost in the application of PV inverter. Thus, the single-stage three phase grid tied PV inverter is an amiable and feasible option to fulfill almost above requirements with comparatively lower cost by eliminating a DC to DC converter for regulation of DCbus voltage [17]. An insight into varied MPPT techniques along with various PV converter topologies (voltage source) are discussed in the references [16-17] [19-20]. Additionally, while ignoring the aspect of stability, various control techniques for single-stage PV system are described in the references [9][20-23][25]. Alternative way to utilize remaining capacity of PV inverter[18], quadrature axis current control is employed to the PV inverter by using a fixed value reactive power as per the safety rating of PV inverter However, if PCC voltage remains below the acceptable lower limit of PCC voltage for more than a prescribed period of time, then DERs need to be disconnect A unique concept of utilizing PV system as STATCOM at reduced load (or night hours) with additional various grid support functions. Furthermore, the unutilized inverter capacity after real power generation can be address by modifying control system during peak load (daytime) without oversizing PV inverter [19][18][20][22][26].

### 4.1 Architecture of PV system

According to power processing stage Photovoltaic (PV) inverters can be divided into the two categories: (i) Two-stage grid tied PV system, and (ii) Single-stage grid tied PV system[3]. In general, the output voltage of a PV array is not high enough and fluctuates with the changing ambient conditions, which is undesirable. As a result, an additional DC-DC converter stage is required[10][86], which ensures a constant DCbus voltage regardless of changes in the input voltage. Despite the fact that the twostage architecture provides advantages in controller design, it also has significant

shortcomings. Increased circuit stages (DC-DC converter stage) cause an increase in power loss, which causes the overall energy transfer efficiency to drop [26]. Increasing the number of circuit stages also increases the complexity of the system, which results in decrease in system reliability. The active power flow of PV system is controlled by voltage source converter through maintaining DC-bus of PV inverter. However, two-stage PV system has a DC-DC converter for Maximum power extraction (i.e. first stage) and voltage source inverter for grid synchronization and power control (i.e. Second stage), which needs several additional power devices and components which cause considerable conduction losses, sluggish transient response and also increase cost. In order to improve system efficiency, the sub-control system like a MPPT algorithm, current control loop, and voltage control loop should only rely on the inverter, as illustrated in Figure 4-1.



Figure 4-1: A power circuit diagram of single stage grid tied PV system

A boost converter for Maximum power extraction (First stage) and voltage source inverter for grid synchronization and power control (Second stage), which needs several additional power devices and components cause considerable conduction losses, sluggish transient response, and also increase the cost. The single-stage PV system is employed with the benefits of good efficiency and low-cost solution, as depicted in Figure 4-1. The drawbacks of the single-stage converter are that the PV panels are in series, and if the shading occurs on one or several PV panels, the whole system's efficiency is reduced. Over the day, the temperature and the solar irradiance level will change gradually as sunlight angles or shading patterns change, making gradual changes in PV characteristics and also, sometimes, quick changes in curves

for just a short period may occur due to circumstances like passing birds or clouds. [7]. It is noted that the power and current of the PV module increase as increases solar irradiance level, in turn, and the MPP voltage will increase while the temperature is inversely proportional to the voltage and power of the PV panel, which means the open-circuit voltage and the MPP voltage decrease as increases temperature. Hence, MPPT control is necessary for maximizing the power generation PV systems. The two primary challenges of the grid-tied inverter, directly or indirectly, are the control of the DC-bus voltage (in the absence of a DC-DC converter) and controlling the AC power. The direct power control of grid-tied inverter can be achieved by applying instantaneous power theory, stationary frame control theory, or synchronous reference frame control theory, as depicted in Figure 4-2, for controlling current and/or voltage. However, the chapter also focuses on the DC-bus voltage management since the absence of a DC-DC converter stage between the PV panels and the grid, i.e., system controls depend only on voltage source converter. If the current control loop is absent, then the control is linear in terms of the decoupling between AC and DC dynamics but nonlinear in terms of the AC dynamics represented directly in terms of power. Direct power control can be achieved using a separate PWM modulator or without one (i.e., hysteresis current control).



Figure 4-2: Conceptual Power theory for grid tied PV system

There are various current reference generation theories for a conventional PV system, STATCOM, and shunt active filter either in the discrete-time or frequency domain. The current reference generation theories in the frequency domain are Fourier series theory, Discrete Fourier transforms approach, Fast Fourier transform theory, recursive discrete Fourier transform, Kalman filter-based control algorithm. In contrast, the current reference generation theories in the time domain are Unit Template theory, Instantaneous reactive power theory, Synchronous reference frame theory, Instantaneous symmetrical component theory[3][5][8][13][28].

### 4.2 Synchronous Reference Frame Power Control of Single Stage Grid Tied Photovoltaic System

The principle of power exchange can be clarified using a short-line model having impedance  $(z = R_f + j\omega L_f)$  between voltage source converter  $(v_{inv,abc})$  and the grid  $(v_{pcc,abc})$  and, as shown in Figure.4-1.The control structure is depicted in the figure 4-3 and the dynamics mathematical expression for the single line model is given as:

$$\vec{V}_{inv,abc} = R_f \vec{i}_{inv,abc} + L_f \frac{d\vec{i}_{inv,abc}}{dt} + \vec{V}_{PCC,abc}$$
(4.1)

For the synchronous reference frame,  $abc \rightarrow dq$  transformation is employed using the Park Transformation matrix and it is described as:

$$C_{k} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos \omega t & \sin \omega t & \frac{1}{\sqrt{2}} \\ \cos(\omega t - 120^{0}) & \sin(\omega t - 120^{0}) & \frac{1}{\sqrt{2}} \\ \cos(\omega t + 120^{0}) & \sin(\omega t + 120^{0}) & \frac{1}{\sqrt{2}} \end{bmatrix}$$
(4.2)

The matrix property is used here:

$$C_k^{-1} = C_K^T$$
(4.3)

The equation (4.1) is written in simplified manner:

$$\begin{bmatrix} \mathbf{v}_{\mathrm{inv}_{a}} \\ \mathbf{v}_{\mathrm{inv}_{b}} \\ \mathbf{v}_{\mathrm{inv}_{c}} \end{bmatrix} - \begin{bmatrix} \mathbf{v}_{\mathrm{pcc}_{a}} \\ \mathbf{v}_{\mathrm{pcc}_{b}} \\ \mathbf{v}_{\mathrm{pcc}_{c}} \end{bmatrix} = \begin{bmatrix} \mathbf{L} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{L} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{L} \end{bmatrix} \frac{\mathrm{d}}{\mathrm{dt}} \begin{bmatrix} \mathbf{i}_{\mathrm{inv}_{a}} \\ \mathbf{i}_{\mathrm{inv}_{b}} \\ \mathbf{i}_{\mathrm{inv}_{c}} \end{bmatrix} + \begin{bmatrix} \mathbf{R} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{R} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \mathbf{R} \end{bmatrix} \begin{bmatrix} \mathbf{i}_{\mathrm{inv}_{a}} \\ \mathbf{i}_{\mathrm{inv}_{b}} \\ \mathbf{i}_{\mathrm{inv}_{c}} \end{bmatrix}$$
(4.4)



### Figure 4- 3 : Control mechanism of single stage grid tied PV system in Synchronous reference frame

In the equation (4.4), abc  $\rightarrow$ dq transformation is employed using the Park Transformation matrix and is described as:

$$[C_k] \left[ v_{inv_{dq}} - v_{pcc_{dq}} \right] = [L] \frac{d}{dt} \{ [C_k] [i_{dq}] \} + [R] \{ [C_k] [i_{dq}] \}$$
(4.5)

The First term of equation (4.5) is simplified and represented as:

$$\frac{\mathrm{d}}{\mathrm{dt}}\left\{\left[C_{k}\right]\left[i_{\mathrm{dq}}\right]\right\} = \left[C_{k}\right]\frac{\mathrm{d}}{\mathrm{dt}}\left\{\left[i_{\mathrm{dq}}\right]\right\} + \left[i_{\mathrm{dq}}\right]\frac{\mathrm{d}}{\mathrm{dt}}\left\{\left[C_{k}\right]\right\}$$

$$(4.6)$$

By substituting the equation (4.2) into the equation (4.6), the differentiation of parktransformation is simplified as:

$$\frac{d}{dt}\{[C_k]\} = \sqrt{\frac{2}{3}} \begin{bmatrix} -\sin\omega t & \cos\omega t & 0\\ -\sin(\omega t - 120^0) & \cos(\omega t - 120^0) & 0\\ -\sin(\omega t + 120^0) & \cos(\omega t + 120^0) & 0 \end{bmatrix} \omega$$
(4.7)

By using trigonometry properties, Equation (4.7) can be simplified as:

$$\frac{d}{dt} \{ [C_k] \} = \sqrt{\frac{2}{3}} \omega \begin{bmatrix} \cos \omega t & \sin \omega t & \frac{1}{\sqrt{2}} \\ \cos(\omega t - 120^0) & \sin(\omega t - 120^0) & \frac{1}{\sqrt{2}} \\ \cos(\omega t + 120^0) & \sin(\omega t + 120^0) & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$
(4.8)

Here, a matrix M is assumed as:

$$[\mathbf{M}] = \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$
(4.9)

Hence, the equation (4.8) can be re-written as:

$$\frac{\mathrm{d}}{\mathrm{dt}}\{[\mathsf{C}_k]\} = \omega[\mathsf{C}_k][\mathsf{M}] \tag{4.10}$$

The equation (4.5) is simplified and re-written as:

$$[C_{k}] \left[ v_{inv_{dq}} - v_{pcc_{dq}} \right] = [L][C_{k}] \frac{d}{dt} \{ [i_{dq}] \} + [L][i_{dq}] \frac{d}{dt} \{ [C_{k}] \} + [R] \{ [C_{k}] [i_{dq}] \}$$

$$(4.11)$$

$$[C_{k}] \left[ v_{inv_{dq}} - v_{pcc_{dq}} \right] = [L][C_{k}] \frac{d}{dt} \{ [i_{dq}] \} + \omega[L][i_{dq}][C_{k}][M] + [R] \{ [C_{k}][i_{dq}] \}$$
(4.12)

$$\left[v_{inv_{dq}} - v_{pcc_{dq}}\right] = [L]\frac{d}{dt}\left\{\left[i_{dq}\right]\right\} + \omega[L][M][i_{dq}] + [R]\left\{\left[i_{dq}\right]\right\}$$
(4.13)

Equation (4.13) can be simplified in context of d-axis and q-axis current:

$$[L]\frac{d}{dt}\{[i_d]\} = \omega[L][i_d] - [R]\{[i_d]\} + [v_{inv_d} - v_{pcc_d}]$$
(4.14)

$$[L]\frac{d}{dt}\{[i_q]\} = -\omega[L][i_q] - [R]\{[i_{dq}]\} + [v_{inv_d} - v_{pcc_d}]$$
(4.15)

The above proved equations (4.14) and (4.15) are the modeled inverter equations which contains the cross-coupled terms. So it can be observed that control of the output parameters is not possible directly by controlling d axis and q-axis separately. As it is a non-linear term, so, the decoupling is added to linearize the cross-coupling terms as well as to achieve control over two axes individually[7][44][46]. The overall amount of active component of reference current (d-axis reference current) is calculated by adding together the output of the proportional– integral (PI) controller and feed- forward PV current value. The simplified and well-known control theory is used to minimize error using the PI controller and assumed actual quantity as x. The difference between a reference quantity (x\*) and an actual quantity (x) can be used to calculate the output of the PI controller, as shown in the following equation.

$$\varepsilon_{\rm x}({\rm m}) = {\rm x}^*({\rm m}) - {\rm x}({\rm m})$$
 (4.16)

The error acquired from equation (4.16) is passed to the PI controller to obtain reference signal for the control system and described as:

$$x_{ref}(m) = k_p \varepsilon_x(m) + k_i \int_0^{T_s} \varepsilon_x(m) dt$$
(4.17)

The discretization of above equation, with the sampling time  $(T_s)$ , can be obtained by converting integration into summation and represented as:

$$x_{ref}(m) = k_p \varepsilon_x(m) + k_i \sum_{k=0}^{m} \varepsilon_x(j) T_s$$
(4.18)

At sampling instant i.e. m=1, the equation can be represented as:

$$x_{ref}(1) = k_p \epsilon_x(1) + k_i \{ \epsilon_x(0) + \epsilon_x(1) \} T_s$$
(4.19)

Similarly, at sampling instant, i.e. m=2 would be represented as:

$$x_{ref}(2) = k_p \epsilon_x(2) + k_i \{ \epsilon_x(0) + \epsilon_x(1) + \epsilon_x(2) \} T_s$$
(4.20)

The difference of reference quantity at consecutive instant is represented as:

$$x_{ref}(2) - x_{ref}(1) = \{ k_p \epsilon_x(2) + k_i \{ \epsilon_x(0) + \epsilon_x(1) + \epsilon_x(2) \} T_s \}$$

$$\{ k_p \epsilon_x(1) + k_i \{ \epsilon_x(0) + \epsilon_x(1) \} T_s \}$$

$$(4.21)$$

The simplification is given as:

$$x_{ref}(2) = x_{ref}(1) + k_p \{ \varepsilon_x(2) - \varepsilon_x(1) \} + k_i \{ \varepsilon_x(2) \} T_s \}$$
(4.22)

Similarly, for m<sup>th</sup> sampling instant, the reference quantity is described as:

$$x_{ref}(m) = x_{ref}(m-1) + k_p \{\epsilon_x(m) - \epsilon_x(m-1)\} + k_i \{\epsilon_x(m)\}T_s\}$$
(4.23)

Similarly, as equation(4.25), the reference quantity of the d-axis current is cumulative of power loss component and feed forward path, and computed by outer DC voltage control loop( Figure 4-3)as follow:

$$i_{d_{ref}}(n) = i_{d_{ref}}(n-1) + k_{P} \{ (V_{dc_{ref}}(n) - V_{dc}(n)) - (V_{dc_{ref}}(n-1) - V_{dc}(n-1)) \} + k_{i}T_{s} \{ V_{dc_{ref}}(n) - V_{dc}(n) \} + \frac{2V_{PV}I_{PV}}{3V_{m}}$$

$$(4.24)$$

The active and reactive power flowing into the short-line model by assuming  $(X_f = j\omega L_f \gg R_f)$  can be computed as:

$$P = \frac{3}{2} \left[ (V_d I_d) + (V_q I_q) \right]$$
(4.25)

$$Q = \frac{3}{2} \left[ \left( -V_{d} I_{q} \right) + \left( V_{q} I_{d} \right) \right]$$
(4.26)

The Phase lock loop unit maintain  $V_d$  as peak value of PCC or grid voltage and  $V_q$  to the zero. Hence, consequently, the equation (4.25) and equation (4.26) are re-written as:

$$P = \frac{3}{2} (V_d I_d)$$
 (4.27)

$$Q = \frac{3}{2} \left( -V_d I_q \right) \tag{4.28}$$

From equation (4.27) and equation (4.28), the active and reactive power output of inverter can be controlled through  $I_d$  and  $I_q$ , respectively, at certain PCC or grid voltage[7].

### 4.3 MPPT Extraction from PV Panel

The PV array delivers maximum power at a single operating point on the PV array characteristics for given fix isolation and temperature. The objective of maximum power point tracker is to detect the single operating point at which PV array can deliver maximum power irrespective of variations in solar isolation and temperature. The perturb and observe (P&O) and incremental conductance (INC) methods are well-known popular MPPT algorithm described in the literature [10][54-58][90-94]. The perturb and observe MPPT algorithm is robust and simple for the implementation on other hand has limitation to track correct maximum power point

(MPP) in rapidly changing atmospheric conditions. Hence, in this proposed work, INC MPPT algorithm is used engaged to identify maximum power point on a PV curve for further creation of the DC reference voltage, which is used in a control system for single- stage grid assisted system. It is worth pointing that the derivative of PV power with respect to its terminal voltage across PV array is result to null at maximum power point (MPP) on the power curve of PV[10][90][93].

The PV power and derivative of PV power with the PV voltage are mathematically written as:

$$P_{pv} = I_{pv} \times V_{pv} \tag{4.29}$$

$$\frac{\Delta P_{pv}}{\Delta V_{pv}} = \frac{\Delta (I_{pv} \times V_{pv})}{\Delta V_{pv}} = I_{pv} + V_{pv} \frac{\Delta (I_{pv})}{\Delta V_{pv}}$$
(4.30)

At MPP, it becomes zero and re-written as:

$$\frac{1}{(V_{pv})} \times \frac{\Delta P_{pv}}{\Delta V_{pv}} = \frac{I_{pv}}{V_{pv}} + \frac{\Delta (I_{pv})}{\Delta V_{pv}} = G_{pv} + \Delta G_{pv} = 0 \text{ (at MPP)}$$
(4.31)

where  $G_{pv} = \frac{I_{pv}}{V_{pv}}$  and  $\Delta G_{pv} = \frac{\Delta(I_{pv})}{\Delta V_{pv}}$  are represented as PV conductance and incremental conductance of PV respectively. From the equation (4.31), there are three operating points to determine the direction in which to climb based on the sign of  $\Delta G_{pv} = \frac{\Delta P_{pv}}{\Delta V_{pv}}$  to reach MPP on a power curve of PV array and represented as:  $G_{pv} + \Delta G_{pv} > 0$  (Left side of MPP, climb upward);  $G_{pv} + \Delta G_{pv} = 0$  (at MPP);  $G_{pv} + \Delta G_{pv} < 0$ (Right side of MPP, climb downward)) (4.32)

Figure 4-4 depicts the flow chart of the operating conditions of the Incrementalconductance MPPT algorithm and the PV characteristic of the PV panel. The primary advantage of the algorithm when compared to Perturb & observe (P&O) algorithms is that it is fast-tracking of the MPP deprived of oscillations with improved accuracy. Although, the time taken for computation in the Incremental-conductance MPPT algorithm is more due to its complexity. The speed of tracking of MPP is directly proportional to the step size in INC MPPT-the bigger the step size, the faster the monitoring. But, the problem with fast-tracking is that the significant power wave keeps oscillating around the MPP value and never attains exact MPP value.



Figure 4- 4 : Flow-chart of Increment-conductance MPPT algorithm,(b) PV characteristic of PV panel with different temperature, and (c) PV characteristic of PV panel with different solar irradiance

This ultimately leads to lower efficiency. Whereas, when the step-size in the INC MPPT is small, the time taken to reach MPP value is more but greater accuracy and efficiency is observed. Thus, a choice between dynamics and oscillation is to be made during the operation of MPPT technique [7] [17][19][29].

### 4.4 DC-Bus Voltage Control

The DC-bus capacitor plays essential role to compensate inverter switches power loss by providing active power. As counter effect, voltage of DC-bus capacitor decays gradually, hence, small amount of active power needed which is absorbed by inverter to maintain a voltage of DC-bus capacitor. During day time a sufficient amount of solar irradiance available, DC-bus capacitor charged from PV panels to maintain DC-bus voltage and rest of the power injected into the grid. The DC-bus capacitor voltage is kept constant during the night by absorbing a minimal amount of active power from the grid through inverter diodes. When the MPPT Algorithm computesV<sub>dc,ref</sub>, it uses the DC-bus voltage controller to maintain that voltage on the DC-bus capacitor.

The Energy stored in DC-bus capacitor is given as:

$$\Delta E = \frac{1}{2} C V^2 \tag{4.33}$$

The PI controller is employed to maintain DC-bus voltage in line with the MPP reference voltage,  $V_{dc,ref}$ , which is computed from MPPT algorithm.

The Power balance equation can be written as:

$$\frac{\Delta E}{\Delta t}\Big|_{t\to 0} = \frac{dE}{dt} = \Delta P = P_{PV} - P_{inv}$$
(4.34)

It can control the active power delivered into the grid by regulating the DC-bus voltage by changing the direct axis current. With the inverter power loss ignored, the power balance of both sides of the inverter in a steady-state should result in DC-bus power, $P_{PV}$ ,equal to the output power at the AC-side terminals of VSC, which is equivalent to the output power at the grid, with the filter power loss ignored.

According to the power balance theory, the DC-bus capacitor's voltage dynamics are as follows:

$$\frac{d(\frac{1}{2}CV_{dc}^{2})}{dt} = P_{PV} - P_{inv}$$
(4.35)

As per Synchronous reference frame (dq frame), The Power of inverter  $(P_{inv})$  can be described as:

$$P_{\rm inv} = \frac{3v_{\rm d}i_{\rm d}}{2} \tag{4.36}$$

By substituting equation (4.36) into (4.35), the power balance equation can be modified as :

$$CV_{dc} \frac{d(V_{dc})}{dt} = I_{PV} * V_{dc} - \frac{3v_d i_d}{2} \quad ; \quad \Rightarrow C \frac{d(V_{dc})}{dt} = I_{PV} - \frac{3v_d i_d}{2V_{dc}}$$

$$C \frac{d(V_{dc})}{dt} = I_{PV} - \frac{3v_d i_d}{2V_{dc}}$$

$$(4.37)$$

Here,  $i_d$  and  $v_d$  are the d-axis grid current and voltage respectively. It is a first order non-linear equation which should be converted into linear form for sake of simplicity in the control system. Consider a non-linear system, which is represented by functions f(x)and b(x) with control state x and given as

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}) + \mathbf{b}(\mathbf{x})^* \mathbf{u}_i$$
 (4.38)

Here, ui is control input and described as:

$$u_i = \frac{1}{b} \{ y - f(x) \}$$
 (4.39)

Now, inserting equation (4.39) within equation (4.38), the non-linear system can be represented as linear system as

Hence, Non-linearity can be eliminated as:

$$\dot{\mathbf{x}} = \mathbf{y} \tag{4.40}$$

Similarly, substituting the  $i_d = \frac{2v_{dc}}{3V_d} \{I_{PV} - y\}$  as control input, the equation (4.37) can

be modified in the linearized differential form

$$C\frac{d(V_{dc})}{dt} = y \tag{4.41}$$

Therefore, the plant transfer function is described as

$$G_{p}(s) = \frac{V_{dc}(s)}{v_{i}(s)} = \frac{1}{sC}$$
(4.42)

A discrete PI controller is employed before plant transfer function to achieve a desired settling time and other dynamics parameters. The sampling time of current control loop is chosen 10times larger than the sampling time of voltage control loop in order to decouple the current control and voltage control loop for the control system.

### 4.5 Reactive Power control

The reactive power is exchanged with grid through PV inverter to achieve the control objective either PCC voltage regulation or maintaining unity power factor at grid side. During the variation of PCC voltage from the acceptable range, the control objective of multipurpose PV inverter is only to provide reactive power support to maintain PCC voltage within acceptable ranges, and behaves as fully STATCOM. During a fully STATCOM operation, direct- axis current reference sets to the zero. The quadrature - axis current reference, which is generated by the PCC outer loop voltage controller, provides a reactive power support to maintained the PCC voltage (in fully STATCOME MODE) or regulate unity power factor at grid side (in Partial-PV and partial STATCOM mode) [17][19-20].

### 4.6 PCC Voltage Regulation

The PCC voltage may be varied away from acceptable ranges depending on the loading conditions i.e. load presents at PCC. Hence, it is the control objective to maintain PCC voltage within acceptable range during any loading conditions and load variation. From the Figure 4-1 and Figure.4-3, grid current and PCC voltage can be described as:

$$i_{g,abc} = i_{Load,abc} - i_{PV,abc}$$
(4.43)

$$V_{PCC,abc} = L_g \frac{di_{g,abc}}{dt} + v_{g,abc}$$
(4.44)

By neglecting a transient condition of MDSOGI-FLL, It should be pointed that  $v_q$  is maintained to the zero by MDSOGI-FLL, where as  $v_d$  gives the PCC voltage. Therefore, ignoring current of the shunt filter capacitor, the PCC voltage in dq frame is described as:

$$v_{d} = L_{g} \omega_{o} i_{q} - L_{g} \omega_{o} i_{Load,q} - L_{g} \frac{di_{d}}{dt} + L_{g} \frac{di_{Load,d}}{dt} + V_{peak}$$
(4.45)

The error of PCC voltage is computed as:

$$\varepsilon_{v_{PCC}} = v_{ref_{PCC}}^* (t) - v_{PCC} (t)$$
(4.46)

The PI controller eliminates the error between reference value of PCC voltage (Peak value of phase voltage / R.M.S value of phase voltage ) and actual value of Peak value of phase voltage/ R.M.S value of phase voltage, which is computed from

sensed three-phase PCC voltages. The output of the PI controller gives the reference value of the quadrature-axis current,  $i_{q_{ref}}$ , and it is expressed as:

$$i_{q_{ref}} = k_p \, \varepsilon_{v_{PCC}} + k_i \int_0^{T_s} \varepsilon_{v_{PCC}} dt$$
(4.47)

At sampling time  $T_s$ , the discretise form of the equation (4.47) can be represented as:

$$i_{q_{ref}}(m) = i_{q_{ref}}(m-1) + k_{p} \{ \epsilon_{v_{PCC}}(m) - \epsilon_{v_{PCC}}(m-1) \}$$

$$+ k_{i} \epsilon_{v_{PCC}}(m) T_{s}$$

$$(4.48)$$

The PI controller is employed in voltage control loop to make the quadrature-axis reference current, consequently, used in the current control loop of inverter. The PCC voltage control loop has inner quadrature-axis current control loop. Hence, the sampling time of voltage control loop is 10-50 times larger than the current control loop for the decoupling.

#### 4.6.1 **Power Factor Correction**

During the availability of reactive loads at the PCC, if and only if PCC voltage is within an acceptable range, then the inverter also provides reactive power support to maintain unity power factor at the grid side, simultaneously injecting active power into the grid. As  $v_q=0$ , the phase difference ( $\delta$ ) is angle between grid voltage (PCC voltage) and grid current and Power factor at grid side is calculated as





Figure 4-5: Block diagram for a Power factor correction

The relationship between quadrature axis inverter current and PF are derived as:

$$\tan \delta = \frac{i_{g,q}}{i_{g,d}} ; \qquad \tan \left( \cos^{-1} PF \right) = \frac{i_{\text{Load},q} - i_{PV,q}}{i_{\text{Load},d} - i_{PV,d}}$$
(4.50)

From the equation (4.50), to obtain desire power factor, the quadrature –axis reference inverter current is derived as:

$$i_{q,ref} = -1 \times \{ i_{Load,q} - \{ tan (cos^{-1} PF) \times (i_{Load,d} - i_{PV,d}) \} \}$$
 (4.51)

The quadrature –axis reference inverter current is generated for unity power factor at grid by taking the value PF to be zero. For unity power factor, which means PF =1 that gives  $(\cos^{-1} PF) = 0$  and equation (4.51) is re-written as:

$$i_{q_{ref}} = -i_{Load,q}$$
(4.52)

### 4.7 Current Control in synchronous reference frame

The dynamics of AC current in multipurpose inverter, as shown in single line diagram (Figure 4-1and Figure 4-3), is mathematically represented by following equations in d-q frame

$$L_{f}\frac{di_{d}}{dt} = -R_{f}i_{d} + \omega L_{f}i_{q} - v_{gd} + v_{inv,d}$$

$$\tag{4.53}$$

$$L_{f}\frac{di_{q}}{dt} = -R_{f}i_{q} - \omega L_{f}i_{d} - v_{gq} + v_{inv,q}$$

$$(4.54)$$

For linearization as well as sake of simplicity,  $v_{inv,d}$  and  $v_{inv,q}$  are taken as:

$$v_{inv,d} = -\left[k_p + \frac{k_i}{s}\right] \times \left(i_{d,ref} - i_d\right) - \omega L_f i_q + v_{gd}$$

$$(4.55)$$

$$\mathbf{v}_{\text{inv},q} = -\left[\mathbf{k}_{p} + \frac{\mathbf{k}_{i}}{s}\right] \times \left(\mathbf{i}_{q,\text{ref}} - \mathbf{i}_{q}\right) + \omega \mathbf{L}_{f} \mathbf{i}_{q} + \mathbf{v}_{gq}$$
(4.56)

The equation (4.53) and equation (4.54) are modified as:

$$L_{f}\frac{di_{d}}{dt} = -\left(R_{f} - \left[k_{p} + \frac{k_{i}}{s}\right]\right)i_{d} - \left(\left[k_{p} + \frac{k_{i}}{s}\right]\right)i_{d,ref}$$

$$(4.57)$$

$$L_{f}\frac{di_{q}}{dt} = -\left(R_{f} - \left[k_{p} + \frac{k_{i}}{s}\right]\right)i_{q} - \left(\left[k_{p} + \frac{k_{i}}{s}\right]\right)i_{q,ref}$$

$$(4.58)$$

Here,  $k_p$  and  $k_i$  are the proportional and integral gains of the PI controllers. A discrete PI controller is employed before plant transfer function to achieve a desired settling time and other dynamics parameters. The sampling time of voltage control loop is chosen 10-50 times larger than the sampling time of current control loop in order to decouple the current control and voltage control loop for the control system.

### 4.8 Mode Operation of PV-STATCOM

The control mode of operation is functioning according to an operating scenario as depicted in Figure 4-6. To evaluate the performance of a multipurpose single-stage PV system, the methodological approaches are used:(i) conventional PV operation in both forward and reverse power flow conditions, (ii) multipurpose PV inverter operation in "Partial STATCOM" mode for voltage regulation and power factor correction and, (iii) conventional STATCOM operation for voltage regulation and power factor correction. The PCC voltage is denoted by  $v_{pcc}$  in all simulation results. Grid currents, PV inverter currents and load currents are denoted by the variables  $i_{grid}$ ,  $i_{inverter}$  and  $i_{Laod}$ , respectively. The effectiveness of the presented grid assisted PV system is demonstrated by the simulation results in Simulink/MATLAB environment.



**Figure 4-6 : Control for mode of operation** 

The active and reactive power of PV inverter, load, and grid are denoted as:  $P_{inv}$ ,  $Q_{inv}$ ,  $P_{load}$ ,  $Q_{load}$ ,  $P_{g}$ , and  $Q_{g}$ , respectively. The presented control approach of inverter is modeled and designed as single-stage grid connected system with 2.5kW maximum power generation capacity of PV system at maximum power point (MPP) during 1000  $\frac{W}{m^2}$  solar insolation/irradiance. The dynamic performance assessment of presented control approach for grid assisted PV system is carried out

for different modes of operation at various operating condition as follow:

### 4.8.1 Active Power injection mode [PV system only-day time, Conventional PV system]

The objective of this control mode is to inject maximum active power from PV panels as per available irradiance to the grid during day hours when the load is not attached to PCC. The quadrature axis reference current is set to a null value in this mode. The 1KW active power and1KVAR reactive power load is connected at PCC. Initially, the PV system is not connected at the PCC. The utility grid fulfills the power demand of load from t=0.3 seconds to 0.4 seconds, as depicted in Figure 4-7. At t= 0.4 seconds, the PV inverter is connected at PCC with 1200W power generation. Consequently, the surplus power (after fulfilling load demand) flows back to the grid source in the reverse direction. It needs more than one cycle for the PV inverter current to stabilize. The performance of a multipurpose single-stage PV system is summarized in the context of time to time action during reverse power flow in table 4-1.

			Active Powe	er	Reactive			
	Action		(Watt)		Power(VAR)			
Time	(PV	PV	Grid	Load	PV	Grid	Load	
(Seconds)	panels)	Invert	(Receiving	Receiving Deman		(Receiving	Domond	
		er	/Suppling)	d	ter	/Suppling)	Demanu	
0.3 to 0.4	disconnec	0	-1000	+1000	0	-1000	+1000	
	ted							
0.4 to 0.5	Connecte	-1200	+200	+1000	0	-1000	+1000	
0.5 to 0.6	d	-1600	+600	+1000	0	-1000	+1000	
0.6 to 0.7	disconnec	0	-1000	+1000	0	-1000	+1000	
	ted							

Table 4-1: Summary of performance evaluation for multipurpose single stage PV system in Full-PV mode



Figure 4-7 : Dynamic performance of multipurpose single-stage PV system during full-PV mode (reverse power flow)

However, the abrupt power reversal at PCC results a transient on grid current and PCC voltage. At t=0.5 seconds, The PV panels increase their power generation from 1200 W to 1600W. These results in an increase in PV inverter currents  $i_{inverter}$ , consequently, increase the grid current  $i_{grid}$  increases in the opposite way as solar energy generation exceeds the required load power. The PV inverter is cut off from the PCC at t= 0.6 seconds. The PV inverter currents ( $i_{inverter}$ ) instantly drop to zero and the entire load demand is supplied by the grid.

Time (Seconds)	Action		Active Powe	er	Reactive Power(VAR)			
	(PV panels)	PV Inverte r	Grid (Receiving /Suppling)	Load Demand	PV Inverter	Grid (Receiving /Suppling)	Load Demand	
0.3 to 0.4	disconnec ted	0	-2000	+2000	0	-2000	+2000	
0.4 to 0.5	connected	-1200	-800	+2000	0	-1000	+1000	
0.5 to 0.6	1	-1600	-400	+2000	0	-1000	+1000	
0.6 to 0.7	disconnec ted	0	-2000	+2000	0	-1000	+1000	

Table 4-2 : Summary of performance assessment for multipurpose single stage PV system in Full-PV mode (Forward power flow)

The 2KW active power and 2KVAR reactive power load are connected at PCC. Initially, the PV system is not connected at the PCC. The utility grid fulfills the power demand of load from t=0.3 seconds to 0.4 seconds, as depicted in Figure 4-8. At t= 0.4 seconds, the PV inverter is connected at PCC with1200W power generation. Consequently, the 2KW load power demand is coordinately fulfilled by the PV inverter and utility grid. However, the grid current declines because more of the load can now be provided by PV power output. The utility grid provides the short of 800W load power demand, as described in table 4-2. At t=0.5 seconds, the PV panels increase their power generation from 1200 W to 1600W, increasing PV inverter currents.



Figure 4-8 : Dynamic performance of multipurpose single-stage PV system during full-PV mode (forward power flow)

Consequently, active power load demand from a utility grid is also reduced from 800W to 400W, as depicted in Figure 4-8. The PV inverter is cut off from the PCC at t= 0.6 seconds. The PV inverter currents instantly drop to zero, and the grid supplies the entire load demand. A gross forward power flows from the grid to load. The performance of a multipurpose single-stage PV system is summarized in the context of time to time action during forward power flow in table 4-2.

# 4.8.2 Active and Reactive Power injection mode [Partial PV & Partial SATCOM-Daytime MODE-B]

The objective of this control mode is to inject maximum active power from PV panels as per available irradiance to the grid, simultaneously ensuring unity power factor by providing reactive power support at the side of the utility grid when the reactive load is connected, an acceptable range of PCC voltage is sensed. The reactive power exchange with a utility occurs with the residual operating capacity of the inverter during this mode. Thus, it is also called the "Partial PV-STATCOM" mode. The performance of a multipurpose single-stage PV system is summarized in the context of time to time action as PV-STATCOM in table 4-3.

Table 4-3: Summary of performance assessment for multipurposesingle stage PV system in PV-STATCOM mode

Time	Actio	A	ctive Power		Reactive Power(VAR)			
	n		(Watt)					
(Seconds)	(PV	PV	Grid	Load	PV	Grid	Load Demand	
(Beconds)	nanels	Inverter	(Receiving	Deman	Inverter	(Receiving		
	puncis		/Suppling)	d		/Suppling)		
0.3 to 0.4	connec	-1600	-200	+1800	-1200	+200	+1000	
0.4 to 0.5	ted	-1300	-700	+1800	-1519.86	+519.86	+1000	
0.5 to 0.6		-1800	0	+1800	-871.78	-128.22	+1000	
0.6 to 0.7	discon	0	-1800	+1800	0	-1000	+1000	
	nected							

In other words, the conventional PV system operates as a STATCOM utilizing its partial inverter capacity in the form of reactive power support to ensure unity power factor (Power factor correction, PFC mode) at the grid side during daytime.



Figure 4-9: Dynamic performance of multipurpose single-stage PV system during Partial PV & Partial-STATCOM mode

The 1800W active power and 1000 VAR reactive power loads are connected at PCC. The dynamic performance evaluation of the multipurpose PV system is tabulated in table-4-3 from the waveform of active and reactive power of the grid, PV inverter, and loads, as depicted in Figure 4-9. The PCC voltages, grid currents, PV inverter currents, and load currents are observed for the performance assessment of multipurpose single-stage PV system, as depicted in Figure 4-9. The PV inverter is connected at PCC with1600W power generation at t= 0.3 seconds, 1300W at t= 0.4 seconds, and 1800W at t= 0.5 seconds. At t= 0.6 seconds, The PV inverter is disconnected from the PCC. The reactive power exchange with utility occurs with the residual operating capacity of PV inverter, i.e., 1200VAR at t= 0.3 seconds, 1519.86 VAR at t= 0.4 seconds, and 871.78VAR at t= 0.5 seconds. At t= 0.6 seconds, the PV inverter is disconnected from PCC, at which the utility grid fulfills the reactive power load demand.

## 4.8.3 Reactive power injection mode [STACOM-Night time, critical day hours, MODE-C]

This control mode ensures a PCC voltage within an acceptable range, i.e.,  $\pm 5\%$  PCC voltage, during both direction power exchanges with utility, sometimes in the day. At night time, PCC voltage regulation is the highest priority; if the PCC voltage is fixed acceptable utility range, then the Secondary objective is to make a unity power factor for the grid. The multipurpose PV system is connected to utility and reactive loads at PCC. The 1800W active power and 1800 VAR reactive power loads are connected at PCC. The dynamic performance evaluation of the multipurpose PV system is tabulated in table-4-4 from the waveform of active and reactive power of the grid, PV inverter, and loads, as depicted in Figure 4-10. The PCC voltages, grid currents, PV inverter currents, and load currents are observed for the performance assessment of multipurpose single-stage PV system. The performance evaluation is carried out without PV-STATCOM (in FULL-STATCOM mode) and with PV-STATCOM (in FULL-STATCOM mode). During the test evaluation without PV-STATCOM (in FULL-STATCOM mode), the utility fulfills the reactive power load demand from t= 0.3 seconds to t = 0.4 seconds (or from t = 0.6 seconds to t = 0.7 seconds) and disconnected PV inverter from PCC.



Figure 4- 10 : Dynamic performance of multipurpose single-stage PV system during Full-STATCOM mode

Time	Action (STATC	Active Power (Watt)			Reactive Power(VAR)			
(Seconds)	OM	PV Grid		Load	PV	Grid	Load	Load
	)	Invert	(Receiving	Deman	Inverter	(Receiving	Demand	Туре
		er	/Suppling)	d		/Suppling)		
0.3 to 0.4	disconnec	0	-1800	+1800	0	-1800	+1800	Inductive
	ted							
0.4 to 0.5	connected	0	-1800	+1800	-1800	0	+1800	
0.5 to 0.6		0	-1800	+1800	-1800	0	+1800	Capactive
0.6 to 0.7	Disconne	0	-1800	+1800	0	-1800	+1800	
	cted							

 Table:4-4: Summary of performance assessment for multipurpose

single stage PV system during Night time

During the test evaluation with PV-STATCOM (in FULL-STATCOM mode), the inductive type load and PV inverter are connected to the utility grid at PCC. In this test, the PV inverter fulfills the reactive power load demand from t= 0.4 seconds to t= 0.5 seconds, and the PV inverter behaves as a capacitive type load. While the capacitive type load demand is fulfilled by PV inverter from t= 0.5 seconds to t= 0.6 seconds and PV inverter act as inductive type load.

### 4.8.3.1 Power Factor Correction

The active load in this simulation is 1500W, whereas the reactive load is altered from inductive to capacitive. The reactive load is initially a 1500VAR inductive type load. Figures 4-11(a) and (b) illustrate the grid, load, and photovoltaic system active and reactive power changes due to load and photovoltaic power variations. Figure 4-11(c) shows the grid power factor, PCC voltage ( $v_{PCC}$ ), and grid current ( $i_{grid}$ ) for phase "A," in the multipurpose single-stage PV inverter's control target being power factor correction. The PV-STATCOM system is interfaced to the grid, and the control objective is set to PV mode at time t=0.3 seconds.

MODELING AND CONTROL OF MULTIPURPOSE SINGLE STAGE GRID TIED THREE PHASE PHOTOVOLTAIC SYSTEM



Figure 4- 11 : Dynamic performance of multipurpose single-stage PV system (PV-STATCOM) during power factor correction

The photovoltaic system output is 400W at this level.

When PV-STATCOM generates solely active electricity, the grid power factor is approximately 0.69. As a result, the voltage at the PCC  $(v_{pcc})$  and the grid current  $(i_{grid})$  are out of phase. The load active power  $(P_{Load})$  is supplied by both the grid (Pgrid) and a photovoltaic-STATCOM system (Pinverter), whereas the majority of the load reactive power ( $Q_{load}$ ) is supplied by the grid ( $Q_{grid}$ ).At t=0.4 seconds, the controller enters power factor correction mode and utilizes the remaining capacity of the inverter to restore the power factor to unity. The controller increases the grid power factor from 0.69 to unity. As a result, following a transient, the PCC voltage  $(v_{pcc})$  and the grid current  $(i_{grid})$  become phase-locked. PVSTATCOM exchanges reactive power equal to the reactive power needs of the load in order to enhance power factor. As a result, the reactive power of PV-STATCOM (Qinverter), equals (Q<sub>load</sub>), and the reactive power of the grid (Q<sub>grid</sub>) decreases to zero. Additionally, the results indicate that improving the power factor of a multipurpose single-stage photovoltaic inverter has little effect on active power output. In other words, during power factor adjustment, the active power output of PV-STATCOM (Pinverter) maintains 400W. Thus, the successful decoupling of the active and reactive power controllers is proved.

# 4.9 Dynamic performance assessment of control approach for multipurpose single-stage grid connected system

The simulation results are carried out to conclude the effectiveness of the control approach for multipurpose single-stage grid-connected system in the following manner: During the daytime, Mode A is operated when the no-load or linear load is connected to the utility grid while Mode B is operated when the non-linear load is attached to the point of common coupling (PCC). In this section, the remaining capacity of the inverter is used to exchange reactive power in Mode B. Hence, this controller mode is also known as the "Partial PV-STATCOM" mode. In other words, the conventional PV system operated as a STATCOM utilizing its partial inverter capacity in the form of reactive power support to ensure unity power factor (Power factor correction, PFC mode) at the grid side during daytime. Figure 4-12 illustrate that the utility grid is only interfaced with PV inverter up-to time instant t=0.3

seconds, i.e., Mode A, the capacitive load is connected at the point of common coupling from the time instant t = 0.3 to 0.5 seconds, and the load shifted to inductive load after time instant t= 0.5 seconds. At t= 0.85 i.e., Mode B. The solar isolation/irradiance is varied from  $1000 \frac{W}{m^2}$  to  $500 \frac{W}{m^2}$ . from time instant t =0.3 to t =0.7 seconds, and again to  $1000 \frac{W}{m^2}$  at t= 0.7 seconds. The non-linear load is shifted from Capacitive Load to inductive load with the rating P<sub>load</sub>= 500W and Q<sub>load</sub>= 1500VA at the time instant t =0.5 seconds to observe the dynamic stability of the system.

From simulation results depicted in Figure 4-12, it is observed that:

- At time instant t ≤ 0.2 seconds, the multipurpose PV system operates active power injection mode(Mode A)and only inject active power (2500W)into utility grid at maximum power point using MPPT algorithm on the inverter, and inverter currents and PCC voltages are 180° out of phase in the mode A. It is intentionally Mode A, and Mode B simulated sequentially to verify the performance of the control algorithm during no-load conditions to reactive load conditions.
- 2. At time instant between t= 0.3 seconds and t = 0.5 seconds, the active power and the reactive power demand of capacitive load is entirely served by the multipurpose PV system and operated in active and reactive power injection mode (Mode B). Moreover, the surplus active power is injected into the grid after serving a capacitive load and ensures unity power at the utility. The active power injection is dependent on available solar irradiance and extracted maximum power from PV panels using the MPPT algorithm on the inverter. The PV system is connected to the grid and inductive type load with the rating rating  $P_{Load} =$ 500W and  $Q_{load} = (-1500VA)$  at the point of common coupling; at the same moment, solar irradiance varied from 1000  $\frac{W}{m^2}$  to  $500\frac{W}{m^2}$ . Therefore, the PV system has generated 1200W ( $P_{inv}$ )in which 500W power ( $P_{load}$ ) delivered to the load and remaining power( $P_{grid}$ ) injected to the utility grid while need of negative reactive power( $Q_{load}$ ) to the load provided by the utility grid ( $Q_{grid}$ ). The active power injection is reduced to the 1250W at time instant t=0.5 seconds, further, again increases to the 2500W at time instant t=0.65 seconds due to

change in solar irradiance from  $1000 \frac{W}{m^2}$  to  $500 \frac{W}{m^2}$ , and again increases to  $1000 \frac{W}{m^2}$ . Besides, the grid reactive power support and unity power factor at grid side are maintained along with main objective to inject active power as per availability of solar irradiance on the PV panels. In a single stage grid-tied converter, DC-bus voltage is maintained by the V<sub>dc,ref</sub>, derived from maximum power point tracking (MPPT) algorithm during the conventional-PV mode or the Partial-PV & Partial-STATCOM mode operation.

- 3. At time instant between t= 0.5 seconds and t = 0.7 seconds, the load is switched from capacitive load to inductive load type with the rating  $P_{load} = 500W$  and  $Q_{load} = (+1500VA)$ , instead of negative reactive power ( $Q_{load}$ ) support, now, positive reactive power ( $Q_{load}$ ) provided to the load from utility grid ( $Q_{grid}$ ) rest of the events are identical.
- 4. At time instant t  $\ge 0.7$  seconds, the PV system is again generating 2500W (i.e.  $P_{inv}$ ) due to the change in solar irradiance $(500\frac{w}{m^2}$ to  $1000\frac{W}{m^2}$ ), surplus active PV power injected to utility grid which causes the PCC voltage  $v_{pcc}$  to rise, resulting in a steady state rise in current  $i_{load}$  through constant impedance load, although after a transient. The inverter filter effectively removes the harmonics in the inverter current. The inverter current leads to load current during an inductive type load, whereas lags to load current during a capacitive type load for maintaining grid current at unity power factor in a grid side.
- 5. Modified DSOGI-FLL can eliminate both the harmonics distorted component (100Hz and 300Hz component) and negative sequence from and, further provided to tan-arc PLL block for the detection of phase-angle needed in synchronization of the control system.





Figure 4- 12: Simulation results of MODE A and MODE B
(a) P<sub>pv</sub> (W)and Irriandance (Irr, <sup>w</sup>/<sub>m<sup>2</sup></sub>),(b) V<sub>dc</sub> and V<sub>dc(ref)</sub> (c) PV current (I<sub>dc</sub>),
(d) d-q axis PCC voltage, (e) d-q axis inverter current ,(f) )grid current, inverter current , load current and theta.



Figure 4- 13 : Simulation results of MODE A and MODE B(a)Active Power of P<sub>g</sub>, P<sub>inv</sub> and Irriandance  $(Irr, \frac{w}{m^2})$ ,(b) Reactive Power of Q<sub>g</sub>, Q<sub>inv</sub>, Q<sub>load</sub> (c) PCC voltage (Phase a) and, (d)grid current, inverter current, load current.

The PV inverter gets disconnected from PV panels during the nighttime and entirely behaves as STATCOM. The control objectives of the system are to regulate PCC voltage as the main priority and power factor correction at the grid side when PCC voltage is in an acceptable range. The PCC voltage is reduced due to sizeable inductive type reactive load connected at PCC whereas increased due to either capacitive type reactive load connected at a PCC or active power injected in a grid. During the day, sometimes, PCC voltage is raised above the acceptable range of voltage due to the active power injection from a PV system, and the Multipurpose PV system is switched from Mode B to Mode C (Full STATCOM).





A),, inverter current(Phase A), and load current(Phase A).

The proposed control approach detaches the PV panels from PV inverter in this condition and regulates PCC voltage with in an acceptable range in a one cycle by exchanging reactive power to the PCC. For validation control approach, The PCC Voltage reference is changed from 1.0 p.u. to 0.97 p.u at t =0.3 seconds, further varied from 0.97 p.u. to 1.03 p.u at t= 0.55 seconds, and again from 1.03 p.u to 0.97 p.u at a t= 0.75 seconds.

From simulation results depicted in Figure 4-14 and Figure 4-15, it is observed that:

1 At time t $\leq$ 0.3 seconds, the multipurpose PV system functions in power factor correction mode due to PCC voltage in permissible limit i.e., 1.0 p.u. In PFC enabled MODE C, The PCC voltage and grid current are in phase to ensure unity power at a utility side.

At time 0.55  $\leq$  t  $\leq$  0.75 seconds, the reference PCC voltage is changed to 1.03 p.u. value and tracked PCC voltage within one cycle time. Again, PV inverter (PV-STATCOM) operated either in inductive mode if large capacitive load connected at PCC or capacitive mode for inductive load attached to PCC. It is noted that PV inverter (PV-STATCOM) phase currents are decreased to regulate PCC voltage as per the reference value if capacitive load connected at PCC, as depicted in Figure 4-14, whereas increased in a case of inductive load connected at PCC, as a depicted in Figure 4-15.



Figure 4- 15 : Simulation result of Multipurpose PV system connected to inductive load at PCC (a) Phase A of PCC voltage, and (b)phase A of grid current, inverter current, and load current

3 For the time  $t \ge 0.75$  seconds, now, PV inverter (PV-STATCOM) phase currents is again increased in a case of capacitive load, as observed in Figure 4-14, and decreased during an inductive load, as observed in Figure 4-15, to regulate PCC voltage as per the reference value 0.97 p.u.

### 4.10 Hysteresis Current Controller

The most well-known method of hysteresis control is employed to control current in the single-stage PV system. Thus, the controller reacts rapidly to any deviation from control references, which explains its high gain characteristic. Note that the digital implementation of hysteresis control methods does not guarantee that the ripples in the control variable are within the bounds of a defined hysteresis band. Following that, a direct power control (DPC) for grid-connected applications was developed to directly manage the converter's active and reactive power by selecting the optimal switching state [36]. It has a simple and without PI controller current control structure. It cannot control additional constraints such as capacitor voltage balancing and switching frequency reduction. Moreover, it is not possible to multi-variable cases.



Figure 4-16 : Functional diagram of Hysteresis current controller

### 4.10.1 Mathematical analysis of Hysteresis current controller

Hysteresis control mechanisms have been implemented in either analog or digital form. When the error between control references and control variables passes the positive or negative hysteresis band boundary, a considerable shift in the controller's output (switching state) occurs, as seen in Figure 4-16.



Figure 4-17 : Hysteresis current control mechanisms

The inverter current  $i_{inverter}$  is also known as line filter current  $i_{fact}$ . From Figure 4-17, the reference current at time instant  $t_1$ ,  $t_2$ , and  $t_3$  are denoted as  $i_{f_{ref}}$ ,  $i'_{f_{ref}}$ , and  $i^{"}_{f_{ref}}$ , respectively. During on time, the derivative of filter current is represented, from the Figure 4-17, as:

$$\frac{\mathrm{di}_{f_{act}}}{\mathrm{dt}_{on}} = \frac{(\mathbf{i}'_{f_{ref}} - \mathbf{i}_{f_{ref}}) + 2\mathbf{h}}{\mathbf{t}_{on}}$$
(4.59)

During off time, the derivative of filter current is represented, from the Figure 4-17, as:

$$\frac{\mathrm{di}_{f_{act}}}{\mathrm{dt}_{off}} = \frac{\left(i_{f_{ref}}^{\prime\prime} - i_{f_{ref}}^{\prime}\right) - 2h}{t_{off}}$$
(4.60)


Figure 4-18 : Functional diagram of grid tied system

According to KVL in the single line diagram of grid tied inverter, as shown in Figure 4-18, the inverter voltage can be computed as:

$$\vec{V}_{inv,abc} - \vec{V}_{PCC,abc} = R_f \vec{i}_{inv,abc} + L_f \frac{d\vec{i}_{inv,abc}}{dt}$$

$$= L_f \frac{di_f}{dt} + R_f i_f = L_f \frac{di_g}{dt} + R_f i_g$$
(4.61)

At the instant  $t = t_{on}$ , the equation (4.61) can be re-written as:

$$m_{a} V_{dc} - V_{m} \sin\omega t = L_{f} \frac{di_{fact}}{dt_{on}} + R_{f} i_{f}$$
(4.62)

By substituting equation (4.59) into the equation (4.62), simplified inverter equation is represented as:

$$m_{a} V_{dc} - V_{m} \sin\omega t = L_{f} \{ \frac{(i'_{fref} - i_{fref}) + 2h}{t_{on}} \} + R_{f} i_{f}$$
(4.63)

At time instant  $t = t_{on}$ , the voltage equation of grid tied inverter is represented as:

$$m_a V_{dc} - V_m sin\omega t = L_f \{\frac{2h}{t_{on}}\} + R_f i_f$$
 (4.64)

$$m_a V_{dc} - V_m \sin\omega t - R_f i_f = L_f \{\frac{2h}{t_{on}}\}$$
 (4.65)

The voltage equation of grid tied inverter at off time is represented as:

$$-m_{a} V_{dc} - V_{m} \sin\omega t = L_{f} \frac{di_{fact}}{dt_{off}} + R_{f} i_{f}$$
(4.66)

$$-m_{a} V_{dc} - V_{m} sin\omega t = L_{f} \frac{(i_{f_{ref}}^{\prime\prime} - i_{f_{ref}}^{\prime})^{-2h}}{t_{off}} + R_{f} i_{f}$$
(4.67)

At time instant  $t = t_{off}$ , simplified inverter equation is represented as:

$$-m_{a} V_{dc} - V_{m} \sin\omega t = L_{f} \{ \frac{-2h}{t_{off}} \} + R_{f} i_{f}$$
(4.68)

$$-m_{a} V_{dc} - V_{m} \sin\omega t - R_{f} i_{f} = L_{f} \left\{ \frac{-2h}{t_{off}} \right\}$$

$$(4.69)$$

The on-time and off-time for grid tied inverter can be represented as:

$$t_{\rm on} = \frac{2hL_f}{m_a V_{\rm dc} - (V_{\rm m} \sin\omega t + R_f i_f)}$$
(4.70)

$$t_{off} = \frac{2hL_f}{m_a V_{dc} + (V_m \sin\omega t + R_f i_f)}$$
(4.71)

The time period and switching frequency can be simplified as:

$$T_{\text{period}} = \frac{1}{f_{\text{sw}}} = t_{\text{on}} + t_{\text{off}}$$

$$= \frac{2hL_f}{m_a V_{\text{dc}} - (V_m \sin\omega t + R_f i_f)} + \frac{2hL_f}{m_a V_{\text{dc}} + (V_m \sin\omega t + R_f i_f)}$$
(4.72)

The time period of PWM in context of line inductor, band size, and modulation index can be represented as:

$$T_{\text{period}} = \frac{1}{f_{\text{sw}}} = \frac{4hL_f}{m_a V_{\text{dc}}}$$
(4.73)

The line inductor can be represented as:

$$L_{f} = \frac{m_{a} V_{dc}}{4 h f_{sw}}$$
(4.74)

The analogue controller maintains perfect current ripples inside the hysteresis range; however switching instances are not equal. A discrete system, on the other hand, has a preset sampling time,  $T_s$ . which it uses. Nonetheless, the hysteresis controller works only when  $h > \frac{di_{f,max}}{dt} T_s$ . When current ripples surpass ( $h < \frac{di_{f,max}}{dt}$ ), the controller acts rather like a delta modulation scheme than hysteresis control.

The discrete controller requires 3.3 milliseconds (300 kHz) of sampling time to accurately reproduce the continuous hysteresis behavior. With a sampling time of 330 milliseconds (3 kHz), the operation of a discrete hysteresis controller is quite different from that of a continuous hysteresis controller. A low pass filter must be connected between the inverter and the grid since the output voltage of the inverter is non-sinusoidal (either a 2-level square pulse or a 3-level square pulse). Here, a passive low pass harmonic filter will be used to minimize voltage harmonics and current distortion. L or LC or LCL filters are all possibilities for this particular piece of equipment. For the whole frequency range, the L-type filters attenuate -20 dB/decade. A high inverter switching frequency is required when using an L filter to reduce high order harmonics effectively. This means that switching losses will grow

with increasing frequency. Because the LC filters resonance frequency is affected by grid inductance, using a weak grid is not a good idea. Consequently, the LCL filter type is considered in the existing system. In addition to the frequencies -60 dB/decade attenuation over the resonance frequency, the LCL filter can be used with a reasonably low switching frequency for the provided harmonic attenuation.



Figure 4-19 : Basic block schematic of LCL type filter

The LCL circuit connection between the AC-terminal of single-stage PV system and the grid is shown in Figure 4-19. The output voltage of inverter and grid voltage are denoted as  $v_{inv}$  and  $v_{pcc}$  (or  $v_g$ ).  $L_{inv}$  is the inverter side inductor and  $L_g$  is the grid side inductor;  $C_f$  is the filter capacitor and  $R_d$  is the damping resistor.

From the references [8][66][95][98][100], The line filter inductor  $L_{inv}$  can be computed as:

$$L_{inv} = \frac{V_{dc} \times (1 - m_a) \times m_a}{4 \times f_{switching} \times I_{rated} \times \Delta_{ripple}}$$
(4.75)

The relation between the line filter inductor  $L_{inv}$  and grid inductor  $L_{g}$  are represented as [8][66][95][98][100],:

$$L_{g} = \alpha L_{inv} \tag{4.76}$$

The current harmonics attenuation ratio ( $\alpha$ ) can be represented as[8][66][95][98][100],:

$$\alpha = 1 - \frac{\frac{1}{L_{inv}c_{f}\omega_{res}^{2}}}{\frac{\Delta_{ripple}V_{rated}\omega_{0}}{2\pi^{2}V_{dc}f_{switching}\gamma}}$$
(4.77)

The filter capacitance can be computed as[8][66][95][98][100],:

$$C_{\rm f} = \gamma C_{\rm base\ capacitance} \tag{4.78}$$

The base capacitance and base impedance are computed as[8][66][95][98][100],:

$$C_{\text{base capacitance}} = \frac{1}{\omega_0 Z_{\text{base Impedance}}};$$

$$Z_{\text{base Impedance}} = \frac{V_g^2}{P_{\text{rated output power}}}$$
(4.79)

The damping resistance can be computed as[8][66][95][98][100],:

$$R_{d} = \frac{\omega_{res}}{C_{f}}$$
(4.80)

Hence, the resonance frequency for the PV system can be computed as[8][66][95][98][100],:

$$f_{\rm res} = \frac{1}{2\pi} \sqrt{\frac{L_{\rm inv} + L_g}{L_{\rm inv} L_g C_f}}$$
(4.81)

Prior to selecting the LCL filter parameter, all necessary criteria must be fulfilled. Total filter inductances should be less than 0.1(p.u.) and the resonance frequency should be in the range of:  $10\omega_g \le \omega_{res} \le \frac{\omega_{sw}}{2}$ .

For the stability analysis of LCL filter, the transfer function without damping resistor can be computed as:

$$G(s) = \frac{1}{(L_{inv}L_gC_f)s^3 + (\{L_{inv}+L_g\}C_f)s^2 + (L_{inv}+L_g)s}$$
(4.82)

For the stability analysis of LCL filter, the transfer function with damping resistor can be computed as:

$$G(s) = \frac{1 + R_d C_f}{(L_{inv} L_g C_f) s^3 + (\{L_{inv} + L_g\} C_f) s^2 + (L_{inv} + L_g\} s}$$
(4.83)

By considering grid inductance  $L_2$ , the equation (4.83) is modified as:

$$G(s) = \frac{1 + R_d C_f}{(L_{inv}(L_g + L_2)C_f)s^3 + (\{L_{inv} + L_g + L_2\}C_f)s^2 + (L_{inv} + L_g + L_2)s}$$
(4.84)

Figure 4-20 shows that the LCL filter has a higher attenuation level even at lower frequencies. The value of the resonance peak depends on the frequency of the system. Using the damping resistor as a resonance peak damper, as shown in Figure 4-21, reducing the resonance frequency by a factor of two while simultaneously increasing the grid inductance's impact on resonance frequency values is possible. When grid impedance varies, we must thus monitor it constantly and shut off the inverter system if it goes outside a specified range.



Figure 4- 21 : Bode plot for LCL type filter considering different conditions

#### 4.10.2 Reference Current Generation using instantaneous power Theory

The compensation scheme described here can be used to either a three-phase, threewire system or a three-phase, four-wire system. However, in either situation, the aim is to provide balanced supply current so that the zero sequence component of the current is zero in both cases and described below:

$$i_{s_a} + i_{s_b} + i_{s_c} = 0 \tag{4.85}$$

Because it is assumed that the power factor angle is zero, it follows that the instantaneous reactive power delivered by the source is also zero. When this angle is greater than zero, on the other hand, the source gives reactive power which is equals to  $\tan \frac{\phi}{3}$  times the amount of instantaneous power, where  $\phi$  is phase angle between source voltage and source current.



Figure 4- 22 : Control mechanism of single stage grid tied PV system in abc reference frame

In a balanced three-phase circuit, the instantaneous power is constant, however in an unbalanced circuit; the instantaneous power has a double frequency component in addition to the dc value. This is accomplished by the use of a voltage source converter, which delivers the double frequency component such that the source supplies the dc value of the load power. The active power of load can be computed as:

$$v_{s_a} \, i_{s_a} + v_{s_b} \, i_{s_b} + v_{s_c} \, i_{s_c} = P_{Load_{ava}} \tag{4.86}$$

It is possible to determine the average load power by employing a moving average (MA) filter with an averaging time of half a cycle. The harmonic component in the load current does not require any real power to be supplied by the source current. The role of inverter is activated at the end of a single cycle of operation. Moreover, at the end of three cycles, the inverter operates at unity power factor mode.

The AC components of load currents are computed as:

$$\mathbf{i}_{Load_a} = \mathbf{i}_{Load_a} - \mathbf{i}_{Load_{avg, a}} \tag{4.87}$$

$$\tilde{i}_{Load_b} = i_{Load_b} - i_{Load_{avg, b}}$$

$$(4.88)$$

$$\tilde{i}_{Load_c} = i_{Load_c} - i_{Load_{avg,c}}$$

$$(4.89)$$

The reference values of currents for the hysteresis current controller are computed as:

$$i_{ref_a}^* = \tilde{i}_{Load_a} + \left(P_{loss} + \frac{2V_{PV}I_{PV}}{3V_m}\right)\frac{v_a}{V_m}$$
(4.90)

$$i_{ref b}^{*} = \tilde{i}_{Load_{b}} + \left(P_{loss} + \frac{2V_{PV}I_{PV}}{3V_{m}}\right)\frac{v_{b}}{V_{m}}$$

$$(4.91)$$

$$i_{ref_c}^* = \tilde{i}_{Load_c} + \left(P_{loss} + \frac{2V_{PV}I_{PV}}{3V_m}\right)\frac{v_c}{V_m}$$
(4.92)

The error between the reference value of DC-bus and actual value of DC-bus is computed in the equation (4.93). The  $P_{loss}$  is computed in the equation (4.94) for extracting the active power from PV panels.

$$\varepsilon(n) = V_{dc_{ref}}(n) - V_{dc}(n) \tag{4.93}$$

$$P_{loss} = V_{dc}(n) + K_P \left[\varepsilon(n) - \varepsilon(n-1)\right] + K_i T_s \varepsilon(n)$$
(4.94)

$$v_{a_{P,U}} = \frac{v_a}{v_m}$$
;  $v_{b_{P,U}} = \frac{v_b}{v_m}$ ;  $v_{c_{P,U}} = \frac{v_c}{v_m}$ ; (4.95)

Prior to the connection of the PV system, both the load power and the source power have the same magnitude and are oscillatory in their output. The supply power becomes flat as soon as the inverter is connected, and delivers the oscillating component after it has been linked. Because the action of the PV system is immediate, it should be highlighted that optimal current sources are used to achieve desire result. Once the load is altered to balanced values at 0.5 s, the source and load powers become flat, and the inverter power and neutral voltage both become zero as a result of the change.



Figure 4- 23 : Simulation result of Multipurpose PV system connected to nonlinear load at PCC (a) PCC voltage, (b) grid currents, (c) inverter currents, (d) load currents, and (e) DC-bus voltage

This is demonstrated in Figure 4-23, which depicts the three source voltages and currents, as well as the inverter currents, respectively. The operation of the source at unity power factor, as well as the balancing of source currents, may be seen in Figure 4-23(a) and (b). According to Figure 4-23(e) when the solar irradiance is changed, the inverter is operative in same manner while when load is shifted that time inverter currents become balanced as a result of the load being balanced, as observed in

Figure 4-23(c) and (d). The operation of the inverter when it is turned on in 20 milliseconds is immediate because it is created from ideal current sources, which is something to keep in mind. Furthermore, because of the load inductances, when the load is changed, the transients last around 2 cycles before they die out. The voltage source converter(PV inverter) has no influence on the amount of time required by the load to settle. It should be noted that after the PV inverter is attached, neither the load power nor the neutral voltage change.

#### 4.11 Current-Sensor less MPPT In Grid-tied Photovoltaic System

Reference (87) presented their works on current-sensor less power-angle based MPPT control for single-stage grid-connected System. The voltage source inverters with current sensors and power angle based MPPT; these researchers had proposed a novel quantity for current-sensor less power-angle based MPPT (VSIs). The suggested control scheme, which MPPT eliminates the need of current sensor and instead relies solely on a voltage sensor: Instead of measuring current, the sine value of the power-angle sensor (the phase angle between the inverter output voltage and the power grid voltage) is computed for MPPT. The usage of current sensors accounts for a significant portion of the costs and complexity challenges (such as failure in currents sensor, calibration error of sensor, quantization error of ADC etc.) associated with MPPTs during failure in currents sensor. By taking into account the hardware cost and the simplicity, control system of grid connected PV system had given satisfactory performance.

#### 4.11.1 Conceptual framework and description of Current-Sensor less MPPT in Grid-tied Photovoltaic System

The control system of PV system is capable to exchange active and reactive power to the utility. The MPPT algorithm is a part of controls system, which is employed to extract maximum power from PV panels and injected to utility through inverter. Figure (4-4) of section 4.3 indicates that in order to calculate the maximum power

point of a PV panel, both voltage and current must be known. The maximum amount of power can be extracted by sensing voltage and current in real time. During the day, the PV system's output voltage is stable throughout its operational range. As a result, the power injected by PV inverter ( $P_{inv}$ ) is inversely proportional to the current variation. Modified-MPPT can be achieved from a PV system if a correlation can be established between the PV current and the output AC current (which is being detected to build a close loop).AC currents and DC link voltage are used in the MPPT algorithm (instead of the PV current).

# 4.11.1.1 Mathematical analysis of sine-angle based MPPT for Single-Stage PV system

There is an equivalent diagram of a grid-connected generation system in Figure4-24 to describe the power injection principle from a generator into the electricity grid. Figure 4-24(b) shows a vector diagram of how output currents can be utilized to build a PV current reference that can be used in the MPPT method to calculate maximum power. As a result of this research, a constant multiplication factor has been developed between PV current and AC current for any given available power. Thus, using the available current reference and PV voltage, the maximum power may be determined.



Figure 4- 24 : Functional and Phasor diagram of grid tied PV system during power injection into a grid

From phasor diagram shown in the figure 4-24, the active and reactive power of grid tied system, are computed as:

$$P_{inv} = \frac{v_{inv}v_{pcc}\sin\delta}{X_f} \tag{4.96}$$

$$Q_{inv} = \frac{v_{pcc}^2 - v_{inv} v_{pcc} \cos \delta}{x_f} \tag{4.97}$$

The relationship of inverter voltage, modulation index, and DC-bus voltage or PV panel voltage is described as:

$$v_{inv} = m_a \frac{v_{DC}}{2} = m_a \frac{v_{PV}}{2} \tag{4.98}$$

The Power of PV panels can be described as:



Figure 4- 25 : Power curve for PV panel using sin angle based DC current sensor-less MPPT

The DC link voltage or PV voltage is directly proportional to inverter voltage (i.e.  $V_{PV} \propto v_{inv}$ ) by considering following terms as constant terms : grid voltages, filter reactance, modulation index, and hardware configuration. The active power relation given in equation is re-written as:

$$P_{\rm inv} \propto (V_{\rm PV} \times \sin \delta) \tag{4.100}$$

The sine value of the power-angle  $(\sin \delta)$  can be used to substitute the PV current in order to inject maximum power through inverter to grid using a modified-MPPT algorithm[87].

#### 4.11.1.2 Modified-INC MPPT algorithm

The basic principles of the INC MPPT algorithm can be summarized thusly: According to the PV module power curve illustrated in Figure (4-4) and Figure (4-25), the derivative of PV module power  $P_{PV}$  with respect to its voltage is positive prior to reaching the MPP, then zero, and then negative after passing through the MPP.

$$\frac{dP_{PV}}{dV_{PV}} \propto \left\{ \frac{d((V_{PV} \times \sin \delta))}{dV_{PV}} \right\} \propto \left\{ (V_{PV} \times \frac{d(\sin \delta))}{dV_{PV}} + (\sin \delta) \right\}$$
(4.102)

The  $P_{PV}$  derivation is given in equation (4.102), which results error (e) signal. It is

given as

$$e = \frac{d(\sin\delta)}{dV_{PV}} + \frac{\sin\delta}{V_{PV}}$$
(4.103)

It is then possible to keep track of the maximum power point by watching the actuating error, then following the following rule:

$$\delta(n) = \begin{cases} \delta(n-1) + \Delta\delta, \ e < 0\\ \delta(n-1) - \Delta\delta, \ e \ge 0 \end{cases}$$
(4.104)

Using the modified INC approach [86-92], the slope of the PV array power curve vs voltage is zero at the maximum power point (MPP) of the array. The accuracy requirements at steady state and the MPPT response time dictate the size of the iteration step for the INC MPPT algorithm. It is therefore necessary to evaluate a trade-off between dynamic and steady-state reactions at the corresponding design stage.

#### 4.12 Modified DC Current-Sensor less MPPT for Grid-tied Photovoltaic System in Synchronous reference frame

Power of photovoltaic system ought to be equal to the output power of inverter at the VSI AC-side terminals, which is equal to the grid power, omitting the inverter loss and filter power loss, based on the power balance of both inverter sides in steady condition.

$$P_{PV}(=V_{PV} \times I_{PV}) = P_{inv} \left(=\frac{3V_d I_d}{2}\right)$$
(4.105)

The power of the PV panels is directly proportional to ac current component d-axis coordinate ( $P_{PV} \propto i_d$ ) by considering following terms as constant terms : balanced

grid voltages( $v_d = constant$ ), fine grid synchronization ( $v_q = 0$ ), constant filter

reactance. It is described as:

$$P_{\rm PV} \propto I_{\rm d} \tag{4.106}$$

The power variation of PV panels  $P_{PV}$  with voltage  $V_{dc}$  is calculable as follows:

$$\frac{dP_{PV}}{dV_{dc}} = \left\{ \frac{3}{2} \frac{d(V_d I_d)}{dV_{PV}} \right\} = \left\{ V_d \frac{3}{2} \frac{d(I_d)}{dV_{PV}} \right\} + \left\{ I_d \frac{3}{2} \frac{d(V_d)}{dV_{PV}} \right\}$$
(4.107)

For the balanced grid voltages, d-axis component of voltage vector is constant and equation is simplified as:

$$\frac{\mathrm{d}P_{\mathrm{PV}}}{\mathrm{d}V_{\mathrm{dc}}} = \left\{ V_{\mathrm{d}} \frac{3}{2} \frac{\mathrm{d}(\mathrm{I}_{\mathrm{d}})}{\mathrm{d}V_{\mathrm{PV}}} \right\} \propto \frac{\mathrm{d}(\mathrm{I}_{\mathrm{d}})}{\mathrm{d}V_{\mathrm{PV}}} \tag{4.108}$$

At kth sample, the DC-link voltage and d-axis inverter current are computed as:

$$\Delta V_{dc}(k) = V_{dc}(k) - V_{dc}(k-1)$$
(4.109)

$$\Delta i_{d}(k) = i_{d}(k) - i_{d}(k-1)$$
(4.110)

When  $I_d \neq 0$ , it means there is change in climate condition. According to equation (4.108), if  $\Delta I_d > 0$ , then  $\frac{\Delta I_d}{\Delta V_{dc}} > 0$ , and the MPPT reference voltage is increased to bring the operating point towards the maximum power point. The reference voltage  $V_{dc_{ref}}(k)$  for outer voltage control loop is computed by modified MPPT algorithm as per the equation.

$$V_{dc_{ref}}(k) = \frac{V_{dc_{ref}}(k) + \Delta V_{step-size}}{V_{dc_{ref}}(k) - \Delta V_{step-size}} (\Delta I_d > 0 \& \Delta V_{dc} > 0) \\ ||(\Delta I_d < 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d < 0 \& \Delta V_{dc} > 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||(\Delta I_d > 0 \& \Delta V_{dc} < 0) \\ ||($$

While $\Delta I_d < 0$ , then  $\frac{\Delta I_d}{\Delta V_{dc}} < 0$ , and the MPPT reference voltage must be decreased in order to bring the operating point toward the maximum power point, as shown in Figure 4-26. The MPPT's step size affects how quickly the MPP is monitored.



Figure 4- 26 : Power curve for PV panel using modified dc current sensor-less MPPT



Figure 4- 27 : Tracking the change in V<sub>PV</sub> [Upper Trace: Voltage Generated by PV Array (Red): X axis: 1 Div. = 20 mSec, Y axis : 1 Div. = 5 V; Lower Trace: Reference Voltage Generated by MPPT Algorithm (Blue): X axis : 1 Div. = 20 mSec, Y axis : 1 Div. = 5 V]

In order to get faster tracking, one can use larger increments, however the system may not run at the MPP perfectly, instead oscillating around it, and this results in low efficiency. When the MPPT is set to a small increment, the situation is the opposite. For the fixed step-size MPPT, a trade-off between dynamics and oscillations is necessary. Here, Figure 4-27 depicts the PV voltage generated by PV Panels tracks MPPT reference generated by modified DC current sensor-less MPPT algorithm.

Now from Figure 4-27, it can be seen that MPPT reference voltage tracks the PV panel voltage accurately. From this the behavior of the algorithm at the standard temperature (25°C) and irradiation (1000  $\frac{W}{m^2}$ ) can be analyzed. According to the error generated by MPPT voltage reference and sensed PV array voltage is fed to PI controller of outer voltage control loop , which determines active current will be injected to utility grid and constant DC link voltage is maintained.





Figure 4- 28 : Dynamic performance of Multipurpose PV system using a modified DC current sensor-less MPPT and synchronous frame current control

Figure 4-28 (a) illustrate the variation in solar power  $P_{PV}$  as per the variation in solar irradiance. The solar isolation/irradiance is varied from  $1000 \frac{W}{m^2}$  to  $500 \frac{W}{m^2}$  from time instant t =0.65 to t =0.65 seconds, again to  $800 \frac{W}{m^2}$  from time instant t =0.65 to t =0.8

seconds, and further shifted to  $1000 \frac{W}{m^2}$  at t =0.8 seconds, depicted in Figure 4-28 (a). Figure 4-28(a) also demonstrate voltages and currents in dq reference frame. Figure 4-28(b) demonstrate that the utility grid is only interfaced with PV inverter up-to time instant t=0.3 seconds, then inductive load is connected at point of common coupling from time instant t = 0.3 to 0.5 seconds, and load shifted to capacitive load after time instant t= 0.5 seconds, as . From simulation results depicted in the Figure 4-28(b) and (c), it is observed that the multipurpose PV system inject only active power (2500W)into utility grid at maximum power point using modified MPPT algorithm at time instant t  $\leq 0.3$  seconds. At time instant between t= 0.5 seconds and t = 0.65 seconds, the active power decreased due to abrupt change in solar irradiance from  $1000 \frac{W}{m^2}$  to  $500 \frac{W}{m^2}$ . While, the active power increased due to increase in solar irradiance from 500  $\frac{W}{m^2}$  to 1000  $\frac{W}{m^2}$  again at time instant between t= 0.65 seconds and t = 0.8 seconds, as depicted in Figure 4-28. The modified DC current sensor-less MPPT algorithm uses sensed DC-bus voltage and d-axis ac current component of inverter for computing direction in which step size is added to reach maximum power point, as depicted in Figure 4-28. The variation in d-axis current component of inverter in synchronous frame is directly influence by change in solar irradiance, which fact is utilized to employ DC current sensor-less MPPT algorithm, as depicted in Figure 4-28. From the simulation result as well as mathematical analysis, it is concluded that maximum power point extracted from PV panel is possible without using dc current sensor.

#### 4.13 Conclusion

This chapter discussed modeling a multipurpose single-stage grid-tied PV system using Simulink/MATLAB. The single-stage grid-tied PV system at PCC serves various purposes and is connected to the utility grid and multiple reactive loads. A single-stage grid-tied PV system conventional control is adjusted to inject active power into the grid together with reactive power support to accomplish either unity power factor at utility or PCC to operate as Partial PV & Partial-STATCOM or Full STATCOM mode, depending on the system's requirements. The partial STATCOM operation mode control objectives include power factor correction, voltage

regulation, and reactive power management. For complete STATCOM operation, the primary goal of control is voltage control. The software simulation studies have verified the controller performance in both modes of operation. If the controller is in partial STATCOM mode, it provides reactive power to the load in order to keep the grid power factor at unity. For demonstration purposes, voltage control modifies the photovoltaic system's active power output to demonstrate the successful decoupling of the active and reactive power controllers. When a load is abruptly applied, the controller disconnects the solar panels from the inverter and manages the voltage using the inverter's full capability. The single-stage grid-tied PV system is designed and simulated using a modified DC current sensor without MPPT to attain the desired performance.

This chapter presents the experimental lab setup for the multipurpose single-stage grid-tied PV system to carry out test results in different situations. Here, it also demonstrates discrete control system implementation for the multipurpose single-stage grid-tied PV system using WAIJUNG block-set of Simulink/ MATLAB on low-cost digital signal processor base 32-bit ARM core STM32F407VG microcontroller. This chapter describes the design, development, and deployment of a multipurpose grid-tied photovoltaic (PV) system in great depth. Because the inverter is a critical component of a PV system, a laboratory-developed single-stage three-phase inverter is used to reduce the overall cost of a Solar PV system significantly. The suggested multipurpose single-stage grid-tied PV system into the electric grid and acts as a PV-STATCOM by providing reactive power support to the utility grid. The proposed design is tested on a laboratory-created prototype to see if it works under different test cases.

#### 5.1 Concept of Model based Programming in Simulink/MATLAB using WAIJUNG block-set

It is described in this section the procedures that must be followed during the construction of the model in Simulink/MATLAB for the microcontroller unit. To begin developing a model base program (target Simulink file), open and save a new file in Simulink/MATLAB. The WAIJUNG block-set has many prefabricated blocks that can be used to create a variety of different models. These prefabricated blocks can be turned directly into C code for the specified microcontroller series, whose Simulink/MATLAB third-party supports are available and required. To create any model using the WAIJUNG block-set in Simulink/MATLAB, drag and drop the preconfigured units/ blocks from the WAIJUNG library. Any model design of grid-tied or motor drive application using a voltage source converter must include the following three fundamental blocks:

a) Target setup block: The target setup block defines the compiler, the specific microcontroller IC number, and the base sampling time. This is true for any model built for a particular microcontroller unit. To add this block, open the following place in the library: Click and drag the Target Setup block in WAIJUNG block-set/STM32F4xx Target/Device Configuration. During code generation, the STM32F407VG microcontroller unit is associated with the MDK-ARM compiler, target Simulink file, ST-Link programmer or debugger, and finally, dump code into the microcontroller. Consequently, select the appropriate choice of discrete blocks for the design of control logic from the pull-down menu in the dialogue box in the target Simulink file.

b) Control Logic blocks: In order to construct control logic for any customizable applications, Simulink/MATLAB blocks such as the pulse generator block, sine generator block, and other similar blocks are used in the target Simulink. These blocks establish a model's control logic and generate the necessary control signals/firing pulses for any application.

c) Input/output blocks: To transfer the generated control signals to the appropriate GPIOs for further transmission, the predefined Input/ Output blocks included in the WAIJUNG block-set are used. To add this/these blocks, the following library location must be opened: Click and drag the required block/s from the WAIJUNG block-set/STM32F4xx Target/On-chip peripherals. The DAC and ADC can be used to create a closed-loop control system. Additionally, the WAIJUNG block-set includes a pulse width modulation (PWM) block, an advanced PWM block (inherent dead band of 1 micro-second between complementary pulses), and a timer block for constructing sophisticated models. Using the model configuration parameter, the discrete model solver should be selected in Simulink/MATLAB. The model is now ready to be dumped into the STM32F407VG ARM cortex microcontroller, which can be done by clicking on the build command icon in the Simulink file. The build command can be issued in three ways: 1) Select the code menu. C/C++ source code 2) Select the Build model option, or 3) press control + B. The code generation process has gone through the following procedure: produce

source code, pack source code, compile source code, connect to target, Erase the entire chip, download and verify, and run the target. These procedures are carried out automatically when the build command is used. After completing these processes, the target file hex code is dumped into the microcontroller. This concludes the process of generating gate signals. These gate signals are gathered on the GPIO pins and routed via jumpers to the power card.

#### 5.1.1 Overview of ARM Cortex M4 STM32F4 microcontroller

This section describes a customizable and cost-effective experimental development for the grid-tied system in context to the microcontroller. Additionally, the controller selected determines the complexity of generating gate signals. For traditional DSPs and microcontrollers like the 8051, there must be well-versed in writing code in order to generate gate signals. Alternatively, the gate signals can be generated using an ARM Cortex M4 microcontroller, WAIJUNG block-set, and Keil. Using the Simulink/MATLAB models, the WAIJUNG block-set used target Simulink file is automatically translated to C and then dumped into the microcontroller memory. Simulink/MATLAB WAIJUNG block-set blocks can be directly used to generate the signals, eliminating the need for coding [11]. [10, 11] This study emphasizes lowcost hardware design. For a single piece of hardware setup (STM32F407VG, IGBTbased power card, current and voltage sensors, and three-phase driver card included), the cost is relatively low. Additionally, the same hardware configuration may be utilized to build a variety of other experiments or carry out different test cases of the grid-tied PV system. Arm Cortex M4 32-bit microcontroller from STMicroelectronics STM32F407xx is designed for high-efficiency digital processing and has a wide range of peripherals. 210 million instructions per second (MIPS) may be processed, and a single cycle multiplication and accumulation can be performed. This microcontroller has several valuable features, including 1) A LQFP100 package with 1MB of Flash memory and 192KB of RAM operates at a maximum frequency of 168 MHz, resulting in a maximum throughput of 210 MIPs. St-LINK/V2 hardware debugger onboard for in-depth hardware troubleshooting (SWD connector for programming and debugging); the A/D converters are 3x12-bit, 2.4 million samples per second, while the D/A converters are 2x12-bit, 2.4 million samples per

second. Direct memory access (DMA) controller with FIFOs and burst support for 16 streams, general-purpose twelve 16-bit and two 32-bit timers up to 168MHz, each with 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder inputs, and up to 17 totals. A total of six additional PWM channels with adjustable dead time insertion are available. More than a dozen different communication interfaces, such as UART and SPI. A maximum of 140 GPIOs (general purpose input and output) are supported, as well as ten 5V-tolerant GPIO pins, Floating-point unit [11], and Incremental Encoder interface [12] are included in this section. ARM Cortex 32-bit M4 microcontroller is used as the controller board since it is less expensive and easier to program.

#### 5.2 Experimental Modeling of Multipurpose Single-Stage PV System in MATLAB/Simulink

The multipurpose single-stage PV inverter controller model is designed in Simulink/MATLAB software and implemented on the 32-bit ARM cortex microcontroller. In the Simulink target model, sensed three-phase inverter current, load currents, and voltage signals are assigned to specific analog-to-digital (ADC) channels. In other words, DC-bus voltage, the inverter current, load current, and PCC voltage are read by ADC channels from sensor cards. The controller design is built on the mathematical model described in chapter 4. The simplified multipurpose single-stage PV inverter controller in Simulink are explained in comprehensive

#### 5.2.1 Discrete control system in synchronous reference frame for Single-stage grid tied PV system using WAIJUNG code

The Discrete control system of a grid-tied PV system is modeled and realized in Simulink/MATLAB environment using WAIJUNG block-set, as depicted in Figure 5-1. The target Simulink STM32F4 model presented in Figure5-1 is configured to read DC-bus voltage, three-phase voltages, three-phase load currents, and three-phase inverter currents.



Figure 5-1: Target Simulink/MATLAB diagram for the control system of Multipurpose Single-stage grid tied PV System

The target Simulink STM32F4 model of a discrete control system for grid-tied PV system is realized by the following key blocks: (1) Analog to digital conversion block to read DC-link voltage, three-phase voltages, three-phase inverter currents, and three-phase currents, (2) DC signal conditioning, (3)Transformation phase voltages, inverter currents, and load currents from three-phase system to synchronous frame,(4) Grid voltage phase-angle extraction for grid synchronization,(5) DC-link voltage reference computation from MPPT, (6) The outer voltage control loop,

(7)D-axis inner current control loop, (8) Q-axis inner current control loop, (9) PWM signals generation, (10) ON/OFF control block, and (11) Protection Block. Furthermore, a difference of d-axis current reference and actual d-axis current component as input of PI regulator decides the amount of active current injected to the utility grid by generating PWM signals using space vector modulation technique.

#### 5.2.2 Design or Implementation of a signal conditioning circuit

In a signal conditioning circuit, current and voltage transducers are used in simultaneously. In the present work, a DC voltage transducer is hall effect based sensor, whereas AC voltage sensors and AC current sensors circuit are designed using potential transformer, which were used to sense and transform high power quantities as, such as three-phase currents and voltages, into low-level analogue voltage signals in the range of +3V DC or 0V to 3V AC signal by DC voltage sensor and AC voltage and current sensors respectively. The Hall Effect voltage sensor provides galvanic isolation between the primary circuits (which are high power) and secondary circuits. Figure 5-2 shows a schematic block diagram of the Hall Effect voltage transducer along with op-amp based amplifier with amplification gain(Again).In laboratory prototype, voltages have been reduced from 250V to 3V for the ADC pin of microcontroller. The sensed output is retrieved from the measurement at output of hall sensor, which is actually output of amplifier. The voltage transducer, for example, requires a supply voltage of 15 V and can measure both AC and DC voltages in the range of 10–500 V. Notably, the input resistance  $R_{in}$  (Potentiometer, 100K $\Omega$ ) should be chosen so that the output measurement resistance  $R_{out}$  (Potentiometer, 1K $\Omega$ ) falls within the range of 100–300 as described in the datasheet for hall base voltage transducer. For a DC-link voltage 250 volt and  $R_{in}$  is set to value  $100 \text{K}\Omega$  ,  $I_{in}$  is computed as follows:

$$I_{in} = \frac{V_{dc_{sensed}}}{R_{in}} = \frac{250}{50 \times 10^3} = 5mA$$
(5.1)

Furthermore, the amplification gain of op-amp base amplifier is gain ( $A_{gain} = 3$ ).



Figure 5-2: Schematic Diagram of (a) voltage Hall sensor circuit, (b) AC voltage sensor circuit using Potential divider and voltage transformer, and(c) current transformer circuit with DC-bias

Consequently, I<sub>out</sub> is calculated as follows:

$$I_{out} = A_{gain} \times I_{in} = 3 \times 5mA = 15mA$$
(5.2)

Assumptions are obtained for the output measurement resistance  $R_{out}$  (Potentiometer, 1K $\Omega$ ) to obtain 3 V when the 250 V input is applied. The output measurement resistance  $R_{out}$  is computed as:

$$R_{out} = \frac{V_{output}}{I_{out}} = \frac{3V}{15mA} = 200\Omega$$
(5.3)

The output measurement resistance  $R_{out}$  is set around 200 $\Omega$  in a potentiometer. The three-phase voltages are sensed with the help of three Potential Transformers (PTs). Figure 5-2(b) shows the schematic of the AC voltage sensing arrangement in which three single-phase potential transformers of rating 230/9 volts are used. Since all the phases are identical, only a single phase arrangement is shown in Figure 5-2. The voltage divider method is used to reduce the AC voltage output from those potential transformers. DC offset is required in this case to convert sensed voltages into positive values (unipolar signal); this has to be done because the input of ADC of the microcontroller must be positive (or unipolar). The value required for this DC offset is itself taken from the microcontroller. Similarly, the voltage divider method is used in the DC offset circuit. The three-phase currents are sensed with the help of three Current Transformers (CTs). Figure 5-2(c) shows the schematic of the AC current sensing arrangement in which three single-phase current transformers of rating 10A/500mA are used. Burden resistors are connected across CTs. As all three phases are identical, only a single-phase arrangement is shown in Figure 5-2. The voltage divider method is used to reduce the voltage output across the burden resistor. Similarly, as in the AC voltage sensing circuit, the voltage divider method in the DC offset circuit is used to convert sensed voltages into positive values; this has to be done because the input of the ADC of the microcontroller must be positive.

#### 5.2.2.1 Brief description of Analog to Digital PINs in WAIJUNG Block-set

The Analog-to-Digital Converter (ADC) converts analog voltage/ current signal into a digital signal. The STM32F407VG microcontroller has three 12-bit ADCs. The ADC offers sample rates of 2.4 million per second and 12-bit resolution. It is feasible

to sample all three ADCs simultaneously on the ARM cortex STM32F407 microcontroller 24 channels. Control blocks can be built using the ADC and DAC for closed-loop applications. In Figure 5.3, the regular ADC units read the voltage/ current of configured pins and produce a value ranging from 0 to 4095 based on the reading. There is no voltage at the input side of the ADC pins, as indicated by the output ADC value of 'Zero'. However, the output ADC value of 4095 implies that there is 3 volts at the input side. Thus, if the output is multiplied by the gain 3/4095, then should get actual value of analog voltage inside the code for the control system. As previously indicated, the Discovery board requires a voltage supply between 0 and +3 volts. Voltages that are either too positive (more than +3.3 V) or negative voltage can damage the board.



# Analog to digital conversion



The Pins AN0, AN1 are configured for sensed DC-bus voltage and reference value of DC-bus (instead of MPPT algorithm), which can be varied by the 0V to 3V potentiometer. The ADC pins AN2,AN3and AN5 are configured for three phase inverter currents, whereas load current are configured on ADC pins AN12,

AN13,AN14.As depicted in Figure 5-4, the pre-scaler value is chosen to 2.



Figure 5-4: Configuration view and Pin assignment of A/D converter in the target Simulink

The reference value of DC-bus can be varied from 200V to 300V at the ADC pin AN1 by multiplying the  $gain \frac{300}{4095}$  and saturation block make sure the variation in the range of 200V to 300V. The sensed three phase inverter currents and sensed three phase load currents are multiplied by  $gain \frac{3}{4095}$  value inside code, as depicted in Figure 5-4.

#### 5.2.2.2 Description of Control block (start/stop) in WAIJUNG blockset

The control block plays a crucial role in controlling the grid-tied PV system. Here, two common ground push switches are connected to the PD7 for the 'ON' or 'OFF' either start or stop gating pulses from the microcontroller as well as reset the PI controller, and PD5 for the shifting from fixed DC-bus reference voltage (250V) to varying DC-bus reference voltage from 200V to 300V through the external potentiometer. The pin PD15 of the microcontroller is interfaced with a common anode base LED, which is used as a status indication of PD5. If PD5 is '1', then fix DC-bus reference voltage (250V) is given to the outer loop voltage control of grid-tied PV system, whereas PD5 is '0', then variable DC-bus reference voltage from

200V to 300V through the potentiometer is given to the outer loop voltage control of grid-tied PV system. Here, PD5 and PD7 are configured as input switches and used in Toggle mode for the stop/ start of the control system.



Figure 5-5: Configuration schematic of Start/Stop of gating pulses control in the target Simulink

#### 5.2.2.3 Description of DC-bus voltage signal conditioning in WAIJUNG block-set

An actual DC-bus voltage is sensed, which is scaled from 250 volt to 3volt using hall sensor and signal conditioning circuit, and fed to ADC pin of microcontroller. Inside the model base program code, sensed DC-bus voltage is converted into actual value of DC-bus voltage by multiplying gain of  $\frac{250V}{3V}$  and fed to discrete moving average filter to obtain ripple free actual DC-bus voltage, as depicted in Figure 5-6.



Figure 5-6: Configuration schematic of DC signal conditioning in the target Simulink

#### 5.2.2.4 Description of synchronous reference frame transformation in WAIJUNG block-set

Synchronous frame power control can be implemented using a current controller in a dq frame (Figure 5-7) and active and reactive power feed-forward control in the simplest way possible. The reference voltage for the active power can be altered by controlling the DC voltage. A matrix is used to convert the command signals into the dq components of the reference current.





Figure 5. 7: Configuration schematic of DQ transformation for (a) three-phase inverter currents, and (b) three phase load currents in the target Simulink

Signal conditioning circuits is employed to add DC offset of 1.5V in sensed inverter and load currents to generate uni-polar signals for the ADC pins. In side code, 1.5 V DC-offset eliminated first, then multiplied by the gain value  $\frac{1.5 \times 2 \times 1.41}{3}$  to obtain actual inverter currents and load currents. Eventually, the abc three-phase stationary frame is transformed into synchronous reference frames dq0.The synchronous reference frames dq0 component of inverter currents as well as load currents are defined by a transformation matrix derived from the abc three-phase stationary frame using phase-angle of utility grid voltages ( $\theta_{v_{gr}}$ ) and computed as:

$$\begin{bmatrix} i_{dqo} \end{bmatrix} = \sqrt{\frac{2}{3}} \times \begin{bmatrix} \cos(\theta_{vg}) & \cos(\theta_{vg} - \frac{2\pi}{3}) & \cos(\theta_{vg} + \frac{2\pi}{3}) \\ -\sin(\theta_{vg}) & -\sin(\theta_{vg} - \frac{2\pi}{3}) & -\sin(\theta_{vg} + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{inv_a} \\ i_{inv_b} \\ i_{inv_c} \end{bmatrix}$$
(5.4)

The currents,  $i_{dqo}$ , are fed to discrete moving average filter to eliminate ripple from DC quantities. The ripple free d-axis and q-axis component of inverter currents and load currents are obtain from the sub system as shown in Figure 5-7(a) and 5-7(b).

#### 5.2.2.5 Grid Synchronization in WAIJUNG block-set

The phase-locked loop (PLL) is used in grid-tied systems to synchronize converter operation with the grid voltage. The bandwidth of an irregular grid should be decreased to enable appropriate disturbance rejection without compromising detection speed. PLLs must increase dynamic response and minimize settling time without compromising system stability or the ability to eliminate disturbances. Control approaches with SOGI-FLL (second-order generalized integrator-frequency locked loop) performed the best for a single-phase /three phase system. It tracks harmonics, voltage changes, and frequency fluctuations precisely. This means that the SOGI-PLL outperforms the other PLLs in terms of speed and accuracy in poor grid circumstances, and detailed analysis is presented in chapter 3. A dual SOGI-FLL (DSOGI-FLL) structure is employed to extract positive component of grid voltages  $(v_{\alpha}^{+} \text{ and } v_{\beta}^{+})$  during the abnormal grid (harmonics distortions, voltage imbalances, frequency changes, voltage imbalances, etc.), which is formed by two SOGI blocks connected in parallel depicted in Figure 5-8. as



Figure 5-8: Configuration schematic of modified SOGI-FLL and angle computation block in the target Simulink

The positive component of grid voltages  $(v_{\alpha}^{+} \text{ and } v_{\beta}^{+})$  are fed to the phase-angle extraction unit, which is formulated based on tan-arc angle extraction method, as depicted in Figure5-8. The Frequency Lock loop is formulated for the frequency extraction.



Figure 5-9: Configuration schematic of DQ transformation for the three phase voltage signal in the target Simulink

Figure 5-9 shows three-phase grid voltages and DSOGI-FLL phase angle. The effectiveness of DSOGI-FLL is tested by taking different situations like frequency change, phase change, unbalancing of three-phase voltages, harmonics distortion, and DC offset. The target Simulink model for test cases is modeled and shown in Figure 5-10. The internal three-phase grid voltages are designed using components from the Simulink library, as depicted in Figure 5-10. The amplitude, phase, and frequency internal three-phase grid voltages can be controlled, changed or varied using three potentiometer 3V at ADC pins or an internal conditional switch with two constant values controlled by an external push switch.



Figure 5-10: Test bench schematic diagram for Modified SOGI-FLL by designing programmable source in the target Simulink

The frequency and phase sift are applied simultaneously, so, the variation of frequency can be observed in digital oscilloscope. For the frequency shift of 10% (frequency change from 50Hz to 45Hz) and phase-shift of 45° in three phase grid voltages, the conditional switch gives 50Hz value and phase of  $0^{\circ}$  to the frequency input and phase-angle of internal three-phase grid voltages when the status of external switch is '0', while 45Hz value and phase of 45° to the frequency input and phase –angle of internal three-phase grid voltages when the status of external switch is '1', as depicted in Figure 5-11. The ARM cortex STM32F407VG has two Digital/ analog converter peripherals to observer signal, but, amplitude must be less than 3V. Figure 5-11(a) displays three-phase grid voltages along with the phase-angle extracted by DSOGI-FLL. The three-phase grid voltages, displayed in Figure 5-11(a), undergoes a frequency shift of 10% (frequency change from 50Hz to 45Hz) and phase-shift of 45° to observe the frequency change. The frequency and phase shift in the three-phase grid voltages are measured by taking difference of cursor positions before and after frequency and phase shift, shown in the Figure 5-11(b). The estimated frequency is settled down to the new frequency of 45 Hz within 35 mille-seconds, as shown in the Figure 5-11 (c) and (d). Figure 5.11

shows the three-phase grid voltages along with extracted phase-angle from DSOGI-





Figure 5-11:Experimental results obtained from test bench of SOGI-FLL and measured during 10% frequency and 45° phase shift in grid voltages: (a) threephase voltage signals and phase –angle of grid, (b)Zoom view of phase-a voltage signal of three phase and phase(c) dynamic performance of angular frequency, (b)Zoom view of dynamic performance of angular frequency

It is noted that extracted phase-angle from DSOGI-FLL is not affected much more when initially balanced grid voltage experiences the balanced sag of 50%, as shown in the Figure 5-12. Figure 5-12 (b) shows the positive sequence of grid voltages i.e. $v_{\alpha}^{+}$  and  $v_{\beta}^{+}$  and along with extracted phase-angel from DSOGI-FLL. During the voltage sag, frequency and extracted phase-angle is settled down within two cycles i.e. around 35 milli-second, as shown in the Figure 5-12. The DSOGI-FLL behaves as second-order band-pass filter, which provides immunity towards highly distorted three-phase grid voltages.



Figure 5. 12:Experimental results obtained from test bench of SOGI-FLL during 50% balanced sag in the grid voltages

The three-phase grid voltages experience the presence of 5<sup>th</sup>, 7<sup>th</sup>,11<sup>th</sup> order harmonics with amplitude proportional 20%, 15%, and 10% respectively, as shown in the Figure 5-13. It is noted that DSOGI-FLL is capable to eliminate the negative sequences and harmonics component from grid voltages. Figure 5-13 shows the highly distorted grid voltages, the positive sequence of grid voltages i.e.  $v_{\alpha}^{+}$  and  $v_{\beta}^{+}$ and along with extracted phase-angel from DSOGI-FLL. The DSOGI-FLL gives superior performance when grid voltages experience multiple abnormalities at the same time. It is also observed that extracted phase-angle is free from high frequency components due to the distorted grid voltages. In the event of a DC offset, the calculated frequency incorporates low frequency oscillations. A modified secondorder generalized integrator frequency-locked loop (MSOGI-FLL) is presented in this work to address grid voltage anomalies of all types, including dc offset. Figure 5-13(a) shows the positive sequence of grid voltages i.e.,  $v_{\alpha}^{+}$  and  $v_{\beta}^{+}$  and along with extracted phase-angel using DSOGI-FLL from distorted grid voltages with 10% DC offset. Figure 5-13(b) shows the result of single-phase grid connected system. As described in previous section, ADC pin accept only unipolar signal. So, AC signal is converted to unipolar signal by adding 1.5Volt DC offset while inside code same amount(1.5Volt) is subtracted from signal at ADC pins to obtain actual signal. The DC offset is added by improper elimination of DC scale. Instead of 1.5 Volt, 1.3 Volt is subtracted from signal which is at ADC pins to get actual signal. In this way, grid voltage is encounter by DC offset.


Figure 5-13:(a) Experimental results for grid synchronization during grid voltages effected by the harmonics, and (b) Experimental results of single-phase grid interfaced voltage source converter (Time scale:10ms//div) :  $i_g$  (Pink and blue; Scale 2A/div),  $v_g$  (Orange; Scale: 40V/div), and theta(green)

It is noted that modified DSOGI –FLL eliminates both harmonics distortion and negative sequences of three-phase grid voltage in order to detect accurately phaseangle of the grid voltage during abnormal grid voltage conditions including DC offset.

## 5.2.2.6 DC Current sensor less modified MPPT algorithm in WAIJUNG block-set

Figure 5-14 shows DC current sensor less modified MPPT algorithm for Single-stage grid tied PV system. The modified MPPT algorithm code is written in user define function of Simulink. The target Simulink file is modelled using multi-processing sampling rate. Here, modified MPPT algorithm (user define function of Simulink) is sampled at time interval which is 100 times of sampling time of target Simulink, as depicted in blue color. It is possible to estimate the reference value of d-axis current component by utilizing the DC-bus voltage regulator. It is necessary to compare the reference DC-bus voltage ( $V_{dc_{ref}}$ ) produced from the MPPT scheme with the actual DC-bus voltage ( $V_{dc}$ ) in order to determine the voltage error ( $\varepsilon_{dc}$ ), which is minimized by employing a PI regulator.

$$\varepsilon_{dc}[n] = (V_{dc_{ref}}[n] - V_{dc}[n-1])$$
(5.5)

$$I_{d_{ref}}[n] = I_{d_{ref}}[n-1] + K_{P_{dc}} \cdot (\varepsilon_{dc}[n] - \varepsilon_{dc}[n-1]) + K_{integral_{dc}} T_{s_{dc}} \cdot \varepsilon_{dc}[n]$$
(5.6)

Here,  $K_{P_{dc}}$  and  $K_{integral_{dc}}$  are the proportional and integral gains in voltage controller, respectively. In the outer DC-bus control loop,  $T_{s_{dc}}$  is a sampling time for outer voltage control loop. A Photovoltaic inverter provides reactive power up to the inverter's maximum VA capacity. A reference value of q-axis component for the PV inverter current,  $I_{q_{ref}}$ , which is chosen based on the operating mode of the inverter. The power factor at PCC is controlled by  $I_{q_{ref}}$ , which is derived by multiplying the negative unity gain to the q-axis component of the Load current,  $I_{q_{Load}}$  in Mode I.



Figure 5-14: Configuration View and m-file of modified MPPT algorithm

In Mode I (power factor control),  $I_{q_{ref}}$  is expressed as follows:

$$I_{q_{ref}}[n] = -1 \times I_{q_{Load}}[n]$$
(5.7)

Mode II  $I_{q_{ref}}$  is derivable from the PI regulator, which is employed to manage grid voltage at PCC and is hence derivable from the PI regulator. It can be deduced from Mode II (grid voltage control) as follows:

$$\varepsilon_{\text{PCC}}[n] = (V_{\text{peak}_{\text{ref}}}[n] - V_{d}[n-1])$$
(5.8)

 $I_{q_{ref}}[n]=I_{q_{ref}}[n-1]+K_{P_{PCC}}(\epsilon_{PCC}[n] - \epsilon_{PCC}[n-1])+K_{integral_{PCC}}T_{s_{PCC}}\epsilon_{PCC}[n])$  (5.9) Here,  $K_{P_{PCC}}$  and  $K_{integral_{PCC}}$  are the proportional and integral gains of the PCC voltage regulator. In the outer PCC voltage control loop,  $T_{s_{PCC}}$  represents the sampling time. It is possible to calculate the PCC voltage error ( $\epsilon_{PCC}$ ) by subtracting the measured peak value of PCC voltage  $V_d$  from a peak reference value of PCC voltage  $V_{peak_{ref}}$ .

#### 5.2.2.7 Synchronous Frame current control in WAIJUNG blockset

Equation (5.10) to (5.12), which contain the values of  $I_{d_{ref}}[n]$  and  $I_{q_{ref}}[n]$ , are used to control  $I_d[n]$  and  $I_q[n]$  with the use of two current regulators.

It is possible to realize these two current regulators using the following equations:

$$\epsilon_{i_d}[n] = (I_{d_{ref}}[n] - I_d[n-1]); \epsilon_{i_q}[n] = (I_{q_{ref}}[n] - I_q[n-1])$$
(5.10)

$$V_{d_{m}}^{*}[n] = V_{d_{m}}^{*}[n-1] + K_{p_{i_{d}}}(\varepsilon_{i_{d}}[n] - \varepsilon_{i_{d}}[n-1]) + K_{integral_{i_{d}}} T_{s} \varepsilon_{i_{d}}[n])$$
(5.11)

$$V_{q_m}^*[n] = V_{q_m}^*[n-1] + K_{p_{i_q}}(\varepsilon_{i_q}[n] - \varepsilon_{i_q}[n-1]) + K_{integral_{i_q}}T_s.\varepsilon_{i_q}[n])$$
(5.12)

Here, the term  $\varepsilon_{i\_d}$  refers to the error, which is calculated by subtracting  $I_d$  from  $I_{q_{ref}}$ . The reference where as  $\varepsilon_{i\_q}$  denotes the error, computed by subtracting  $I_d$  from  $I_{q_{ref}}$ . The reference PV inverter voltage signal for the d-axis and q-axis are represented by the symbol  $V_{d_m}^*[n]$  and  $V_{q_m}^*[n]$  respectively. The proportional and integral gains of the d-axis current regulator are denoted by the variables  $K_{p_{i\_d}}$  and  $K_{integral_{i\_d}}$ , respectively. The proportional and integral gains of the q-axis current regulator are denoted by the variables  $K_{p_{i\_q}}$  and  $K_{integral_{i\_d}}$ , respectively.

# Inner d-axis current control loop



Inner q-axis current control loop



Figure 5-15: Configuration View of synchronous frame inner current control loop

It is possible to derive the modulating PV inverter voltages in a synchronous frame by taking the internal decoupling into account. It is expressed as follows:

$$V_{d_{m}}^{*}[n] = V_{d}[n] - V_{d_{ref}}^{*}[n] + I_{q}[n] \times \omega[n] \times L$$
(5.13)

$$V_{q_{m}}^{*}[n] = V_{q}[n] - V_{q_{ref}}^{*}[n] - I_{d}[n] \times \omega[n] \times L$$
(5.14)

Equation (5.13) to (5.14), which contain the values of  $V_{d_m}^*[n]$  and  $V_q^*[n]$ , are realized in target Simulink model with sampling timeT<sub>s</sub>, which is indicated by green color. The inner current loop of multipurpose PV system (as depicted in Figure) is tested and validated experimentally. The steady state performance of current control loop in synchronous reference frame is carried out by taking three test cases such as : (i) only active current injection ( $i_{inverter(ref)_d} = -2$  A and  $i_{inverter(ref)_q} = 0$ ,Conventional PV system), (ii) active current injection and reactive power exchange ( $i_{inverter(ref)_d} = -2$ A and  $i_{inverter(ref)_q} = +1.5/-1.5$ , Partial PV-STATCOM system), and (ii) only reactive power support ( $i_{inverter(ref)_d} = 0$  and  $i_{inverter(ref)_q} = +1.5/-1.5$ , Partial

Full-STATCOM system). In the first test case, the real power is injected into the grid by PV inverter. During experiment in a day time, the reference value of DC-bus  $(V_{dc_{ref}})$  is set to 240V and PV current is observed 1.8 A. The reference value of daxis is generated as per the equation and given to d-axis inner current control loop. While the reference value of q-axis is set to be zero. The line to line voltage of PCC is adjusted at 110 V (rms value). It is noted from the figure 5-16 that active current of 2A is only injected into utility. The PCC voltage and inverter current are out of phase, as depicted in Figure 5-16. The reactive power support is not provided by PV inverter, as observed from the Figure 5-16.





#### A and $i_{inverter(ref)_a} = 0$ , Conventional PV system

During second test case, the active power injection and reactive power exchange by the of multi-purpose PV inverter is validated its effectiveness by utilizing a remaining capacity of PV inverter. The reactive power support provided by multipurpose PV inverter when inductive or capacitive load is connected at PCC to maintain unity power factor at the utility grid. The active power injection is managed by MPPT algorithm as per the availability of solar irradiance from dawn to duck. The reactive power support i.e. Partial-STATCOM is demonstrated by considering two cases: inductive mode and capacitive mode operation of PV inverter. Instead of capacitive load or Inductive Load, the reference value of d-q axis load current value is chosen a fix value i.e.  $i_{inverter(ref),d}$  and  $i_{inverter(ref),q}$  for an experimental validation. Therefore, PCC voltage (Phase a) and inverter current (Phase a) are observed as experimental result to conclude the nature of PV system. If the inverter currents are lagging to PCC voltages with the chosen fix d-q axis capacitive load

current value, then inductive nature of PV inverter whereas leading to PCC voltages with a chosen a fix d-q axis inductive load current value, then capacitive nature of PV inverter. According to the equation, if capacitive load is connected at PCC at that time PV inverter has to behave as inductive load for maintaining unity power factor at source side or utility grid side, and vice versa. The capacitive behavior of PV system along with active power injection is validated experimentally by taking  $i_{inverter(ref)_d} = -2 \text{ A} and i_{inverter(ref)_q} = +1.5$ , as depicted in Figure 5-17(a).



Figure 5-17: Experimental results of inner current control loop obtained in grid-tied PV system without outer voltage controller obtained by taking (a)  $i_{inverter(ref)_d} = -2$  A and  $i_{inverter(ref)_q} = +1.5$ , and (b)  $i_{inverter(ref)_d} = -2$  A and

 $i_{inverter(ref)_g} = -1.5$ , Partial PV-STATCOM

The inverter current (Phase A) is leading the PCC voltage (Phase A) to act as capacitive for the compensation of reactive power in inductive load, which fulfil the objective of unity power factor at grid side as STATCOM, as depicted in a Figure 5-17. The inverter current is leading the PCC voltage by observing wave form in the Figure 5-17with respect to the wave form of conventional PV system in figure 5.16. Furthermore, the inductive behavior of PV system along with active power injection is validated experimentally by taking  $i_{inverter(ref)_d} = -2$  A and  $i_{inverter(ref)_q} = -1.5$ , as depicted in Figure 5-17(b). The inverter current is lagging the PCC voltage by observing waveform in Figure 5-17 with respect to the wave form of conventional PV system in Figure 5-16. The inverter current (Phase A) is lagging the PCC voltage (Phase A) to act as inductive for the compensation of reactive power in capacitive load, which fulfil the objective of unity power factor at grid side as STATCOM.



Figure 5-18: Experimental results of inner current control loop obtained in grid-tied PV system without outer voltage controller obtained by  $i_{inverter(ref)_d} = 0$ A (a)  $i_{inverter(ref)_d} = +1.5$ , and (b)  $i_{inverter(ref)_d} = -1.5$ , Full -STATCOM

The objective of third test case is to provide only reactive power support to the grid. It operates to fulfil prioritize two objectives: 1) voltage control and Power factor correction. If the PCC voltage within acceptable limits, then PV inverter is providing only unity power factor at grid. As per load convention for grid connection, if PV system(here, it is considered as load) is injecting power in grid at that time grid current and PCC voltage out of phase at no-load or resistive load condition while grid current and PCC voltage are in phase when PFC mode(as rectifier) is enabled, when PV panels is disconnected from PV inverter. The PCC voltage is reduced when inductive load connected while increased when capacitive load is connected at PCC. The objective of PCC voltage controller block is to create the reactive current reference according to reference value of PCC voltage. If PCC voltage increases due to capacitive load, multipurpose inverter is acting as an inductor, as shown in Figure in the Figure 5-18(a) , while decreasing at that moment behave as capacitor, as shown in the Figure 5-18(b), to regulate PCC voltage.

## 5.2.2.8 PWM generation, Display unit, and Protection unit in WAIJUNG block-set

The voltages  $(V_{d_m}^*[n], V_{q_m}^*[n])$  are converted to stationary reference voltages  $(v_{a_m}^*, v_{b_m}^*, v_{c_m}^*)$  using the following formula:

$$\begin{bmatrix} v_{a_{m}}^{*}[n] \\ v_{b_{m}}^{*}[n] \\ v_{c_{m}}^{*}[n] \end{bmatrix} = \frac{1}{v_{d[n]}} \begin{bmatrix} \sin(\theta_{PLL}[n]) & \cos(\theta_{PLL}[n]) \\ \sin(\theta_{PLL}[n] - \frac{\pi}{3}) & \cos(\theta_{PLL}[n] - \frac{\pi}{3}) \\ \sin(\theta_{PLL}[n] - \frac{2\pi}{3}) & \cos(\theta_{PLL}[n] - \frac{2\pi}{3}) \end{bmatrix} \begin{bmatrix} V_{d_{m}}^{*}[n] \\ V_{d_{m}}^{*}[n] \end{bmatrix}$$
(5.15)

Advance PWM Timer 8 of STM32F407VG microcontroller is used to compare the modulating PV inverter voltages ( $v_{a_m}^*[n]$ ,  $v_{b_m}^*[n]$ , and  $v_{c_m}^*[n]$ ) to a high frequency carrier wave. The Advance Timer 8 of microcontroller can generate gating pulses using bi-polar sinusoidal pulse width modulation.



Figure 5-19: Configuration view of PWM generation block in target Simulink file

The modulating signals of PV inverter voltages  $(v_{a_m}^*[n], v_{b_m}^*[n], and v_{c_m}^*[n])$  are amplified by gain value 50, and the further added DC offset of value 50, aforementioned modulation technique. Consequently, the signal can vary between 0 to 100 values, which is the duty cycle requirement of Advance PWM Timer in microcontroller, as depicted in Figure 5-19. Active and reactive power control can achieved through the use of the sine pulse width modulation pulses generated by the PV inverters.



Figure 5-20: Configuration view of Display unit and DSO unit in target Simulink file



#### Figure 5-21: Configuration View and m-file Protection algorithm of system

The advance Timer 8 can generates six complimentary PWM gating pulses with programmable dead time insertion (1 micro-second) for the converter through controller pins (C6/A7, C7/B0, and C8/B1), which provides short circuit protection in power card. A Display unit is very crucial during PI controller tuning in outer voltage control loop as well as inner current control loop. The LCD (16\*2) setup block is configured in target Simulink file, which have information about microcontroller pins interfaced with command line(RS, read, and write pin) and date

pins(8 bit mode or 4-bit mode). There are two CLCD write block (for line 1 and line 2 in LCD (16\*2)) configured in target Simulink , which is used to control character print position for line 1 and line 2.Buffer block is configured to display the quantities which want to be observed during functioning of experimental set-up. A protection block is created to protect the voltage source converter. During operation of grid tied PV system, if DC-bus voltage is out of voltage range ( $V_{dc} \leq 300V$ ), then this block stop the gating pulses from the advance PWM Timer, as depicted in Figure 5-21.

# 5.3 Experimental setup of the Multipurpose Single-stage grid tied PV system

This chapter describes the laboratory setup and justification of the sensible PV system performance for all three operational modes as a multipurpose PV system. For designing low rating prototype, a 10KVA 3 phase variac (Star/Star configuration) as interface transformer is employed as interconnection of the photovoltaic system, grid, and load at power common coupling. An experimental setup consists of a three phase IGBT power converter card, IGBT driver card with short-circuit protection, STM32F407VG 32-bit DSP based microcontroller, current and voltage Hall sensor for DC side, 3 set of current transformer (CT) and power transformer (PT) for ac side along with the features of DC offset adjustment for unipolar ADC in a microcontroller, line inductor, 8 series connected PV panel strings, and 3-phase varic as power interface between PV system and utility grid. The inverter currents and PCC voltage are sensed and scaled into proportionally within 3V by 3-set of current transformer (CT) and power transformer (PT)and scaling circuits, respectively. It is to be taken care that microcontroller has uni-polar ADC pins with the limitation of maximum voltage 3.3V at ADC pins. Hence DC offset circuits are required to converter bi-polar signal into unipolar signal. The role of sensors circuit is sensed as well as scaled into 3V (for the safety) and DC offset circuits add 1.5V DC into scaled ac signals to make unipolar signal, which is given to the ADC pins of microcontroller The hall sensors are used to measure current and voltage of PV strings and scaled into 3V to be used in MPPT algorithm to generate active current reference for the control approach of presented PV system. The

discrete model of control system of presented PV system is designed using WAIJUNG block set for STM32F4 series controller in Simulink/MATLAB environment. Simulation models can be easily and automatically converted to C code using the WAIJUNG block-set in Simulink, which can be used to create code for a STM32F family microcontroller models (Targets). The WAIJUNG block-set was created to work with ST Microelectronics high-performance and DSP-capable STM32F4 microcontrollers (STM32F4 Target).

#### **5.4 Experimental Results and Discussion**

In this section, the results of experimental study are demonstrated for Partial and Full STATCOM operating modes of multipurpose single-stage PV inverter. The control objectives are power factor correction, voltage control and reactive power control for partial STATCOM mode whereas the objective is voltage control for full STATCOM mode. In Figure 5-22, the experiment setup is depicted as a line diagram. The autotransformer adjusts the 415 V, 50 Hz three-phase line to line voltages to 110 V. Line inductance of 5 mH is coupled to this 150 V grid supply to realize the transmission line. Additionally, the single-stage PV inverter and the load bank are all connected to the PCC via a line inductance terminal. An IGBT inverter with three phases and two levels and a 1920 W SPV source make up the PV inverter. An Agilent 4-channel digital signal oscilloscope is used to record the outcomes of the tests. The DC-bus voltage, grid voltage, load current, and SPV current are all sensed using hall effect-based sensor cards. The three-phase current transformer sensor cards are used to monitor the currents in the PV inverter Experiment setup photos are presented in Figure 5-23.



system



Figure 5-23: Experimental set-up of Single Stage grid tied PV system

Parameter Value					
<b>Photovoltaic</b>	Solar power	240W			
Panels	PanelsVolatge at MPP, $V_{PV_{max}}$ , Current at MPP, $I_{PV_{max}}$				
$(1000 \frac{\text{W}}{\text{W}}, \text{AM})$	Open circuit	36V			
1.5 Spectrum,	Short circuit	8.9A			
cell	cell No. of PV panels connected in series and Parallel				
$25^{\circ}C$ )	Maximum Power from				
			240*8=1920W		
DC-link	DC-linl	250V			
	DC-Link capaci	4700 $\mu$ farad			
IGBT	Power capacity		12000W		
<u>Power</u> Ratings	Switching freq	5000Hz			
Line Filter	Line in	5 mH			
Dinala Filton	Resistor		5 ohm		
<u>Kipple Filter</u>	Capacitor		10 $\mu$ farad		
	Line to line voltage at PCC, and frequency		110V, 50Hz		
Utility Crid	Auto transformer (line to line voltage, and				
<u>Otinty Gria</u>	current)		415V/110V,		
		15 A			
Load at	Three- phase variable	0-10A			
<u>PCC</u>	(delta connected)				
	MPPT Control	Sampling Time	0.4 seconds		
	Parameter	Step size∆	0.5 Volt		
	Modified SOGI-FLL Parameter	$Gain(A_{Gain_{DC-Blocker}})$	0.998		
<u>Control</u>		$k_{SOGI}$ , $\Gamma_{FLL}$	0.5 , -1000		
<u>Parameter</u>		Sampling Time	400 μsecond		
	Outer DC-Link	$K_{p_{DC}}, K_{integral_{DC}}$	0.5, 3		
	voltage Controller	Sampling Time	4000 μsecond		
	Outer PCC voltage	$K_{p_{PCC}}, K_{integral_{PCC}}$	0.5, 3		

 Controller	Sampling Time	4000 μsecond
Inner d-axis current	K <sub>pd</sub> , K <sub>integrald</sub>	5, 10
Controller	Sampling Time	400 μsecond
Inner q-axis current	$K_{p_q}, K_{integral_q}$	5, 10
Controller	Sampling Time	400 μsecond

# 5.4.1 Performance of the multipurpose single-stage grid tied PV system

To monitor the influence of the control system actions on the PCC voltages and source currents, a phase-A of PCC voltage( $v_{PCC_a}$ ), source current ( $i_{source_a}$ ), PV inverter current (i<sub>invertera</sub>), and load current(i<sub>Loada</sub>), are monitored in the experimental setup. To achieve a desired operation of the presented control system, additional signals such as the DC-bus voltage, PCC voltages, inverter currents, and load currents are sensed. These signals are sent into the ADC pins of a generic ARM CortexM4 microcontroller (STM32F407VG), on which the control system( discussed in chapter 4) is implemented. A sampling time of the MPPT technique is set at 0.4 seconds in the controller. Therefore, the  $V_{dc_{ref}}$  is generated for outer voltage control loop every 0.4 second by MPPT block of target Simulink code. The outer voltage control for DC-bus voltage and PCC voltage control are carried out in 4000µs, whereas the inner current control loops through synchronous reference frame are carried out in 400 µs. The grid synchronization block is operated at 400 µs. The outer control loops for DC-bus voltage and PCC voltage control are carried out in 4000  $\mu$ s, whereas 5KHz is the frequency at which the inverter switches work. The initial PI controller values are computed by considering second ordered control system with damping factor, 0.707. The "Simulink Design Optimization" package of MATLAB is used to further enhance the performance of PI controller using the gradient descent technique [24,25]. The active Solar PV source, which consists of eight 250 W solar panels connected in series, has been thoroughly investigated. Using the modified DSOGI-FLL scheme, the effective grid voltage angle estimate ( $\theta_{v_{PLL}}$ ) is tested, as a

first test of grid- tied multipurpose PV system, and dynamic results are presented in the section 5.2.1.5. A control system of PV inverter is responsible for supplying both active and reactive power to PCC. In addition to active solar power transfer, the PV inverter exchanges the reactive power required by the load, ensuring that the unity power factor operation is maintained at the PCC. According to KCL, the utility grid acts as a source of power for the purpose of determining current direction, whereas the load and the inverter, in the absence of a PV system or a DC source, act as a load by accepting current from the utility grid. The load current is 90° behind the PCC voltage when there is just an inductive load connected to the PCC. The load current is 90° ahead of the PCC voltage (leading) when there is only a capacitive load. Instead of an inductive or a capacitive load attached to PCC, if the voltage source converter is connected to the PCC as a rectifier, the PCC voltages and converter currents (or source currents) are in phase with one another. It has been determined that the utility grid is supplying power to the converter in order to serve as a load convention for current measurement.

#### 5.4.1.1 Test-1 Steady state performance of multipurpose singlestage PV system using MPPT

The maximum power of solar panel is tracked using a modified DC current sensorless MPPT technique that is sampled every 0.4 s. The DC-bus voltage is dynamically adjusted to extract maximum power from solar panel, which can be achieved by providing reference DC voltage from MPPT algorithm to outer voltage control loop for active power control. The steady-state and dynamic performance of the power tracking algorithm is evaluated during cloudy day. The performance of modified DC current sensor-less MPPT technique is evaluated by observing v<sub>PCCa</sub>,i<sub>sourcea</sub>, solar power P<sub>pv</sub>, and the d-axis component of inverter currents (i<sub>inverterd</sub>). During cloudy day, four experimental results were recorded and demonstrated in Figure 5-24.At 430  $\frac{W}{m^2}$  of solar radiation, the steady-state power tracking performance is shown in Figure 5-24(a).



Figure 5-24: Dynamic performance of single stage grid tied PV system during variable solar irradiance (Time scale:60ms//div) :  $v_{PCC}$  (Red; Scale 75V/div),  $i_{source}$  (Pink; Scale: 4A/div),  $P_{PV}$  (Blue; Scale: 500W/div), and  $i_d$  (green Scale: 4A/div)



Figure 5-25: Dynamic performance of single stage grid tied PV system during variable solar irradiance (Time scale:60ms//div) :  $v_{PCC}$  (Red; Scale 75V/div),  $i_{source}$  (Pink; Scale: 4A/div),  $P_{PV}$  (Blue; Scale: 500W/div), and  $i_d$  (green Scale: 4A/div

To demonstrate the steady-state tracking performance at 430  $\frac{W}{m^2}$  of solar radiation, Figure 5-24(a) provides to get the comparable Solar PV output of 650 watts (W). Both the DC-bus voltage and the d-axis component of inverter currents (i<sub>inverterd</sub>) are recorded at 232 V and 2.8 A in the system. However, with lower sun radiation  $(250 \frac{W}{m^2})$ , steady-state power tracking performance is shown in Figure 5-24(b) with a little lower value of DC-bus voltage (205 V), the d-axis component of inverter currents (1.6 A), and generated SPV power (328 W) than at the previous higher sun radiation condition. Figure 5-25(a) shows the SPV power tracking performance as the ambient conditions vary with a slighter higher value of DC-bus voltage (211 V), the d-axis component of inverter currents (1.8 A), and generated SPV power (379W). At lower solar radiation  $(290\frac{W}{m^2})$ , steady-state power tracking performance is shown in Figure 5-25(b), where the DC-bus voltage (201V), d-axis component of inverter currents (1.3A), and generated solar power are adjusted at somewhat lower values than in the preceding greater sun radiation condition, respectively. It is demonstrated in Figure 5-25. a that the DC-bus voltage is adjusted at the value for extracting maximum power from solar panels through outer voltage control loop of active power control and modified MPPT algorithms, which is injected into the grid. Peak power tracking can be achieved by varying the DC-bus voltage in response to changes in the surrounding environment.



Figure 5-26: (a)Dynamic Performance of DC-bus reference voltage and DC-bus voltage and d-axis current synchronous reference frame. (Time scale:2ms//div) :  $V_{DC}$  (purple)and  $V_{DC_{ref}}$ (orange) : Scale: 110V/div, and  $i_d$  (cyan)Scale: 1A/div, and (b) the PV curve characteristics

The source current increases with an increase in Solar PV generation(as increase in solar irradiance), while decreases with decrease in in solar irradiance , as depicted in Figure 5-24 and Figure5-25. The dynamic performance of DC-link outer loop voltage controller is validated by changing DC-bus reference voltage from fix 230 Volt to fix 265V through switching function. The voltage at MPP ( $V_{MPP_{solar Panels}}$ ) for panels is 240Volt. The the d-axis component of inverter currents ( $i_{inverter_d}$ ) is decreased from 2.8A to 0.7 A when the DC-bus reference voltage increased from the fix 230 Volt to fix 265V. It is observed from the Figure5-26 that DC-bus voltage is fine-tuned with DC-bus reference voltage. Furthermore, d-axis current is decreased when DC-bus reference voltage is higher than the voltage at maximum power point. A modified DC current sensor-less MPPT is designed as per the observation from Figure5-26(b). If  $\Delta I_d > 0$ , then  $\frac{\Delta I_d}{\Delta V_{dc}} > 0$ , and the MPPT reference voltage is increased to bring the operating point towards the maximum power point.

 Table-5-2 Possible Variations in Modified DC current Sensor-less

MPPT

Cases	$\Delta i_{d_{inverter}}$	$\Delta V_{DC-link}$	$\Delta i_{d_{inverter}}$	Action	Response
			$\Delta V_{DC-link}$	Required	
Case-I	+ve	+ve	+ve	$\uparrow V_{dc_{ref}}$	$\uparrow P_{PV},\uparrow V_{DC}$
Case-II	+ve	-ve	-ve	$\downarrow V_{dc_{ref}}$	↑ $P_{PV}$ ,↓ $V_{DC}$
Case-III	-ve	+ve	-ve	$\downarrow V_{dc_{ref}}$	↑ $P_{PV}$ ,↓ $V_{DC}$
Case-IV	-ve	-ve	+ve	↑ V <sub>dc<sub>ref</sub></sub>	$\uparrow$ P <sub>PV</sub> , $\uparrow$ V <sub>DC</sub>

The reference voltage  $V_{dc_{ref}}(k)$  for outer voltage control loop is computed by modified MPPT algorithm as per the equation.

$$V_{dc_{ref}}(k) + \Delta V_{step-size} \qquad (\Delta I_d > 0 \& \Delta V_{dc} > 0) ||$$

$$(\Delta I_d < 0 \& \Delta V_{dc} < 0)$$

$$V_{dc_{ref}}(k) = \qquad (5.15)$$

$$V_{dc_{ref}}(k) - \Delta V_{step-size} \qquad (\Delta I_d < 0 \& \Delta V_{dc} > 0) ||$$

$$(\Delta I_d > 0 \& \Delta V_{dc} < 0)$$

While  $\Delta I_d < 0$ , then  $\frac{\Delta I_d}{\Delta V_{dc}} < 0$ , and the MPPT reference voltage must be decreased in order to bring the operating point towards the maximum power point.

#### 5.4.1.2 Test-2 Performance of system as Partial PV- STATCOM

The sensed PCC voltage(Phase-A) and load currents are shown in Figure 5-27(a). .The variable three phase inductive load is set at 1 ampere (RMS value is recorded from multi meter). It is noted from Figure 5-27 (b) that the PV inverter is only injecting active power to the grid, and no reactive power support is provided by the inverter during this operation. Figure 5-27(b) illustrate the performance indices of v<sub>PCCa</sub>, i<sub>sourcea</sub>, i<sub>invertera</sub>, andi<sub>loada</sub>. It is noted that the multipurpose PV system is operated active power injection mode (as conventional PV system) and only inject active power (W)into utility grid at maximum power point using MPPT algorithm on inverter, and further more inverter currents and PCC voltages are 180° out of phase as depicted in Figure 5-27(b). The PV inverter injects additional power into the utility grid. The active power requirement of inductive load is provided by the photovoltaic inverter and surplus power injected into the grid, while the grid provides the reactive power that is required by the inductive load, as seen in Figure 5-27(b). Figure 5-27 (b) illustrates the steady state performances at 240  $\frac{W}{m^2}$  solar radiations. In Figure 5-27 (b), solar power of 185 W is generated at  $240\frac{W}{m^2}$ . The PV inverter has generated 1.8 ampere current in which 1 ampere current is delivered to the variable three phase inductive load and extra 0.8 ampere current is injected to the grid, as depicted in Figure 5- 27(c). The DC-bus voltage is adjusted to 230 V which MPP voltage corresponding to is given sun radiation of  $240\frac{W}{m^2}$ . As a result, the power factor is noted to be non-uniform, as seen from the Figure 5-27(a). In Figure 5-27(b), the power factor correction mode is activated which means multi-purpose PV inverter is providing reactive power support in addition of active power injection. Figure 5-27 (b) illustrate that PCC voltages and source currents are not maintained at unity power factor where as PCC voltages and source currents are out of phase. The PV inverter current is leading to PCC voltage, whereas load current is lagging to PCC voltage, as depicted in Figure 5-27. It is concluded that multi-purpose PV inverter behave as capacitive load for providing reactive power support to the grid when inductive load is connected at the PCC.



Figure 5-27:(a) Waveform of sensed Phase-A PCC voltage and sensed three phase inductive load currents, (b)Experimental Results of PV inverter without reactive power support at grid side, and (c) Experimental Results of PV inverter with reactive power support at grid side(Time scale:10ms//div) :  $v_{PCC}$  (Red; Scale 75V/div),  $i_{source}$  (Pink; Scale: 0.4A/div),  $i_{inverter}$  (Blue; Scale: 1.6A/div), and  $i_{load}$  (green Scale: 0.5A/div)

The  $v_{PCC_a}$  and  $i_{source_a}$  are observed to be in out of phase, and the PV inverter current  $(i_{inverter_a})$  is noted to be ahead of the power supply voltage,  $v_{PCC_a}$ . PV inverters transfer active solar PV power and exchange reactive power required by a three phase variable inductive load as depicted in Figure 5-28(a). As a result of the PV inverter is supplying the three phase variable inductive power demand (active and reactive), the  $v_{PCC_a}$  and  $i_{source_a}$  are noted to be in- phase, as depicted in Figure 5-28(b).





#### 5.4.1.3 Test-3 Performance of PV system as Full-STATCOM

The power factor is preserved steady at power factor. It demonstrates that the photovoltaic inverter meets load requirements when necessary and sufficient solar power is not available or during night time. Figure 5-29 illustrates the steady state performances during night time. The variable three phase inductive load is set at 1 ampere (RMS value is recorded from multi meter). The dynamic performance of the PV inverter is shown in Figure 5-29, when it is attached without and with three phase inductive load and maintained unity power factor at grid (Full-STATCOM Test of multipurpose PV system). The variable three phase inductive load is set at 1 ampere (RMS value is recorded from multi meter). Figure 5-28 and Figure 5-29 illustrates the performance of PV system in the unity power factor mode when the load current varies during day time or night time. Full-STATCOM Test of multipurpose PV

system is carried without PV panels for the night time. The reactive power requirement of the load fluctuates dynamically as the load current varies. It is noted that power factor is kept at unity by supporting reactive power from the shunt connected photovoltaic inverter in accordance with load requirements. FFT analysis is carried out in the digital oscilloscope and noted that current harmonics are less than 5%, which complies with IEEE 519 grid code



Figure 5- 29: Dynamic results of PCC voltage of Phase-A, Source current of Phase-A, inverter current Phase-A, and load current of Phase-A (Time scale:10ms//div) : PCC voltage of Phase-A(Red: Scale 50V/div), Source current of Phase-A((Pink), load current of Phase-A(Blue), and load current of Phase-A, (green), from no load to inductive load of 1 A

The steady-state performance of the PV inverter is shown in Figure, which is zoom view of Figure 5-30 when three phase inductive load is attached at PCC and maintained unity power factor at grid. Figure 5-29 and 5-30 illustrate the performance indices of  $v_{PCC_a}$ ,  $i_{source_a}$ ,  $i_{inverter_a}$ , and  $i_{load_a}$ . The variable three phase inductive load is set at 1 ampere (RMS value is recorded from multi meter). It is noted that multi-purpose PV inverter behave as capacitive load for providing reactive power support to the grid when three-phase inductive load is connected at the PCC. The  $v_{PCC_a}$  and  $i_{source_a}$  are observed to be in-phase, and the PV inverter current ( $i_{inverter_a}$ ) in Full- STATCOM unity power factor mode is noted to be ahead of the



Figure 5-30:Zoom view of Figure 5-29 and experimental results of PCC voltage of Phase-A, Source current of Phase-A, inverter current Phase-A, and load current of Phase-A.

A multipurpose PV inverters exchanges only reactive power which is required by a three phase variable inductive load as depicted in Figure 5-30. A shunt-connected PV inverter is used to support reactive power during this test, which verifies the system's grid voltage management capability. Figure5-31 demonstrates the results of the system with and without grid voltage regulation. Figure 5-31 illustrates how the system performs when the heavy variable restive load connected parallel to the inductive load is adjusted. The supply current ( $i_{source_a}$ ), the reactive power component of the PV inverter current ( $i_{inverter_a}$ ), and the RMS value of line voltage ( $v_g$ ), are observed during the experiment. According to Figure 5-31, without grid voltage management, ( $v_g$ ), fluctuates widely between 102 and 120 V. The reactive power from the PV inverter is supported in Figure 5-31, which reduces the voltage fluctuations. At 110V<sub>rms</sub>, the line voltage is kept stable. During a decrease in grid voltage, the leading reactive power is delivered, and vice versa.



Figure 5-31: Experimental results during PCC voltage control( Source current phase-A, q-axis inverter current , and line to line grid voltage): (a) without PCC voltage control, and(b) with voltage control



Figure 5-32: Experimental results during PCC voltage control( inverter current phase-A, solar power , and line to line grid voltage): (a) without PCC voltage control, and(b) with voltage control

Figure 5-32 (a) and (b) demonstrate the performance of multipurpose PV inverter with different levels of solar power generation as per solar irradiance. During the experiment, an inverter current ( $i_{inverter_a}$ ), solar power ( $P_{PV}$ ), and line voltage rms value ( $V_g$ ) are all measured and depicted in Figure5-32. As can be seen in Figure 5-32, the PV inverter is solely supplying active power to PCC, the grid voltage fluctuates between 102 and 120 V as a result of the dynamic change in SPV power. The performance of the system is illustrated in Figure 5-32(b) when the photovoltaic inverter injects active power and also accommodates reactive power to regulate the grid voltage. The system performs better when the PV inverter also trades reactive power to maintain the grid voltage. Variations in grid voltage are reduced, and the grid voltage is kept constant at 110 volts, as has been seen in Figure 5-32.

#### **5.5** Conclusion

This chapter is validating the multipurpose use of conventional-PV system by modifying control approach to manage the active and reactive power at the utility grid and load side with unity power factor at grid, maintaining PCC voltage is within acceptable range. It has been demonstrated from the experimental results that proposed multipurpose PV system is to inject active power according to solar irradiance and exchange reactive power at PCC to manage either PCC voltage or unity power factor at grid side during day time if and only if PCC voltage within acceptable range. Moreover, it is also proven that it autonomously operated as Full-STATCOM during night time, consequently, grid current remains in unity power factor with PCC voltage when reactive Load is connected to PCC.

#### CHAPTER 6 CONCLUSION & FUTURE SCOPE

Renewable energy technologies such as photovoltaic (PV) are becoming more commonly accepted as a means of sustaining and enhancing living standards while minimizing environmental damage.

#### 6.1 Conclusion

This thesis has validated the multipurpose use of conventional PV systems by modifying the control approach to manage the active and reactive power at the utility grid and load side with unity power factor at grid during PCC voltage within an acceptable range. However, the Conventional-PV is only injected with active power, has no reactive power support to the utility grid, and is also useless at night. During a day time, the objective of the presented multipurpose PV system is to inject active power according to solar irradiance and exchange reactive power at PCC to manage either PCC voltage or unity power factor at grid side if and only if PCC voltage is within an acceptable range. The mode of operation of a multipurpose PV system is validated through simulation results and experimental results. The grid synchronization needed for the control approach of a multipurpose PV system is deployed by combining the MDSOGI-FLL and tan-arc angle method to detect the frequency of the grid and phase angle under non-ideal grid conditions. Simulation results and experimental results also validate the synchronization approach. The control approach is implemented on a single-stage PV system to eliminate the DC-DC converter efficiency improvement with a cost-effective solution. The simulation results and experimental results confirm that multipurpose single-stage PV stem can provide fast, reactive power supports when needed, either voltage regulation support or power factor correction, and also validated the effectiveness and performance evaluation of control approach in different operative modes during the day as well as night. The switching between different modes of operation approves that the control approach of a multipurpose single-stage grid-tied PV system has adaptability scalability and can accommodate a wide range of atmospheric conditions and dynamic PV system operation.

Based on the research objective and the summary of the work provided in the thesis regarding the proposed control techniques, the following conclusions are made:

- [1] The modified dual-SOGI-FLL and tan-arc method are validated to extract the phase angle of PCC voltage for the control system during non-ideal grid conditions.
- [2] The multi-purpose PV inverter can manage smartly active power injection and fulfill the need for reactive power at PCC and grid without an oversizing inverter. Besides, it also provides reactive power exchange to either regulate PCC voltage or unity power factor at grid side if PCC voltage is within an acceptable range. It can handle a reactive power current through quadrature– axis (q-axis) current control during load variation 1-2 cycles.
- [3] The multi-purpose PV inverter can inject active power into the grid, controlled through a linearized DC bus voltage controller with a modified DC current sensor less MPPT algorithm.

#### 6.2 Future scope

The multipurpose single-stage PV system presented in the thesis still has scope to work. The future scopes are listed below:

- [1] The grid-tied PV system typically operates in a current-controlled mode to supply a predetermined amount of electricity to the primary grid. As scope of work, the multipurpose single-stage PV system must identify an islanding condition and as action control shift from current-controlled mode to voltagecontrolled mode and disconnect from the utility grid. It will maintain a constant voltage for the local load, including non-linear load during this mode.
- [2] PR controller and model predictive controller maybe apply for the seamless transition from the grid-tied PV system to standalone PV system or islanding PV system to accommodate the local load.
- [3] From the implementation point of view, parallel processors may reduce the computation burden on a single processor. It will increase the speed as well as the performance of the system.

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