CHAPTER 7

EXPERIMENTAL EVALUATION

7

EXPERIMENTAL EVALUATION

7.1 INTRODUCTION

In chapter 6 we have introduced, simulated and implemented m-DPA and DSA scheduling algorithms, out of which DSA supports QoS. This chapter compares various switching fabrics with iSLIP, m-DPA, and DSA scheduling algorithms for 4x4 and 8x8 switching fabric and experimental results are tabulated.

7.2 COMPARISION OF SWITCHING FABRICS

We have simulated and compared various switching fabric like Batcher-Banyan with Trap, Knockout (with concentrator output l=4), Knockout (with concentrator output l=2), and crossbar switching fabric with iSLIP, m-DPA, and DSA scheduling algorithms for 4x4 and 8x8 switching fabric. We have applied different traffic models (A,B,C and D) using MATLAB 7.0 as we have done in chapter 5. All the switching fabric are simulated for 1000 time slots and results are taken by averaging the outcomes for 100 simulations and various parameters like throughput (efficiency), average latency and delay variance have been measured for variation in offered load.

7.2.1 4x4 SWITCHING FABRIC

A. With i.i.d. Bernoulli arrivals and uniformly distributed destinations:

Simulation results from 7.1 to 7.3 show that for this traffic model, throughput of DSA is second best and only 3% less compare to knockout(l=4). Average latency for DSA are at par with knockout(l=4),but delay variance is 2 to 6 time slots high.

B. *With i.i.d. Bernoulli arrivals and non-uniformly distributed destinations:*

Simulations are done for normally distributed destinations. Results are plotted from figure 7.4 to 7.6 Results show that for this traffic model, throughput (efficiency) of DSA is at par with knockout(l=4), average latency is 2-3 time slot lower than knockout(l=4) but delay variance increases by 5 to 100 timeslots in DSA compared to knockout(l=4) due to prioritized QoS support.

C. With bursty arrivals and uniformly distributed destinations:

We illustrate the effect of burstiness on all the switching fabric using an on-off arrival process. Simulation results from figure 7.7 to 7.9 are shown below. They show that throughput (efficiency) and

average latency of DSA are at par with knockout (l=4), but delay variance is 2-3 time slot higher than knockout (l=4).

D. *With bursty arrivals and non-uniformly distributed destinations*:

We illustrate the effect of burstiness as well as non-uniform distribution for output on DSA in this traffic model. Simulation results from figure 7.10 to 7.12 are shown below. They show that throughput (efficiency) and average latency of DSA are at par with knockout (l=4), but delay variance is 3 time slots higher than knockout (l=4).

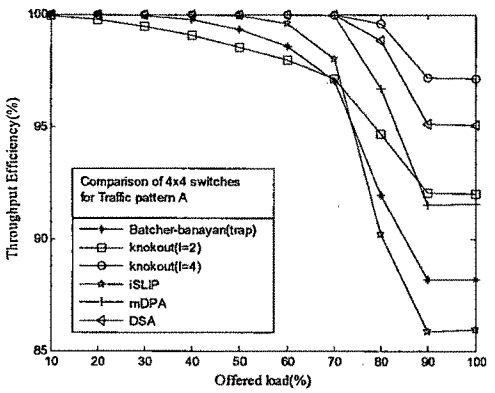


Figure 7.1 Throughput (efficiency) A (%)

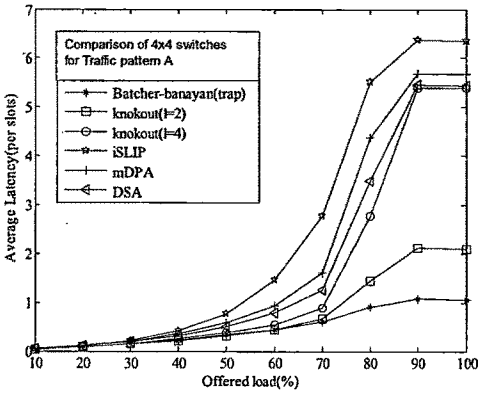


Figure 7.2 Average latency A (timeslots)

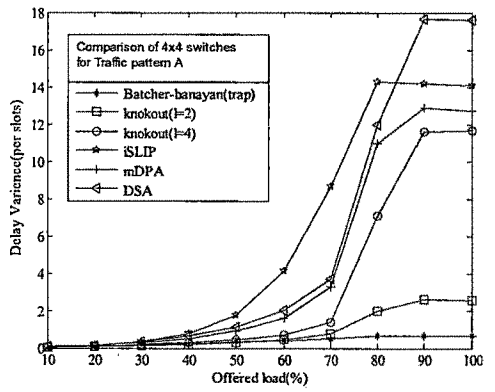


Figure 7.3 Delay variance A (timeslots)

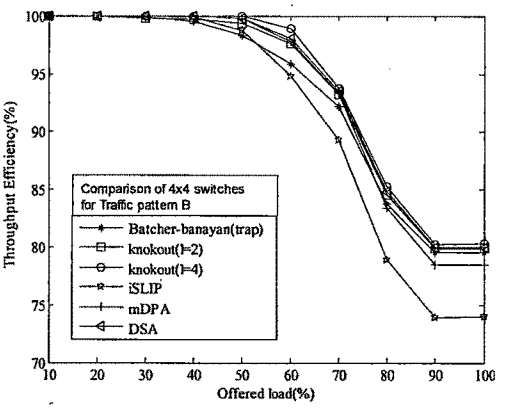


Figure 7.4 Throughput (efficiency) B (%)

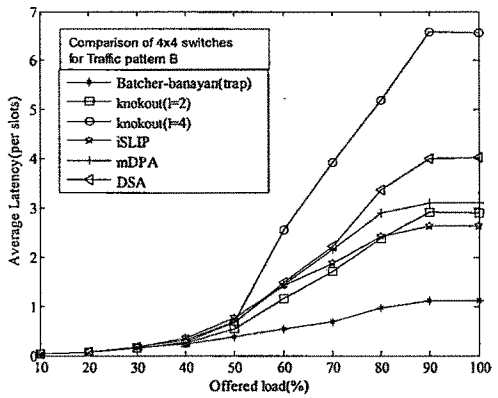


Figure 7.5 4x4 Average latency B (timeslots)

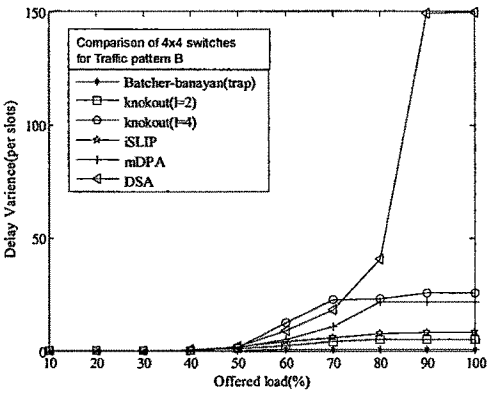


Figure 7.6 Delay variance B (timeslots)

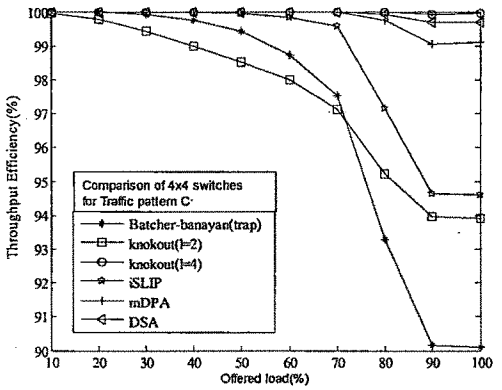


Figure 7.7 Throughput (efficiency) C (%)

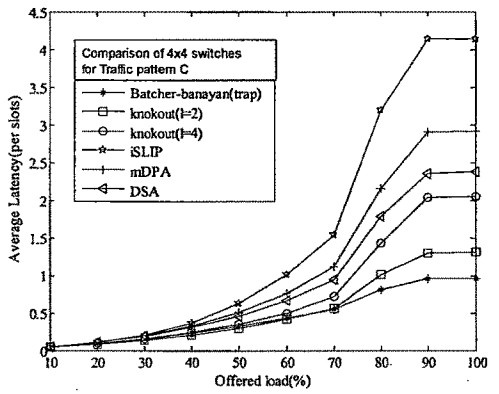


Figure 7.8 Average latency C (timeslots)

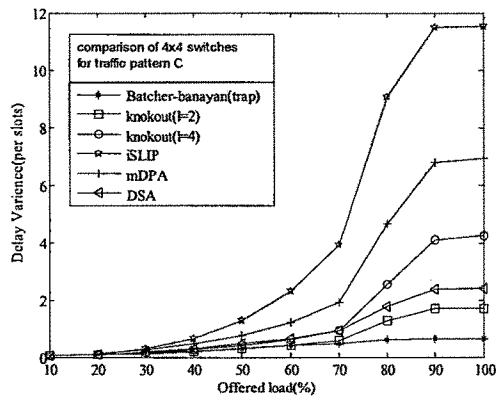


Figure 7.9 Delay variance C (timeslots)

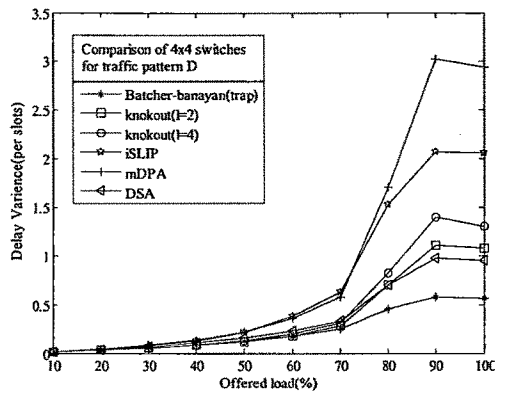


Figure 7.10 Throughput (efficiency) D (%)

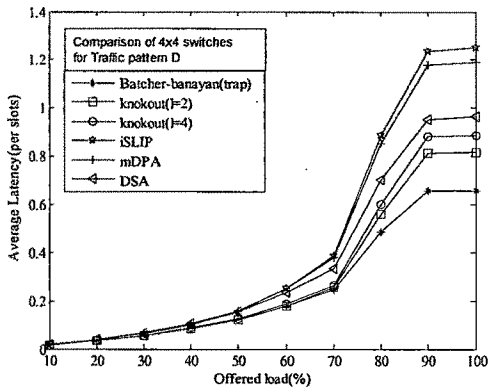


Figure 7.11 Average latency D (timeslots)

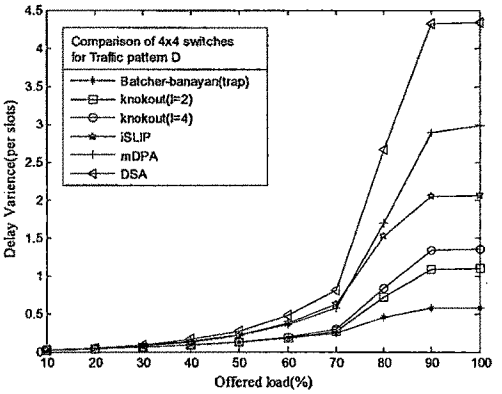


Figure 7.12 Delay variance D (timeslots)

7.2.2 8x8 SWITCHING FABRIC

A. With i.i.d. Bernoulli arrivals and uniformly distributed destinations:

Simulation results from 7.13 to 7.15 show that for this traffic model, throughput (efficiency) and average latency of DSA are at par with knockout(l=4), but delay variance is 2 to 8 time slots high.

B. *With i.i.d. Bernoulli arrivals and non-uniformly distributed destinations:*

Simulations are done for normally distributed destinations. Results are plotted from figure 7.16 to 7.18. Results show that for this traffic model, throughput (efficiency) and average latency are at par with knockout(l=4) but delay variance increases by 5 to 100 timeslots in DSA compared to knockout(l=4) due to QoS support.

C. With bursty arrivals and uniformly distributed destinations:

We illustrate the effect of burstiness on all the switching fabric using an on-off arrival process. Simulation results from figure 7.19 to 7.21 are shown below. They show that throughput (efficiency) and average latency of DSA are at par with knockout (l=4), but delay variance is 2-10 time slot higher than knockout (l=4).

D. *With bursty arrivals and non-uniformly distributed destinations*:

We illustrate the effect of burstiness as well as non-uniform distribution for output on DSA in this traffic model. Simulation results from figure 7.22 to 7.24 are shown below. They show that throughput (efficiency) and average latency of DSA are at par with knockout (l=4), but delay variance is 3 time slots higher than knockout (l=4).

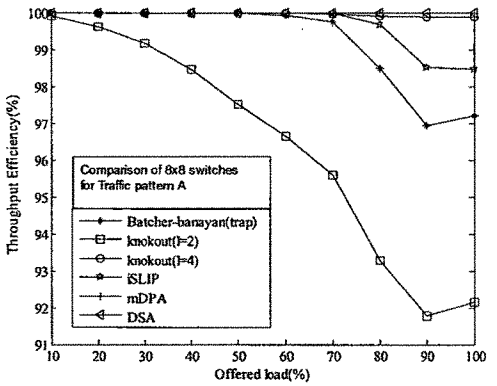


Figure 7.13 Throughput (efficiency) A (%)

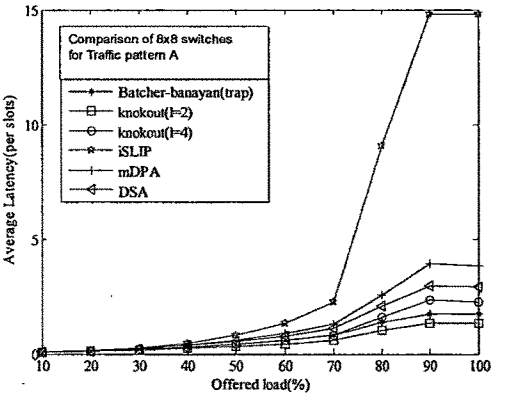


Figure 7.14 Average latency A (timeslots)

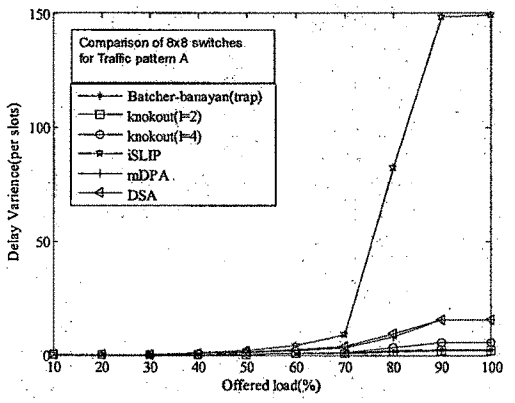


Figure 7.15 Delay variance A (timeslots)

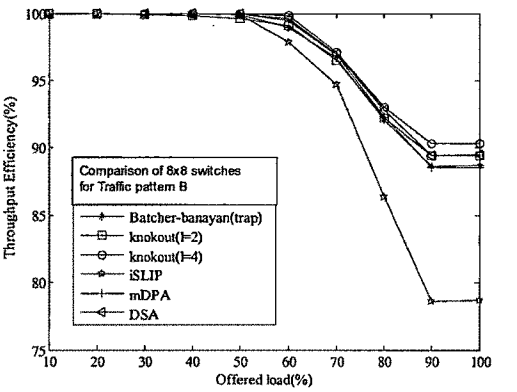


Figure 7.16 Throughput (efficiency) B (%)

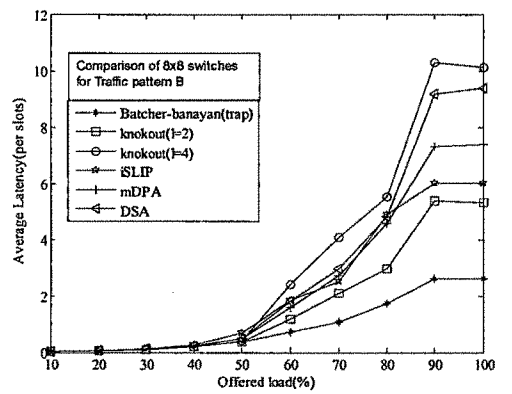


Figure 7.17Average latency B (timeslots)

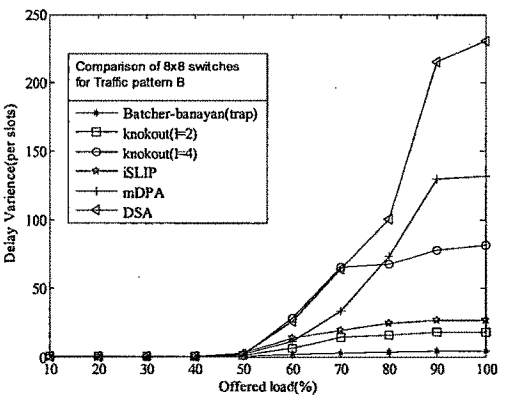


Figure 7.18 Delay variance B (timeslots)

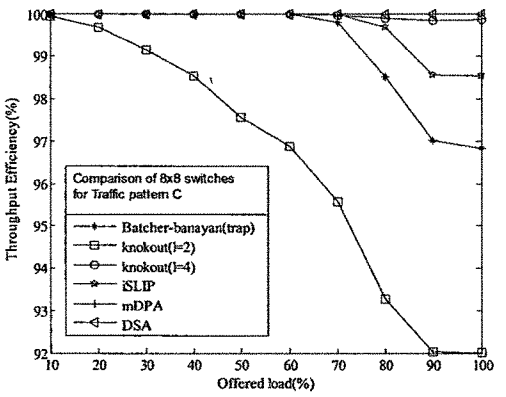


Figure 7.19 Throughput (efficiency) C (%)

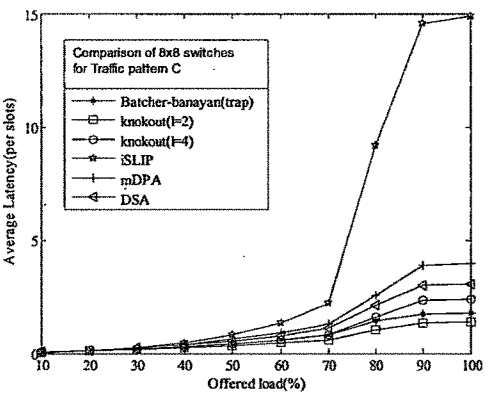


Figure 7.20 Average latency C (timeslots)

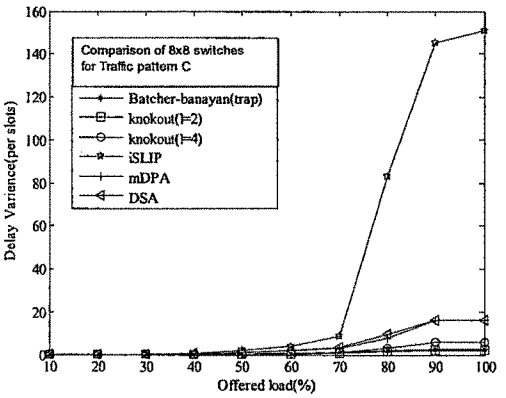


Figure 7.21 Delay variance C (timeslots)

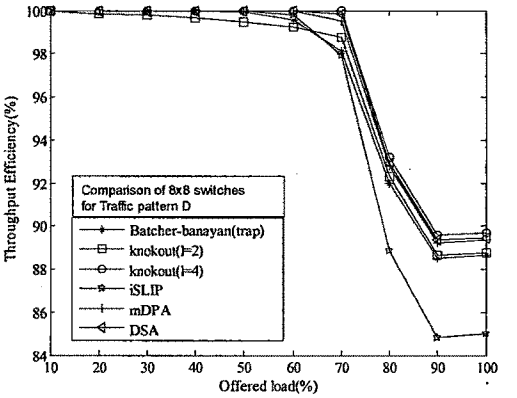


Figure 7.22 Throughput (efficiency) D (%)

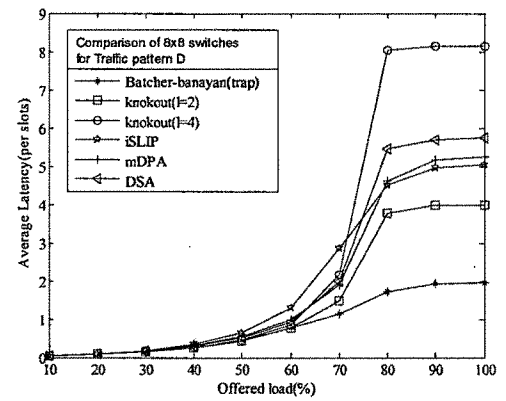


Figure 7.23 Average latency D (timeslots)

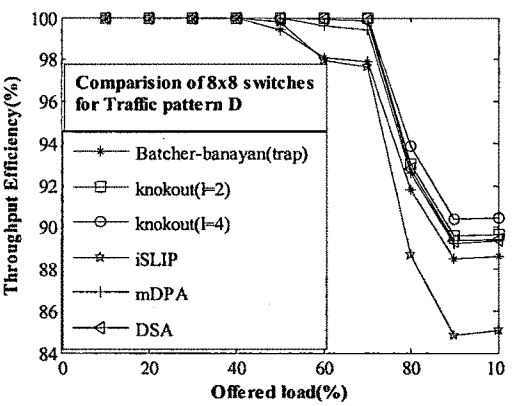


Figure 7.24 Delay variance D (timeslots)

7.3 COMPARISON OF SWITCHES

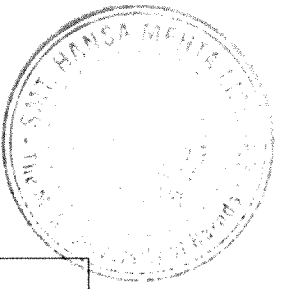
We have applied four different traffic patterns (A, B, C, D) to all the switches and throughput (efficiency), average latency and delay variance are plotted in chapter 4, 5 and 6.

Table 7.1 MATLAB simulation result comparison for 4x4 switches

Switches (scheduling algorithm) 4x4	MATLAB Simulation Speed (in second)	Throughput (efficiency) in Percentage	Average Latency in Time Slot	Delay Variance in Time Slot
BATCHER BANYAN TRAP	0.074	88.860	0.945	0.683
KNOCK OUT L=2	0.012	91.316	1.781	2.644
KNOCK OUTL=4	0.024	94.333	3.719	10.710
CROSSBAR (PIM)	0.051	76.070	3.234	14.320
CROSSBAR (RRM)	0.029	72.401	4.078	31.019
CROSSBAR (iSLIP)	0.030	80.841	2.471	4.702
CROSSBAR (RPA)	0.0299	84.975	1.981	4.158
CROSSBAR (DPA)	0.009	85.117	2.021	3.423
CROSSBAR (mDPA)	0.010	86.470	2.198	5.232
CROSSBAR (DSA)	0.020	88.715	2.235	23.033

Table 7.2 VLSI implementation result comparison for 4x4 switches

Scheduling Algo./ Project 4x4	Total Logic Elements (Device EP20k1500EB C652-1)	Total Pins	Total Memory Bits	Maximum clock Frequency (In MHz)
RRM ATM_RRM_4x4	5,722 / 51,840 (11 %)	87 / 488 (18 %)	33,920 / 442,368 (8 %)	37.92
iSLIP ATM_iSLIP_4x4	5,707 / 51,840 (11 %)	87 / 488 (18 %)	33,920 / 442,368 (8 %)	39.70
RPA ATM_RPA_4x4	5,810 / 51,840 (11 %)	87/ 488 (18 %)	33,920 / 442,368 (8 %)	10.51
DPA ATM_DPA_4x4	5,656 / 51,840 (11 %)	87 / 488 (18 %)	33,920 / 442,368 (8 %)	13.59



mDPA ATM_DAP44m	5,816 / 51,840 (11 %)	87 / 488 (18 %)	33,920 / 442,368 (8 %)	13.09
DSA ATM_DSA_4x4	6,907 / 51,840 (13 %)	111 / 488 (23 %)	33,920 / 442,368 (8 %)	32.18

Table 7.3 MATLAB simulation result comparison for 8x8 switches

Switches (scheduling algorithm) 8x8	MATLAB Simulation Speed (in Second)	Throughput (efficiency) in Percentage	Average Latency in Time Slot	Delay Variance in Time Slot
BATCHER BANYAN TRAP	1.86	92.853	2.017125	3.10805
KNOCK OUT L=2	0.17	90.580	3.0031	10.227625
KNOCK OUT L=4	0.18	94.945	5.73395	46.989325
CROSSBAR (PIM)	0.79	76.435	11.100525	69.606175
CROSSBAR (RRM)	0.43	75.073	12.51785	165.746725
CROSSBAR (iSLIP)	0.39	86.075	7.068725	16.6163
CROSSBAR (RPA)	5.07	93.001	4.4068	9.83375
CROSSBAR (DPA)	4.48	93.071	4.5047	9.32245
CROSSBAR (mDPA)	4.56	94.346	5.001325	16.7283
CROSSBAR (DSA)	0.34	95.975	5.05715	55.252275

Table 7.4 VLSI implementation result comparison for 8x8 switches

Scheduling Algo./ Project 8x8	Total Logic Elements (Device EP20k1500EB C652-1)	Total Pins	Total Memory Bits	Maximum clock Frequency (In MHz)
RRM ATM_RRM_8x8	26,380 / 51,840 (51 %)	178 / 488 (36 %)	133,376/442,368 (30%)	21.72
iSLIP ATM_iSLIP_8x8	26,067 / 51,840 (50 %)	178 / 488 (36 %)	133,376/442,368 (30%)	21.08
RPA ATM_RPA_8x8	22,855 / 51,840 (44 %)	178 / 488 (36%)	133,376 / 442,368 (30 %)	6.78
DPA ATM_DPA_8x8	22,778 / 51,840 (44 %)	178 / 488 (36 %)	133,376 / 442,368 (30 %)	6.66
mDPA ATM_DPA_88md	23,178/51,840 (45%)	178 / 488 (36 %)	136,960/ 442,368 (31 %)	6.76
DSA ATM_DSA_88	25,558 / 51,840 (49 %)	226 / 488 (46 %)	133,376 / 442,368 (30 %)	23.56

Average results (MATLAB simulation speed, throughput (efficiency), average latency and delay variance) of all the traffic patterns are tabulated in table 7.1 for 4x4 switch, in table 7.3 for 8x8 switch, in table 7.5 for 16x16 switch and in table 7.6 for 32x32 switch at offered load of 100% and buffer size of 2 in 4x4 switches, 3 in 8x8 and 16x16 switches and 4 in 32x32 switches.

Table 7.5 MATLAB simulation result comparison for 16x16 switches

Switches (scheduling algorithm) 16x16	MATLAB Simulation Speed (in Second)	Throughput (efficiency) in Percentage	Average Latency in Time Slot	Delay Variance in Time Slot
CROSSBAR (PIM)	1.971	79.239	18.944	472.584
CROSSBAR (RRM)	1.048	79.806	20.391	664.034
CROSSBAR (iSLIP)	1.127	87.897	12.122	99.052
CROSSBAR (RPA)	57.45	91.754	5.459	32.799
CROSSBAR (DPA)	57.35	95.471	5.452	36.830
CROSSBAR (mDPA)	57.50	95.797	5.700	44.779
CROSSBAR (DSA)	1.281	97.435	6.734	86.990

Table 7.6 MATLAB simulation result comparison for 32x32 switches

Switches (scheduling algorithm) 32x32	MATLAB Simulation Speed (in Second)	Throughput (efficiency) in Percentage	Average Latency in Time Slot	Delay Variance in Time Slot
CROSSBAR (PIM)	24.54	70.315	43.108	2637.198
CROSSBAR (RRM)	2.99	71.218	46.525	2716.184
CROSSBAR (iSLIP)	4.62	78.614	29.226	664.416
CROSSBAR (RPA)	867.15	84.713	11.252	227.308
CROSSBAR (DPA)	865.95	84.709	11.250	221.765
CROSSBAR (mDPA)	860.35	84.811	11.752	276.0679
CROSSBAR (DSA)	15.04	85.229	11.027	405.475

Table 7.2 and 7.4 show the VLSI implementation results like logic element requirement, pins, memory bits and maximum clock frequency details for 4x4 and 8x8 switches respectively for buffer size of 4 using Quartus tool.