

LIST OF FIGURES

Figure No	Figure Details	Page No.
1.1	Common switch fabric architecture, and interfacing with network processor.....	002
1.2	General structure of a packet switch with input buffers.....	006
1.3	Bipartite graph G and a matching W on it.....	007
2.1	Relationship between speed of Internet Connections and time	013
2.2	Networking functionality.....	014
2.3	General Purpose Processor architecture for networking functionality.....	014
2.4	ASIP architecture for networking functionality.....	014
2.5	ASIC architecture for networking functionality.....	015
2.6	Co-processor architecture for networking functionality.....	015
2.7	FPGA for networking functionality.....	015
2.8	Programmability v/s performance aspect.....	016
2.9	First generation network system architecture.....	016
2.10	Second generation network system architecture.....	017
2.11	Third generation network system.....	017
2.12	Basic Network Processor architecture.....	018
2.13	Taxonomy of switching system.....	020
2.14	Single stage cross points matrix.....	021
2.15	A Shared Bus Architecture.....	023
2.16	Output buffer.....	026
2.17	Input buffer.....	026
2.18	Virtual Output Queuing Structure.....	027
2.19	Switches with multiple input queues.....	028
2.20	Combine input output buffer.....	029
2.21	Cross point buffer.....	029
2.22	Basic switching element.....	030
2.23	8×8 Delta network (Omega).....	030
2.24	2-input Banyan switching element.....	030
2.25(a)	4 x 4 banyan.....	031
2.25(b)	8 x 8 banyan.....	031
2.26	Starlite switch.....	032
2.27	Tandem Banyan Switch.....	032
2.28	Knockout switch architecture.....	033
3.1	Single round of IDEA.....	038
3.2	Output transformation stage of IDEA.....	039
3.3	Overall IDEA structure.....	039
3.4	Classification flowchart.....	042,043
3.5(a)	Capture by "Ethereal" software. (TCP or UDP packet only).....	044
3.5(b)	Packet classification by C program.....	044
3.6	Hardware packet classifier.....	045
3.7	Architecture overview.....	047
3.8	Dedicated module overview.....	048
3.9	C Code Example using switch-case statements.....	048
3.10	Protocol processor architecture.....	049
3.11	Compare unit.....	051
3.12	Effect of <i>Offset</i> on output from input buffer.....	052
3.13	Payload memory interfacing.....	054

3.14	Using FIFO enhance performance.....	055
3.15	Internet checksum calculation.....	056
3.16	Pseudo header (IPv4) used in TCP/UDP calculation.....	056
3.17	Pseudo header (IPv6) used in TCP/UDP calculation.....	057
3.18	Instruction format.....	058
3.19	SYN instruction format.....	058
3.20	CMP instruction format.....	058
3.21	SET instruction format.....	059
3.22	CPS instruction format.....	059
3.23	General format of JMP instruction.....	059
3.24	JMP instruction format.....	060
3.25	WAT instruction format.....	060
3.26	Contents of ILT.....	062
3.27	Contents of PLT.....	063
3.28	Contents of CLT.....	064
3.29	Simulation result of input buffer.....	067
3.30	Simulation result of ILT.....	068
3.31	Simulation result of PLT.....	069
3.32	Simulation result of CLT.....	070
3.33	Simulation result of compare unit.....	071
3.34	Simulation result of counter Unit.....	072
3.35	Simulation result of payload Memory.....	073
3.36	Simulation result of IP length counter.....	074
3.37	Simulation result of Internet checksum.....	075
3.38	Execution of instruction -1.....	076
3.39	Execution of instruction -2.....	077
4.1	NxN Knockout switch architecture.....	082
4.2	Detail architecture of output module.....	083
4.3	Detail architecture of 8x4 concentrator.....	084
4.4(a)	The 2x2 contention switch.....	084
4.4(b)	Bar states.....	084
4.4(c)	Cross states.....	084
4.5	Detail architecture of 8x8 knockout switch.....	085
4.6	Packet loss probability for the concentrator.....	086
4.7(a)	A banyan switch with eight input lines and eight output lines.....	087
4.7(b)	The routes that two cells take through the banyan switch.....	087
4.8(a)	Cells colliding in a banyan switch.....	088
4.8 (b)	Collision-free routing through a banyan switch.....	088
4.9	The switching fabric for a Batcher-Banyan switch.....	088
4.10	An example with four cells using the Batcher-Banyan switch.....	089
4.11	8x8 Batcher Banyan switch with Trap.....	089
4.12	Traffic pattern A (4x4 knockout switch, buffer size 2).....	090
4.13	Traffic pattern B (4x4 knockout switch, buffer size 2).....	090
4.14	Traffic pattern C (4x4 knockout switch, buffer size 2).....	090
4.15	Traffic pattern D (4x4 knockout switch, buffer size 2).....	090
4.16	Traffic pattern A (4x4 knockout switch, buffer size 4).....	090
4.17	Traffic pattern B (4x4 knockout switch, buffer size 4).....	090
4.18	Traffic pattern C (4x4 knockout switch, buffer size 4).....	091
4.19	Traffic pattern D (4x4 knockout switch, buffer size 4).....	091
4.20	Traffic pattern A (8x8 knockout switch, buffer size 2).....	091
4.21	Traffic pattern B (8x8 knockout switch, buffer size 2).....	091
4.22	Traffic pattern C (8x8 knockout switch, buffer size 2).....	091
4.23	Traffic pattern D (8x8 knockout switch, buffer size 2).....	091

4.24	Traffic pattern A (8x8 knockout switch, buffer size 4).....	092
4.25	Traffic pattern B (8x8 knockout switch, buffer size 4).....	092
4.26	Traffic pattern C (8x8 knockout switch, buffer size 4).....	092
4.27	Traffic pattern D (8x8 knockout switch, buffer size 4).....	092
4.28	Traffic pattern A (4x4 Banyan/Batcher-Banyan/Batcher-Banyan-Trap).....	093
4.29	Traffic pattern B (4x4 Banyan/Batcher-Banyan/Batcher-Banyan-Trap).....	093
4.30	Traffic pattern C (4x4 Banyan/Batcher-Banyan/Batcher-Banyan-Trap).....	093
4.31	Traffic pattern D (4x4 Banyan/Batcher-Banyan/Batcher-Banyan-Trap).....	093
4.32	Traffic pattern A (8x8 Banyan/Batcher-Banyan/Batcher-Banyan-Trap).....	094
4.33	Traffic pattern B (8x8 Banyan/Batcher-Banyan/Batcher-Banyan-Trap).....	094
4.34	Traffic pattern C (8x8 Banyan/Batcher-Banyan/Batcher-Banyan-Trap).....	094
4.35	Traffic pattern D (8x8 Banyan/Batcher-Banyan/Batcher-Banyan-Trap).....	094
4.36	Implementation packet format.	095
4.37	Waveform of filter for destination address "000".....	095
4.38	Waveform of contention.....	096
4.39	Waveform of 4x4 shifter.....	096
4.40	Waveform of buffer read clock generator.....	096
4.41	Waveform of buffer write clock generator.....	097
4.42	Waveform of output selector.....	097
4.43	Waveform of 8x4 concentrator.....	097
4.44	Waveform of output module unit for output 1.....	098
4.45	2x2 Banyan switching element.....	100
4.46	Waveform of 2x2 Banyan switching element.....	100
4.47	Waveform of 8x8 Banyan switch.....	101
4.48	2x2 Batcher up module.....	101
4.49	Waveform of 2x2 Batcher up module.....	101
4.50	2x2 Batcher down module.....	102
4.51	Waveform 2x2 Batcher down module.....	102
4.52	Waveform of 8x8 Batcher sorter.....	102
4.53	Waveform of 8x8 Batcher Banyan switch.....	103
4.54	Waveform of 16x16 Trap switch.....	104
4.55	Waveform of 8x8 Batcher Banyan switch with Trap.....	105
5.1	RRM scheduling algorithm (a) Request (b) Grant (c) Accept.....	111
5.2	Two dimensional ripple-carry arbiter (a) request (b) grant.....	112
5.3	The RPA arbiter cell.....	113
5.4	Internal combinational logic of RPA cell.....	113
5.5	Arbitration cell for RPA.....	114
5.6(a)	A cyclic two-dimensional ripple carry arbiter architecture.....	115
5.6(b)	Selected cells (in the shaded squares) with highest priority cell (1,1)....	115
5.7	RPA architecture with highest priority cell (1, 1).....	116
5.8	RPA architecture with highest priority cell (1, 2).....	116
5.9	Diagonal Propagation Arbiter (DPA).....	117
5.10	Diagonal Propagation Arbiter (DPA) with highest priority to the diagonal I....	118
5.11	Modified arbitration cell for diagonal propagation arbiter (DPA) architecture.....	119
5.12	Diagonal Propagation Arbiter (DPA) with highest priority to the diagonal III ..	119
5.13	Throughput (%) v/s offered load (traffic model A,4x4 switch).....	120
5.14	Throughput (%) v/s buffer size (traffic model A,4x4 switch).....	120
5.15	Average Latency v/s offered load (traffic model A,4x4 switch).....	120
5.16	Average Latency v/s buffer size (traffic model A,4x4 switch).....	120
5.17	Delay variance v/s offered load (traffic model A,4x4 switch).....	121
5.18	Delay variance v/s buffer size (traffic model B,4x4 switch).....	121
5.19	Throughput (%) v/s offered load (traffic model B,4x4 switch).....	121
5.20	Throughput (%) v/s buffer size (traffic model B,4x4 switch).....	121

5.21	Average Latency v/s offered load	(traffic model B,4x4 switch).....	121
5.22	Average Latency v/s buffer size	(traffic model B,4x4 switch).....	121
5.23	Delay variance v/s offered load	(traffic model B,4x4 switch).....	122
5.24	Delay variance v/s buffer size	(traffic model B,4x4 switch).....	122
5.25	Throughput (%) v/s offered load	(traffic model C,4x4 switch).....	122
5.26	Throughput (%) v/s buffer size	(traffic model C,4x4 switch).....	122
5.27	Average Latency v/s offered load	(traffic model C,4x4 switch)	122
5.28	Average Latency v/s buffer size	(traffic model C,4x4 switch).....	122
5.29	Delay variance v/s offered load	(traffic model C,4x4 switch).....	123
5.30	Delay variance v/s buffer size	(traffic model C,4x4 switch).....	123
5.31	Throughput (%) v/s offered load	(traffic model D,4x4 switch).....	123
5.32	Throughput (%) v/s buffer size	(traffic model D,4x4 switch).....	123
5.33	Average Latency v/s offered load	(traffic model D,4x4 switch).....	123
5.34	Average Latency v/s buffer size	(traffic model D,4x4 switch).....	123
5.35	Delay variance v/s offered load	(traffic model D,4x4 switch).....	124
5.36	Delay variance v/s buffer size	(traffic model D,4x4 switch).....	124
5.37	Throughput (%) v/s offered load	(traffic model A,8x8 switch).....	126
5.38	Throughput (%) v/s buffer size	(traffic model A,8x8 switch).....	126
5.39	Average Latency v/s offered load	(traffic model A,8x8 switch).....	126
5.40	Average Latency v/s buffer size	(traffic model A,8x8 switch).....	126
5.41	Delay variance v/s offered load	(traffic model A,8x8 switch).....	126
5.42	Delay variance v/s buffer size	(traffic model B,8x8 switch).....	126
5.43	Throughput (%) v/s offered load	(traffic model B,8x8 switch).....	127
5.44	Throughput (%) v/s buffer size	(traffic model B,8x8 switch).....	127
5.45	Average Latency v/s offered load	(traffic model B,8x8 switch).....	127
5.46	Average Latency v/s buffer size	(traffic model B,8x8 switch).....	127
5.47	Delay variance v/s offered load	(traffic model B,8x8 switch).....	127
5.48	Delay variance v/s buffer size	(traffic model B,8x8 switch).....	127
5.49	Throughput (%) v/s offered load	(traffic model C,8x8 switch).....	128
5.50	Throughput (%) v/s buffer size	(traffic model C,8x8 switch).....	128
5.51	Average Latency v/s offered load	(traffic model C,8x8 switch).....	128
5.52	Average Latency v/s buffer size	(traffic model C,8x8 switch).....	128
5.53	Delay variance v/s offered load	(traffic model C,8x8 switch).....	128
5.54	Delay variance v/s buffer size	(traffic model C,8x8 switch)	128
5.55	Throughput (%) v/s offered load	(traffic model D,8x8 switch).....	129
5.56	Throughput (%) v/s buffer size	(traffic model D,8x8 switch).....	129
5.57	Average Latency v/s offered load	(traffic model D,8x8 switch).....	129
5.58	Average Latency v/s buffer size	(traffic model D,8x8 switch).....	129
5.59	Delay variance v/s offered load	(traffic model D,8x8 switch).....	129
5.60	Delay variance v/s buffer size	(traffic model D,8x8 switch).....	129
5.61	Throughput (%) v/s offered load	(traffic model A,16x16 switch).....	131
5.62	Throughput (%) v/s buffer size	(traffic model A, 16x16 switch).....	131
5.63	Average Latency v/s offered load	(traffic model A, 16x16 switch).....	132
5.64	Average Latency v/s buffer size	(traffic model A, 16x16 switch).....	132
5.65	Delay variance v/s offered load	(traffic model A, 16x16 switch).....	132
5.66	Delay variance v/s buffer size	(traffic model B, 16x16 switch).....	132
5.67	Throughput (%) v/s offered load	(traffic model B, 16x16 switch).....	132
5.68	Throughput (%) v/s buffer size	(traffic model B, 16x16 switch).....	132
5.69	Average Latency v/s offered load	(traffic model B, 16x16 switch).....	133
5.70	Average Latency v/s buffer size	(traffic model B, 16x16 switch).....	133
5.71	Delay variance v/s offered load	(traffic model B, 16x16 switch).....	133
5.72	Delay variance v/s buffer size	(traffic model B, 16x16 switch).....	133
5.73	Throughput (%) v/s offered load	(traffic model C, 16x16 switch).....	133
5.74	Throughput (%) v/s buffer size	(traffic model C, 16x16 switch).....	133
5.75	Average Latency v/s offered load	(traffic model C, 16x16 switch).....	134

5.76	Average Latency v/s buffer size	(traffic model C, 16x16 switch).....	134
5.77	Delay variance v/s offered load	(traffic model C, 16x16 switch).....	134
5.78	Delay variance v/s buffer size	(traffic model C, 16x16 switch).....	134
5.79	Throughput (%) v/s offered load	(traffic model D, 16x16 switch).....	134
5.80	Throughput (%) v/s buffer size	(traffic model D, 16x16 switch).....	134
5.81	Average Latency v/s offered load	(traffic model D, 16x16 switch).....	135
5.82	Average Latency v/s buffer size	(traffic model D, 16x16 switch).....	135
5.83	Delay variance v/s offered load	(traffic model D, 16x16 switch).....	135
5.84	Delay variance v/s buffer size	(traffic model D, 16x16 switch).....	135
5.85	Throughput (%) v/s offered load	(traffic model A,32x32 switch).....	135
5.86	Throughput (%) v/s buffer size	(traffic model A, 32x32 switch).....	135
5.87	Average Latency v/s offered load	(traffic model A, 32x32 switch).....	136
5.88	Average Latency v/s buffer size	(traffic model A, 32x32 switch).....	136
5.89	Delay variance v/s offered load	(traffic model A, 32x32 switch).....	136
5.90	Delay variance v/s buffer size	(traffic model B, 32x32 switch).....	136
5.91	Throughput (%) v/s offered load	(traffic model B, 32x32 switch).....	136
5.92	Throughput (%) v/s buffer size	(traffic model B, 32x32 switch).....	136
5.93	Average Latency v/s offered load	(traffic model B, 32x32 switch).....	137
5.94	Average Latency v/s buffer size	(traffic model B, 32x32 switch).....	137
5.95	Delay variance v/s offered load	(traffic model B, 32x32 switch).....	137
5.96	Delay variance v/s buffer size	(traffic model B, 32x32 switch).....	137
5.97	Throughput (%) v/s offered load	(traffic model C, 32x32 switch).....	137
5.98	Throughput (%) v/s buffer size	(traffic model C, 32x32 switch).....	137
5.99	Average Latency v/s offered load	(traffic model C, 32x32 switch).....	138
5.100	Average Latency v/s buffer size	(traffic model C, 32x32 switch).....	138
5.101	Delay variance v/s offered load	(traffic model C, 32x32 switch).....	138
5.102	Delay variance v/s buffer size	(traffic model C, 32x32 switch).....	138
5.103	Throughput (%) v/s offered load	(traffic model D, 32x32 switch).....	138
5.104	Throughput (%) v/s buffer size	(traffic model D, 32x32 switch).....	138
5.105	Average Latency v/s offered load	(traffic model D, 32x32 switch).....	139
5.106	Average Latency v/s buffer size	(traffic model D, 32x32 switch).....	139
5.107	Delay variance v/s offered load	(traffic model D, 32x32 switch).....	139
5.108	Delay variance v/s buffer size	(traffic model D, 32x32 switch).....	139
5.109	Basic Architecture of input queue NxN cross bar switch.....		140
5.110(a)	An ATM cell.....		141
5.110(b)	ATM cell header detail.....		141
5.111	Input_port internal architecture.....		141
5.112	The VOQ buffer in each input_port module.....		142
5.113	General NxN Switch fabric module.....		144
5.114	4x4 RRM scheduler block.....		146
5.115	Simulation waveform of Port_Req_Gen.....		146
5.116	Simulation waveform of GRT_RRM.....		147
5.117	Simulation waveform of Port_GRT_Gen.....		147
5.118	Simulation waveform of ACPT_RRM.....		147
5.119	Simulation waveform of CLKIPDRM.....		148
5.120	Internal detail of iSlip Scheduler.....		148
5.121	Simulation waveform of iSlip scheduler.....		149
5.122	Internal detail of RPA Scheduler.....		150
5.123	Simulation waveform of RPA_scheduler.....		151
5.124	Internal detail of DPA Scheduler.....		151
5.125	Simulation waveform of Scheduler for DPA.....		152
6.1	m-DPA architecture.....		156
6.2	DSA Scheduler Architecture.....		157
6.3	Throughput (%) v/s offered load (traffic model A,4x4 switch).....		159

6.4	Throughput (%) v/s buffer size	(traffic model A,4x4 switch).....	159
6.5	Average Latency v/s offered load	(traffic model A,4x4 switch).....	159
6.6	Average Latency v/s buffer size	(traffic model A,4x4 switch).....	159
6.7	Delay variance v/s offered load	(traffic model A,4x4 switch).....	159
6.8	Delay variance v/s buffer size	(traffic model A,4x4 switch).....	159
6.9	Throughput (%) v/s offered load	(traffic model B,4x4 switch).....	160
6.10	Throughput (%) v/s buffer size	(traffic model B,4x4 switch).....	160
6.11	Average Latency v/s offered load	(traffic model B,4x4 switch).....	160
6.12	Average Latency v/s buffer size	(traffic model B,4x4 switch).....	160
6.13	Delay variance v/s offered load	(traffic model B,4x4 switch).....	160
6.14	Delay variance v/s buffer size	(traffic model B,4x4 switch).....	160
6.15	Throughput (%) v/s offered load	(traffic model C,4x4 switch).....	161
6.16	Throughput (%) v/s buffer size	(traffic model C,4x4 switch).....	161
6.17	Average Latency v/s offered load	(traffic model C,4x4 switch).....	161
6.18	Average Latency v/s buffer size	(traffic model C,4x4 switch).....	161
6.19	Delay variance v/s offered load	(traffic model C,4x4 switch).....	162
6.20	Delay variance v/s buffer size	(traffic model C,4x4 switch).....	162
6.21	Throughput (%) v/s offered load	(traffic model D,4x4 switch).....	162
6.22	Throughput (%) v/s buffer size	(traffic model D,4x4 switch).....	162
6.23	Average Latency v/s offered load	(traffic model D,4x4 switch).....	163
6.24	Average Latency v/s buffer size	(traffic model D,4x4 switch).....	163
6.25	Delay variance v/s offered load	(traffic model D,4x4 switch).....	163
6.26	Delay variance v/s buffer size	(traffic model D,4x4 switch).....	163
6.27	Throughput (%) v/s offered load	(traffic model A,8x8 switch).....	164
6.28	Throughput (%) v/s buffer size	(traffic model A,8x8 switch).....	164
6.29	Average Latency v/s offered load	(traffic model A,8x8 switch).....	164
6.30	Average Latency v/s buffer size	(traffic model A,8x8 switch).....	164
6.31	Delay variance v/s offered load	(traffic model A,8x8 switch).....	164
6.32	Delay variance v/s buffer size	(traffic model B,8x8 switch).....	164
6.33	Throughput (%) v/s offered load	(traffic model B,8x8 switch).....	165
6.34	Throughput (%) v/s buffer size	(traffic model B,8x8 switch).....	165
6.35	Average Latency v/s offered load	(traffic model B,8x8 switch).....	165
6.36	Average Latency v/s buffer size	(traffic model B,8x8 switch).....	165
6.37	Delay variance v/s offered load	(traffic model B,8x8 switch).....	165
6.38	Delay variance v/s buffer size	(traffic model B,8x8 switch).....	165
6.39	Throughput (%) v/s offered load	(traffic model C,8x8 switch).....	166
6.40	Throughput (%) v/s buffer size	(traffic model C,8x8 switch).....	166
6.41	Average Latency v/s offered load	(traffic model C,8x8 switch).....	166
6.42	Average Latency v/s buffer size	(traffic model C,8x8 switch).....	166
6.43	Delay variance v/s offered load	(traffic model C,8x8 switch).....	167
6.44	Delay variance v/s buffer size	(traffic model C,8x8 switch).....	167
6.45	Throughput (%) v/s offered load	(traffic model D,8x8 switch).....	167
6.46	Throughput (%) v/s buffer size	(traffic model D,8x8 switch).....	167
6.47	Average Latency v/s offered load	(traffic model D,8x8 switch).....	168
6.48	Average Latency v/s buffer size	(traffic model D,8x8 switch).....	168
6.49	Delay variance v/s offered load	(traffic model D,8x8 switch).....	168
6.50	Delay variance v/s buffer size	(traffic model D,8x8 switch).....	168
6.51	Throughput (%) v/s offered load	(traffic model A,16x16 switch).....	169
6.52	Throughput (%) v/s buffer size	(traffic model A, 16x16 switch).....	169
6.53	Average Latency v/s offered load	(traffic model A, 16x16 switch).....	169
6.54	Average Latency v/s buffer size	(traffic model A, 16x16 switch).....	169
6.55	Delay variance v/s offered load	(traffic model A, 16x16 switch).....	169
6.56	Delay variance v/s buffer size	(traffic model B, 16x16 switch).....	169
6.57	Throughput (%) v/s offered load	(traffic model B, 16x16 switch).....	170
6.58	Throughput (%) v/s buffer size	(traffic model B, 16x16 switch).....	170

6.59	Average Latency v/s offered load	(traffic model B, 16x16 switch).....	170
6.60	Average Latency v/s buffer size	(traffic model B, 16x16 switch).....	170
6.61	Delay variance v/s offered load	(traffic model B, 16x16 switch).....	170
6.62	Delay variance v/s buffer size	(traffic model B, 16x16 switch).....	170
6.63	Throughput (%) v/s offered load	(traffic model C, 16x16 switch).....	171
6.64	Throughput (%) v/s buffer size	(traffic model C, 16x16 switch).....	171
6.65	Average Latency v/s offered load	(traffic model C, 16x16 switch).....	171
6.66	Average Latency v/s buffer size	(traffic model C, 16x16 switch).....	171
6.67	Delay variance v/s offered load	(traffic model C, 16x16 switch).....	172
6.68	Delay variance v/s buffer size	(traffic model C, 16x16 switch).....	172
6.69	Throughput (%) v/s offered load	(traffic model D, 16x16 switch).....	172
6.70	Throughput (%) v/s buffer size	(traffic model D, 16x16 switch).....	172
6.71	Average Latency v/s offered load	(traffic model D, 16x16 switch).....	173
6.72	Average Latency v/s buffer size	(traffic model D, 16x16 switch).....	173
6.73	Delay variance v/s offered load	(traffic model D, 16x16 switch).....	173
6.74	Delay variance v/s buffer size	(traffic model D, 16x16 switch).....	173
6.75	Throughput (%) v/s offered load	(traffic model A, 32x32 switch).....	173
6.76	Throughput (%) v/s buffer size	(traffic model A, 32x32 switch).....	173
6.77	Average Latency v/s offered load	(traffic model A, 32x32 switch).....	174
6.78	Average Latency v/s buffer size	(traffic model A, 32x32 switch).....	174
6.79	Delay variance v/s offered load	(traffic model A, 32x32 switch).....	174
6.80	Delay variance v/s buffer size	(traffic model B, 32x32 switch).....	174
6.81	Throughput (%) v/s offered load	(traffic model B, 32x32 switch).....	174
6.82	Throughput (%) v/s buffer size	(traffic model B, 32x32 switch).....	174
6.83	Average Latency v/s offered load	(traffic model B, 32x32 switch).....	175
6.84	Average Latency v/s buffer size	(traffic model B, 32x32 switch).....	175
6.85	Delay variance v/s offered load	(traffic model B, 32x32 switch).....	175
6.86	Delay variance v/s buffer size	(traffic model B, 32x32 switch).....	175
6.87	Throughput (%) v/s offered load	(traffic model C, 32x32 switch).....	175
6.88	Throughput (%) v/s buffer size	(traffic model C, 32x32 switch).....	175
6.89	Average Latency v/s offered load	(traffic model C, 32x32 switch).....	176
6.90	Average Latency v/s buffer size	(traffic model C, 32x32 switch).....	176
6.91	Delay variance v/s offered load	(traffic model C, 32x32 switch).....	176
6.92	Delay variance v/s buffer size	(traffic model C, 32x32 switch).....	176
6.93	Throughput (%) v/s offered load	(traffic model D, 32x32 switch).....	176
6.94	Throughput (%) v/s buffer size	(traffic model D, 32x32 switch).....	176
6.95	Average Latency v/s offered load	(traffic model D, 32x32 switch).....	177
6.96	Average Latency v/s buffer size	(traffic model D, 32x32 switch).....	177
6.97	Delay variance v/s offered load	(traffic model D, 32x32 switch).....	177
6.98	Delay variance v/s buffer size	(traffic model D, 32x32 switch).....	177
6.99	Throughput (%) v/s offered load	(High QoS traffic model A, 4x4 switch)...	178
6.100	Throughput (%) v/s buffer size	(High QoS traffic model A, 4x4 switch)....	178
6.101	Average Latency v/s offered load	(High QoS traffic model A, 4x4 switch).....	178
6.102	Average Latency v/s buffer size	(High QoS traffic model A, 4x4 switch)....	178
6.103	Delay variance v/s offered load	(High QoS traffic model A, 4x4 switch) ...	178
6.104	Delay variance v/s buffer size	(High QoS traffic model B, 4x4 switch)....	178
6.105	Throughput (%) v/s offered load	(High QoS traffic model B, 4x4 switch)...	179
6.106	Throughput (%) v/s buffer size	(High QoS traffic model B, 4x4 switch).....	179
6.107	Average Latency v/s offered load	(High QoS traffic model B, 4x4 switch).....	179
6.108	Average Latency v/s buffer size	(High QoS traffic model B, 4x4 switch).....	179
6.109	Delay variance v/s offered load	(High QoS traffic model B, 4x4 switch).....	179
6.110	Delay variance v/s buffer size	(High QoS traffic model B, 4x4 switch).....	179
6.111	Throughput (%) v/s offered load	(High QoS traffic model C, 4x4 switch).....	180
6.112	Throughput (%) v/s buffer size	(High QoS traffic model C, 4x4 switch).....	180
6.113	Average Latency v/s offered load	(High QoS traffic model C, 4x4 switch).....	180

6.114	Average Latency v/s buffer size (High QoS traffic model C,4x4 switch).....	180
6.115	Delay variance v/s offered load (High QoS traffic model C,4x4 switch).....	180
6.116	Delay variance v/s buffer size (High QoS traffic model C,4x4 switch).....	180
6.117	Throughput (%) v/s offered load (High QoS traffic model D,4x4 switch).....	181
6.118	Throughput (%) v/s buffer size (High QoS traffic model D,4x4 switch).....	181
6.119	Average Latency v/s offered load (High QoS traffic model D,4x4 switch).....	181
6.120	Average Latency v/s buffer size (High QoS traffic model D,4x4 switch).....	181
6.121	Delay variance v/s offered load (High QoS traffic model D,4x4 switch).....	181
6.122	Delay variance v/s buffer size (High QoS traffic model D,4x4 switch).....	181
6.123	Implementation detail of m-DPA.....	182
6.124	Simulation waveform of m-group44m.....	183
6.125	Simulation waveform of gr_arng44m.....	183
6.126	Scheduler block of DSA.....	184
6.127	Internal Architecture of Scheduler (Mix1_scheduleneu).....	185
6.128	Internal Architecture of Priority Resolver.....	187
6.129	Internal Architecture of usew_converte.....	188
6.130	Simulation waveform for ATM_CELL_SIZE_3.....	188
6.131	Simulation waveform for QoS.....	188
6.132	Simulation waveform for mult24.....	189
6.133	Simulation waveform for mixer.....	189
6.134	Internal Architecture of basic Batchter sorter.....	189
6.135	Simulation waveform for batcher_dyn0.....	189
6.136	Internal Architecture of TestZ block.....	190
6.137	Simulation waveform for clkipol.....	191
6.138	Simulation waveform for clk_swp.....	191
6.139	Simulation waveform for Globalschedipxn0.....	191
7.1	Throughput (efficiency) A (%).....	195
7.2	Average latency A (timeslots).....	195
7.3	Delay variance A (timeslots).....	195
7.4	Throughput (efficiency) B (%).....	195
7.5	4x4 Average latency B (timeslots).....	196
7.6	Delay variance B (timeslots).....	196
7.7	Throughput (efficiency) C (%).....	196
7.8	Average latency C (timeslots).....	196
7.9	Delay variance C (timeslots).....	196
7.10	Throughput (efficiency) D (%).....	196
7.11	4x4 Average latency D (timeslots).....	197
7.12	Delay variance D (timeslots).....	197
7.13	Throughput (efficiency) A (%).....	198
7.14	Average latency A (timeslots).....	198
7.15	Delay variance A (timeslots).....	198
7.16	Throughput (efficiency) B (%).....	198
7.17	8x8 Average latency B (timeslots).....	198
7.18	Delay variance B (timeslots).....	198
7.19	Throughput (efficiency) C (%).....	199
7.20	Average latency C (timeslots).....	199
7.21	Delay variance C (timeslots).....	199
7.22	Throughput (efficiency) D (%).....	199
7.23	Average latency D (timeslots).....	199
7.24	Delay variance D (timeslots).....	199
A1	Markov ON-OFF Model.....	215