❖ Summary and scope for future work

➢ Summary

Work done in this study can be grouped into three main categories. In the first stage, CIS compound is synthesized and thin films of CIS are developed as an absorber layer using two different deposition techniques viz thermal evaporation and flash evaporation. The effects of substrate temperature and heat treatment (thermal annealing) on properties of films are analyzed. In the second stage, thin films of cadmium sulphide are developed and optimized. RF magnetron sputtering method for deposition of Bi-layer Zinc Oxide, the Transparent Conducting Oxide (TCO), front Contact for CIS based solar cells is employed and deposition parameters are optimized. In the final stage, efforts are made to fabricate CIS based thin film solar cell devices with CIS layers thinner than the standard thickness values. The thickness of the CIS layer in the standard devices is 2 μm. The thickness of this layer is reduced to 0.5 μm. The initial performance of these devices are considerable, although less when compared to the standard values. The data from all the experiments showed that when the thickness of the CIS layer is reduced, the space-charge region is moved towards the back contact which causes reduction in the width of the space-charge region. As the thickness is reduced by a factor of 4 compared to the standard, there could be significant back contact recombination. The devices become electrically shunted when the thickness is reduced to 0.5 μm. The I-V curves of these devices show significant collection problems also. Hence, it is concluded that thickness of 0.5 μm affects the performance of the devices to a large extent. Therefore, efforts are made to prepare CIS based thin film solar cells having CIS thickness of 1 μm. It is found from number of attempts made to fabricate devices, that the Mo/CIS/CdS interface is very important for the optimum performance of the devices. The conductivity of the interface layers also affects the performance. An important factor contributing to the interfaces is thought to be the thickness of CdS layer. More experiments are carried out to understand the effect of the thickness of CdS buffer layer on device performance, especially when the absorber layer thickness is 1 μm. Dark I-V characterization of Mo/CIS/CdS structure is carried out.

➢ Scope for Future Work

- Study of CdS/ZnO interface for improvement of efficiency.
- Fabrication of device with CIS thickness of 1 μm.
- Replacement of CdS with other buffer layers and their interface study with CIS.
- Fabrication of CIS/CIGS based thin film tandem solar cell.