# Abstract

Thin film polycrystalline solar cells based on copper indium diselenide (CIS) are excellent candidate for clean energy production with competitive prices in the near future. CIS based thin film solar cells with efficiencies of 20.3 % for laboratory cell have already been reported. In this study, CIS absorber layers are fabricated by a single-stage direct thermal evaporation and flash evaporation process. CIS material synthesized from its' constituent elements is used to prepare CIS thin films initially, on glass substrates for optimization of deposition parameters and than on molybdenum coated glass substrates for device fabrication. The typical thickness of the absorber layers fabricated in this study is in the range of 0.3-1.0 μm.

The very thin layer of cadmium sulphide between the CIS absorber and aluminum (Al) doped zinc oxide layer, serving as transparent conducting oxide (TCO) at front is known as a "buffer" or "window" layer. Although p-n junctions will form between TCO and p-type absorber layer, the quality of the junctions is improved considerably with the introduction of an intermediate buffer layer. The effect of thickness of evaporated CdS thin films, as a hetrojunction partner to the CIS absorber layer in CIS thin film solar cell is investigated using numerical simulation as well as experimental technique.

The ZnO transparent front contact, for CIS based thin film solar cell, is a bi-layer with a thin intrinsic layer (i-ZnO) and a thicker Al doped n-type layer (AZO). These layers have been fabricated using radio frequency magnetron sputtering technique from i-ZnO and AZO targets. The effect of the working pressure on the deposition of ZnO thin films are investigated in detail.

Efforts are made in this study to prepare CIS cells with reduce thickness of the CIS absorber layer, as this would translate directly into reduction in production costs and the amount of material being used. Devices with reduced absorber layer thickness of 0.5 μm is fabricated. The 0.5 μm thick CIS absorber layer based devices showed a noticeable $V_{oc}$ and $I_{sc}$. So attempts are made to fabricate devices with CIS layer thickness near to 1 μm. As CIS/CdS interface is important for the optimum performance of the devices more experiments have been carried out to understand the effect of the thickness of buffer layer on dark I-V measurements, especially when the absorber layer thickness is ~1 μm.