### **CHAPTER NINE**

### NOVEL CONCEPT FOR VOLTAGE COMPENSATION

#### 9.1 INTRODUCTION

In the present scenario, many installations face severe voltage dips passed on from the incoming supply network. These dips cause tripping of equipment connected down the line. In process industries such tripping can stall the plant (example: aluminum smelting) and cause considerable production loss. Sometimes, it can take days to get back the plant to normalcy. These dips can contaminate embedded software's and can result in robots getting parked in unwanted positions in automobile and other industries. In terms of technology, with help of current research- manufacturers do have identified the power electronics based solutions like Dynamic Voltage Restorers (DVRs) or Series Voltage Restorers (SVRs). However, economics of usage of such solution, still makes it prohibitive from wide spread usage especially for application where load variation are from few KW to few MW. Presently, in fact there are other traditional methods for addressing voltage dip/rise compensating demands for such needs but their effectiveness is limited [242]. To address this aspect, novel method, of voltage dips/rise compensation for Low Voltage (LV) distribution networks in an economical way is introduced in this chapter. This chapter, after initially highlighting the need for such a method, then gives the details of concept. It is then followed by simulation results and experimental results to establish the concept.

### 9.2 NEED FOR VOLTAGE DIP-RISE COMPENSATOR

In the last few decades the distribution networks have grown substantially. However, the number of problems faced by the consumers also has grown in equal measure. The power supply problem includes flicker, brownouts, frequency drifts, voltage distortion, unbalance and many others. One of the important aspects related to problems faced by High Tension (HT) consumers is the sudden voltage dips in the incoming HT supply. The modern controls and control stations involve high level of integration of control electronics operating at 3.3V or lower logic levels. The voltage dips in such scenario, create havoc with these control systems and many times can result in unwanted trips and restarts, apart from many times resulting in sudden hangout of operating controls and then demanding individual intervention to facilitate restarts. The unwarranted dips also affect the drives and many other power electronic controllers also.

This happens when dips are beyond the normally expected limits. The stoppage of processes, washouts, and loss of production hence are huge. There are some solutions to these issues, which can restrict the dips passed on to the sensitive controllers and loads. These are Dynamic Voltage Restorers (DVR) and / or Series Voltage Regulators (SVR). These power electronic controllers usages however, do not get justified in LV and control applications. Hence, the users have been looking for some cost effective solutions. The proposed model is based on the electromagnetic transformer, which includes winding re-connection without deploying any power electronic converter.

### 9.3 CONCEPT OF NOVEL VOLTAGE DIP AND RISE COMPENSATION

The concept for voltage dip –rise compensation using multi winding transformer, is based on achieving the phase compensation of the secondary winding of star-star connected transformer. The modified voltage for each phase will be function of all three phases. The simplified connection diagram is as given below in fig. 9.1.



Notes:-

1) Each secondary winding voltage is equal to: V<sub>R'N</sub> = x V<sub>RN</sub>,

Where  $V_{R'N'}$  is secondary voltage,  $V_{RN}$  is primary voltage, and x is turns ratio, can be 0.5 to 1, based on desired compensation.

2) Series voltage inserted in each load line 0, under balanced voltage condition.

#### Fig. 9.1 Voltage dips and sag compensation scheme

In the concept as shown in fig. 9.1 a conventional transformer with isolated secondary windings is connected, while supplying to a load under normal conditions. During the dips, the phase compensation reduces the intensity of the dip. In the same way it tries to compensate if voltage rises suddenly. Under unbalanced voltage conditions, voltage assumes the mean value. This solution, while provides a very economical approach for addressing the sudden dip and sags, it also has limitation that it does not work if all the three phase supply voltages dip or rise

simultaneously. Polarity marking of the windings is also equally important while deploying such transformer for compensation.

## 9.4 MODELING AND SIMULATION

The transformer as shown above is modeled in MATLAB environment. Shown below are the blocks.



(a) Basic System



(b) Compensating Transformer block details

Fig. 9.2 Basic MATLAB simulation block

The compensating transformer is modeled with parameters as shown in the fig. 9.3

Block Parameters: Multi-Winding Transformer	X
Multi-Winding Transformer (mask) (link)	^
Implements a transformer with multiple windings. The number of windings can be specified for the left side and for the right side of the block. Taps can be added to the upper left winding or to the upper right winding.	
Parameters	
Units: SI	*
Number of windings on left side	
1	
Number of windings on right side	
3	
Tapped winding no taps	*
Nominal power and frequency [Pn(VA) fn(Hz)]:	
[75e3 50]	=
Winding nominal voltages (U1 U2 Un) (Vrms):	
[240 240*0.65 240*0.65 240*0.65]	
Winding resistances [R1 R2 Rn] (Ohm):	
[0.011482 0.011482 0.011482 0.011482]	
Winding leakage inductances [L1 L2 Ln] (H):	
[0.00014619 0.00014619 0.00014619 0.00014619]	
Saturable core	
Magnetization resistance Rm (Ohm)	
114.82	
Magnetization reactance Lm (H)	_
114.82	

Fig. 9.3 Compensating Transformer modeling

## 9.4.1 MATLAB SIMULATIONS RESULTS

With the above system, the three phase programmable voltage source is used to feed the

system to observe the compensating response as detailed in fig.9.4

Three-Phase Programmable Voltage Source (mask) (link)	
This block implements a three phase zero impedance voltage source. The common node (neutral) of the three so Time valuation for the amplitude, phase and linequency of the fundamental can be preprogrammed. In addition, in undamental	urces is accessible via input 1 (N) of the block. In harmonics can be superimposed on the
components A and B in any sequence.	
Parameters	
Positive-sequence: [Amplitude(Vims Ph-Ph) Phase(deg.) Freq. (Hz) ]	
[415 0 50]	
Time variation of: Amplitude	~
Type of variation: Table of time-amplitude pairs	~
Variation on phase A only	
Amplitude values (pu);	
[108112100810121051151]	
Time values:	
[0 0.024 0.026 0.044 0.046 0.06 0.1 0.14 0.18 0.204 0.206 0.224 0.226]	
Fundamental and/or Harmonic generation.	
A: [Order(n) Amplitude(pu) Phase(degrees) Seq(0, 1 or 2)]	
[3 0 2 -25 0]	
8: [Order(n) Amplitude(pu) Phase(degrees) Seq[0, 1 or 2)]	
[2 0 15 35 2]	
Timing (s): [Start End]	

Fig. 9.4 Input source modeling for voltage dip/rise simulation

Voltage of R Phase is varied as follow. For initial first cycle all the three phase voltages are maintained balanced. Then around the peak of 2<sup>nd</sup> cycle (from 24 to 26ms) voltage of Phase R is lowered to 80% value (20% voltage dip) for 2ms i.e. during 2nd cycle only. Subsequently during 3<sup>rd</sup> cycle peak, voltage is increased to 120% value for phase R (20% voltage rise) for 2ms i.e. during 3<sup>rd</sup> cycle. Similarly, voltage sag of 20% is introduced during 4<sup>th</sup> and 5<sup>th</sup> cycle and 20% swell during 8<sup>th</sup> and 9<sup>th</sup> cycle. On the same lines, 50% sag and swell for 2 ms are introduced during peak of 11<sup>th</sup> and 12<sup>th</sup> Cycle respectively.

The simulation responses are given in fig. 9.5 and fig. 9.6







(b) R phase input and output profile

Fig. 9.5 R phase input and output voltage profile under dip and rise conditions



(a) Three phase input and output voltage response under dip and rise

### conditions...contd.



### (b) Three phase input and output voltage response under dip and rise conditions

### Fig. 9.6 Three phase voltage profile under dip and rise conditions

The simulation results above very clearly shows that by maintaining proper ratio of the secondary windings effective reduction in the voltage dip-rise manifestation on the output side can be achieved.

## 9.5 EXPERIMENTAL SETUP AND RESULTS

Subsequent to above simulation, a three phase 10 kVA transformer for achieving the voltage dip-rise compensation is designed and manufactured with specifications as given in table 9.1.

## Table 9.1 Specification of Voltage Dip-Rise compensating transformer

Transformer Specification		1U • 2u1	
3 phase Rating (kVA)	10	• 2u2	
Winding connection	Star/Star splitted (see figure)	2u2' 2u3	
Vector group	Ynyn0	1Un2u3'	
Number of phases Terminals	Input 3 ph (one winding per phase), Output 3 ph (three winding per phase) 3 Input, 12 output (6 per phase)	1V • 2v1	
Frequency(Hz)	50	• 2v2	
Type of cooling	ONAN/ AN (Air cooling prefrable)	2v2' 2v3	
Impedance Data	As per IS 1180	1Vn 2v3	
Тар	Not required	1W 2wl	
Losses (Iron and Copper)	As per IS 1180	2w1	
Insulation level	As per IS 1180	• 2w2	
Bushings (HV & LV)	As per IS 1180	• 2w3	
Winding Voltage		1Wn 2w3'	
1U-1Un, 1V-1Vn, 1W-1Wn 2u1-2u1', 2u2-2u2', 2u3-2u3'	415/sqrt(3)		
2v1-2v1', 2v2-2v2', 2v3-2v3' 2w1-2w1', 2w2-2w2', 2w3-2w3'	0.667*415/sqrt(3)		

Experimental setup then was created to validate the simulation results and same are presented

below fig. 9.7



Fig. 9.7 Experimental setup

Expected performance of the designed transformer is as per below Table 9.2

### Table 9.2 Theoretical performance of Voltage dip/rise compensation through proposed

### transformer

#### Case 1 : Single Phase Dip

The theortical expectations are as follows:-

Absolute values					C	Deviation		
	Vm	Vyn	Vbn	Input condition remarks	Vrn'	Vyn'	Vbn'	Output condition remarks
Input	240	240	240	All phase nominal	0	0	0	
Output	240	240	240	All phase norminal	0	0	0	All phase norminal
Input	216	240	240	One phase Dip by 10%	-24	0	0	Phase Dip impact only
Output	232.008	231.996	231.996	One phase bip by 10%	-7.992	-8.004	-8.004	(10/3)=3.33%
Input	192	240	240	One phase Dip by 20%	-48	0	0	Phase Dip impact only
Output	224.016	223.992	223.992	One phase bip by 20%	-15.984	-16.008	-16.008	(20/3)=6.66%
Input	168	240	240	One phase Dip by 20%	-72	0	0	Phase Dip impact only
Output	216.024	215.988	215.988	One phase bip by 30%	-23.976	-24.012	-24.012	(30/3)=10%
Input	144	240	240	One phase Dip by 40%	-96	0	0	Phase Dip impact only
Output	208.032	207.984	207.984	One phase Dip by 40%	-31.968	-32.016	-32.016	(40/3)=13.3%

#### Case 2 : Three Phase Dip

The theortical expectations are as follows:-

		Absolute values			C	Deviation		
	Vrn	Vyn	Vbn	Input condition remarks	Vrn'	Vyn'	Vbn'	Output condition remarks
Input	240	240	240		0	0	0	
Output	240	240	240	All phase nominal	0	0	0	All phase norminal
Input	216	216	240	Two phase Dip by 10%	-24	-24	0	Phase Dip impact only
Output	224.004	224.004	223.992	Two phase Dip by 10%	-15.996	-15.996	-16.008	((10+10)/3))=6.66%
Input	192	192	240	Two obaco Dio by 20%	-48	-48	0	Phase Dip impact only
Output	208.008	208.008	207.984	Two phase Dip by 20%	-31.992	-31.992	-32.016	((20+20)/3)=13.33%
Input	168	168	240	Two phase Dip by 20%	-72	-72	0	Phase Dip impact only
Output	192.012	192.012	191.976	Two phase Dip by 30%	-47.988	-47.988	-48.024	((30+30)/3)=20%
Input	144	144	240	Two phase Dip by 40%	-96	-96	0	Phase Dip impact only
Output	176.016	176.016	175.968	1 wo phase Dip by 40%	-63.984	-63.984	-64.032	((40+40)/3)=26.66%

#### Case 3: Two Phase Dip

The theortical expectations are as follows:-

		Absolute values				Deviation		
	Vrn	Vyn	Vbn	Input condition remarks	Vrn'	Vyn'	Vbn'	Output condition remarks
Input	240	240	240		0	0	0	
Output	240	240	240	All phase nominal	0	0	0	All phase nominal
Input	216	216	216	Three phase Dip by 10%	-24	-24	-24	Phase Dip impact only
Output	216	216	216	Three phase bip by 10 %	-24	-24	-24	((10+10+10)/3))=10%
Input	192	192	192	Three phase Dip by 20%	-48	-48	-48	Phase Dip impact only
Output	192	192	192	Three phase bip by 20%	-48	-48	-48	((20+20+20)/3))=20%
Input	168	168	168	Three phase Dip by 20%	-72	-72	-72	Phase Dip impact only
Output	168	168	168	Three phase bip by 30%	-72	-72	-72	((30+30+30)/3))=30%
Input	144	144	144	Three phase Dip by 40%	-96	-96	-96	Phase Dip impact only
Output	144	144	144	Three phase bip by 40 %	-96	-96	-96	((40+40+40)/3))=40%

In the experimental setup while the R phase is fed through auto transformer so as to achieve variable input voltage dip and rise condition on the single phase, phase Y and B are fed directly from the line voltage. However, due to small unbalance between different phase directly from

the source side, a small differential voltage exist in nominal voltage across the series windings of the three phases respectively as shown in fig. 9.8.



## Fig. 9.8 Differential voltage waveforms for the R, Y, and B phase series connected

### secondaries as per the scheme at the nominal input excitation

Fig. 9.8 shows the input nominal voltage for R, Y, B Phase which are 234, 238, 242V rms and they generate 5 to 6.5V of differential voltage across the series connected secondaries.



# Fig. 9.9 Differential voltage waveforms for the R,Y,B phase series connected secondaries as per the scheme at the varying R phase excitation with 235, 220, 203V

Fig. 9.9 shows the differential voltage waveforms for the varying R phase voltages (Nominal-235V, 220V, 203V) with Y and B Phase voltage at the nominal levels of 238V, 242V rms respectively. The differential (hence the compensating) voltage generated for this case for series connected windings in the R phase (and so for other phases also) can be seen increasing with reduction of R phase input voltage.



## Fig. 9.10 Differential voltage waveforms for the R, Y and B phase series connected secondaries as per the scheme at the varying R phase excitation with 180 and 157V

Fig. 9.10 shows the differential voltage waveforms for the varying R phase voltages (Nominal-180, 157V) with Y and B Phase voltage at the nominal levels of 238V, 242V rms respectively. The differential (hence the compensating) voltage generated for this case for series connected windings in the R phase (and so for other phases also) can be seen increasing with reduction of R phase input voltage.



(a) Input –Output voltage for varying R phase



### (b) Input- Output voltage for varying R phase

# Fig. 9.11 Input and Output voltage waveforms for the R, Y, and B phase with compensating transformer at the varying R phase excitation (load side)

Fig. 9.11 shows the input and output voltage waveforms for the varying R phase voltages (Nominal- 160V, 182V, 203V, 221V, 236V) with Y and B Phase voltage at the nominal levels of 238V, 242V rms respectively. The output voltage generated with compensating effect of series windings facilitates to maintain the voltage close to the nominal values and thereby the impact of voltage dip being faced on the input side is not passed on to the output / load side voltages with the help of compensating transformer. It should also be seen that at the nominal input conditions input and output voltage profile for the R phase track practically each other (overlap in the waveforms shown in fig. 9.11).



## Fig. 9.12 Transient response of compensated voltage for sudden change in input voltage conditions on R phase Input

As can be seen from the fig. 9.12 the transformer offers excellent tracking of the voltage around the nominal value even when the voltage on the input side sees sudden rise or fall. Further it can be seen from the fig. 9.13, that there is no phase shift introduced by the transformer on the output side while providing the compensating effect.

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Fig. 9.13 Phase relationship of input and output voltage



Fig. 9.14 Voltage compensation at very low input voltage, R phase input = 138V (Ch1), R phase output = 209V (Ch2), while Y & B phase are 219 and 213 V (Ch3 and 4 respectively)



(a) Input –Output voltage for varying R phase



(b) Input- Output voltage for varying R phase

Fig. 9.15 Input and Output voltage waveforms for the R, Y, and B phase with compensating transformer at the varying R phase excitation (source side)

Shown below are waveforms for different cases of two phase coupled variation on the input side..



(a) Input –Output voltage for varying R and Y phase



### (b) Input –Output voltage for varying R and Y phase

# Fig. 9.16 Input and Output voltage waveforms for the R, Y, and B phase with compensating transformer at the varying R and Y phase excitation ( source side)

Fig. 9.16 shows the input and output voltage waveforms for the varying R and Y phase voltages The output voltage generated with compensating effect of series windings in this scenario also facilitates to maintain the voltage close to the nominal values and

thereby the impact of voltage dip being faced on the input side is not passed on to the output / load side voltages with the help of compensating transformer.



## (a) Input –Output voltage for varying R and Y phase



### (b) Input –Output voltage for varying R and Y phase

# Fig. 9.17 Input and Output voltage waveforms for the R, Y, and B phase with compensating transformer at the varying R and Y phase excitation (load side)

Transient response with two coupled phase variation is also captured in the below waveforms for the rise and dip scenarios





(a) Rise and fall effect

•••

(b) Short duration sag for coupled R and Y phase with Ch1 as Input R and Ch2,3,4 as

## output R,Y,B respectively





(a) Input –Output voltage for coupled R, Y and B phase



#### (b) Input –Output voltage for coupled R, Y and B phase

## Fig. 9.19 Waveforms for the R, Y, and B phase with compensating transformer at the coupled variation on R Y and B phase inputs (waveforms are for load side)

As can be seen from the above Fig 9.19 in case of coupled variation on 3 phase the compensating transformer is not able to offer the compensation to the sagging of the voltage.

## 9.6 SUMMARY

The experimental results as shown above do confirm the observation obtained during the simulation and theoretical expectations. As summarized in the table 9.3, the impact of dips to the tune of 20% or more in one or two phases gives results within acceptable limits by deploying proposed transformer. On tightly maintaining the transformer winding errors and winding ratios, for one line dips the voltages will be "nominal voltage -1/3 dip" and if two line dips, then the voltages will be "nominal voltage -2/3 dip".

## Table 9.3 Experimental results of voltage dip/rise compensation through designed

			Absolute values				
		Vm	Vyn	Vbn	Input condition remarks	Output condition remarks	
	Input	236	238	242			
Expected	Output	239	239	239	All phase nominal	All phase within 3 % of nominal	
Observed	Output	240	244	233			
	Input	221	238	242			
Expected	Output	234	234	234	One phase Dip by 6.36%	All phase within 5% of nominal	
Observed	Output	235	238	228			
	Input	202	238	242			
Expected	Output	227	227	227	One phase Dip by 14.41%	All phase within 8% of nominal	
Observed	Output	228	232	223			
	Input	182	238	242			
Expected	Output	221	221	221	One phase Dip by 22.88%	All phase within 10% of nominal	
Observed	Output	221	227	218			
	Input	160	238	242			
Expected	Output	213	213	213	One phase Dip by 32.22%	All phase within 13% of nominal	
Observed	Output	214	219	210			

## transformer

( Ref fig 9.9)

Case 2 Two Phase Dip

Case 1 Single Phase Dip

(Ref fig. 9.15)

			Absolute values				
		Vm	Vyn	Vbn	Input condition remarks	Output condition remarks	
	Input	238	242	240			
Expected	Output	240	240	240	All phase nominal	All phase within 3 % of nominal	
Observed	Output	243	244	237			
	Input	222	225	240			
Expected	Output	229	229	229	Two phase Dip by 7%	All phase within 6% of nominal	
Observed	Output	233	235	226			
	Input	203	206	240			
Expected	Output	216	216	216	Two phase Dip by 15%	All phase within 11% of nominal	
Observed	Output	222	223	214			
	Input	181	183	240			
Expected	Output	201	201	201	Two phase Dip by 24%	All phase within 17% of nominal	
Observed	Output	207	209	200			
	Input	160	161	240			
Expected	Output	187	187	187	Two phase Dip by 33%	All phase within 23% of nominal	
Observed	Output	196	199	186			

### Case 3 Three Phase Dip

## (Ref fig. 9.17)

			Absolute values				
		Vm	Vyn	Vbn	Input condition remarks	Output condition remarks	
	Input	240	238	242			
Expected	Output	240	240	240	All phase nominal	All phase within 3 % of nominal	
Observed	Output	247	247	240			
	Input	220	218	222			
Expected	Output	220	220	220	Three phase Dip by @8.33%	All phase dip with @ 9% of nomina	
Observed	Output	226	227	219			
	Input	201	199	203		All phase din with @ 17% of	
Expected	Output	201	201	201	Three phase Dip by @16.25%	nominal	
Observed	Output	207	209	200			
	Input	182	181	183		All phase dip with @ 25% of	
Expected	Output	182	182	182	Three phase Dip by @24.17%	nominal	
Observed	Output	184	187	181			
	Input	162	161	163		All phase dia with @ 24% of	
Expected	Output	162	162	162	Three phase Dip by @32.50%	nominal	
Observed	Output	163	166	159			

This result clearly demonstrates the resultant voltages are well within acceptable limits.

Further, it is to be noted that the transformer secondaries which comes in series in each line carry current normally at zero voltage. While, the secondaries being in series will have to be rated for full currents, however, when we look at primary , each primary winding carries reflected i<sub>r</sub>, i<sub>y</sub>, and i<sub>b</sub> (all) three currents and in a balanced condition the total primary current in each winding is zero. Under unbalanced situation only the three primary windings will carry some current. The current rating of the primary windings hence will depend upon output side / reflected unbalanced currents. So there is no active power loss as far as compensating transformer is concerned. The suggested method not only mitigates the impacts of voltage dip/rise but also equalizes the three-phase voltages. It tries to bring the voltages within acceptable band. If one needs higher accuracy (smaller band) an additional DVR/SVR then can be used, which still can help keep overall cost within acceptable limits.

#### 9.7 CONCLUSION

Such a concept can be economically very lucrative as, the concept is simple to apply in many applications. A very simple application could be control logic in a power electronic panel supplied by a 240 V phase to neutral power supply. The concept will help avoidance of relay and contactor chattering. Thus, it can bring improvements in the LV distribution at a small additional cost increase, due to cost of DT itself. It can also be used in combination with DVR depending upon the impact of duration of dips/rise and considering economics of the applications. Or purely as DVR for mitigation of voltage sag in an industrial power distribution system. Even, a consideration like modifying the DT's with this arrangement (set of three secondary windings to be added in each output line internally), can give a good edge towards selling the DT with internal compensation for voltage dip / rise.

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