3
A CURRENT CONTROLLED HARMONIC INDEX BASED PROTECTION SCHEME FOR SERIES COMPENSATED TRANSMISSION LINES

3.1 Introduction

Metal Oxide Varistors are typically placed in parallel with series capacitors [49]. These devices, known as MOVs, are crucial in the protection schemes of these capacitors. When a fault occurs and line current increases to a level significantly higher than normal, damage to the dielectric in the capacitor can occur [50]. The MOV placed in parallel with the capacitor prevents this by acting in a manner similar to a Zener diode.

In the protection of series capacitors, the use of Metal Oxide Varistors (MOV) has become common practice. These devices protect the capacitors by ensuring that the voltage across the capacitor does not exceed a certain threshold as might occur during high current faults [50]. This is accomplished by a device whose terminal characteristics resemble that of a Zener diode. When the voltage is below the threshold, the device has very high resistance. However when the voltage exceeds the level set for the device, its resistance drops very quickly and acts to short the terminals of the capacitor in order to protect the dielectric from the damaging effects of a flashover.

The device however can cause problems due to its highly non-linear nature. The resistance of this device will vary as the voltage on the capacitor terminals varies. There is however a positive side effect to all of this. When the MOV does operate (keeping in mind that not all faults will induce a current level sufficient to pass the MOV voltage threshold and activate the device), it creates a frequency signature which can be positively identified. When there is operation of an MOV, it is obvious that a series capacitor was part of the fault loop since only fault current would cause an MOV to operate and clip the voltage waveforms seen by the relay.

This chapter proposes current controlled harmonic index based protection technique using Fast Fourier Transform (FFT), which can be used to identify the presence of the capacitor in the fault loop in post fault scenario by identifying specific frequency signatures in voltage signals at relaying bus.

3.2 Protective Equipments for Series Capacitors

As mentioned earlier, protective equipment is applied to the series capacitor to protect it from the excessive voltages which can occur during faults. This equipment takes one of two basic forms: a parallel power gap or a metal-oxide varistor (MOV).

3.2.1 Parallel Power Gap

Up until the late 1970s, the power gap was the primary means of providing over voltage protection of the series capacitor. A simplified schematic of this system is shown in Figure 3.1. The gap provides protection for the capacitor by sparking over when the voltage across the capacitor exceeds a specific level. This level is known as the protective level. Usual values of protective level are 2.5 to 4.0 times normal operating voltage. A reactor is placed in series with the gap to limit the capacitor discharge current through the gap. Once current flow is initiated in the gap, a parallel bypass switch is closed to extinguish the arc in the gap. The bypass switch remains closed for a period sufficient to allow the gap to recover and then is opened automatically to reinsert the capacitor.

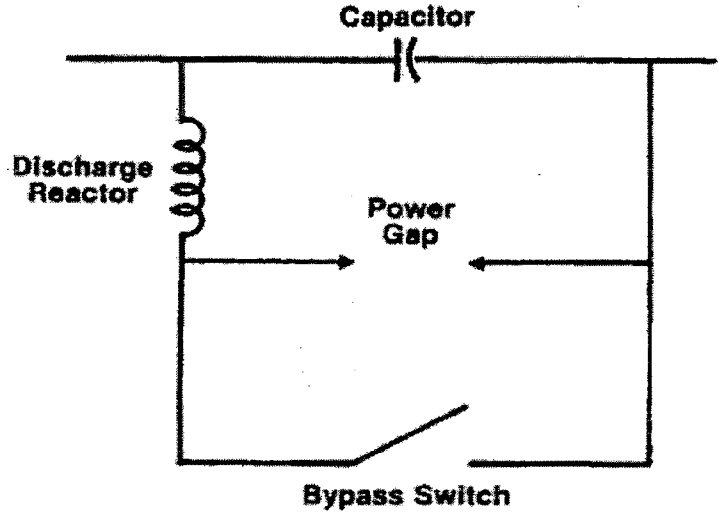


Fig.3.1 Parallel Power Gap

If the capacitor is used for transient stability improvement, then high speed reinsertion of the capacitor as well as high speed fault clearing is desirable. One of the means for providing high speed insertion is the use of a vacuum gap in place of the air gap. The vacuum gap has excellent recovery voltage withstand which allows for high speed opening of the bypass switch. Another system has achieved high speed reinsertion by extinguishing the arc by air blast rather than by closure of a parallel bypass switch. This system initiates air flow immediately upon detection of gap current. A drawback of this system is the potential for multiple spark-over of the gap for the same event which places added stress on the capacitor.

The selection of the protective level is based on the ability of the gap to withstand the various system transients such as depicted in Figure 3.2. The particular concern for a gap is, its ability to withstand the reinsertion transients. As previously discussed, reinsertion of the capacitor gives rise to sub-harmonic transients. These transients are superimposed on the normal power frequency system swings which follow the clearing of the fault. The gap must be able to withstand these combined over voltages. This results in variation in the gap spark-over level which has been evaluated on the basis of 50 Hz current flow only. The peak of this combined transient current may occur approximately 1/2 second to as long as several seconds after reinsertion.

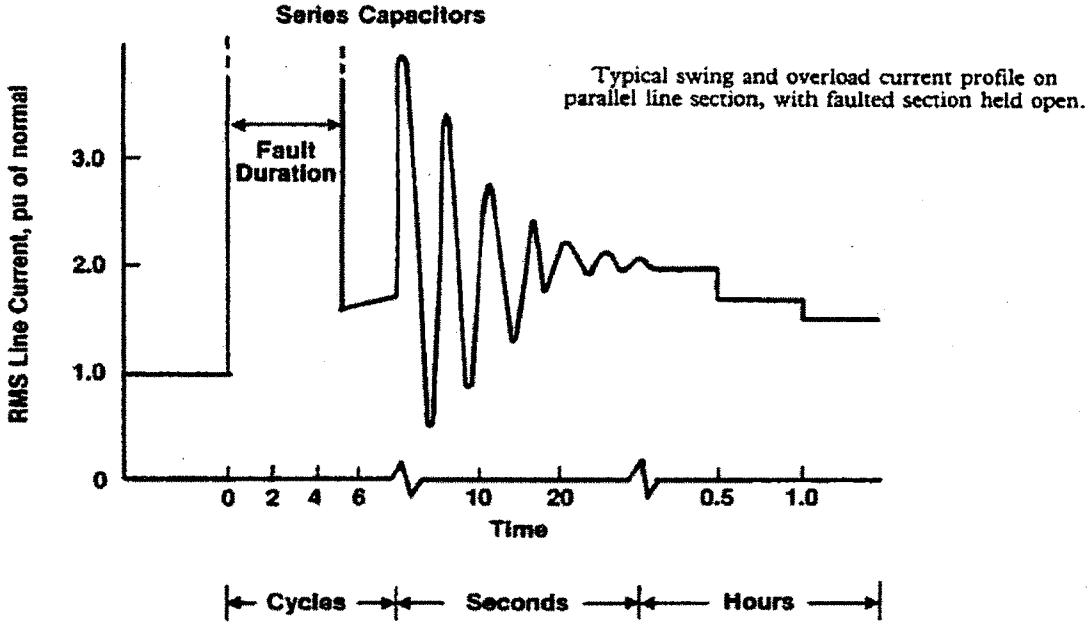


Fig.3.2 System Transients during Faults

Due to the limitations in the ability to build large voltage gaps, banks which are protected by gaps are made up of multiple series/parallel segments. The sequential insertion of these segments can result in increased reinsertion transients and non-simultaneous gap flashing.

3.2.2 Metal Oxide Varistors (MOV)

The 1980s have marked the widespread use of metal oxide varistors for transient over voltage protection for series capacitors. Figure 3.3 is a simplified schematic diagram for this system. The MOV is connected directly across the capacitor with no intervening reactor or gap. The exceptional nonlinearity of the MOV results in no conduction through the MOV during normal system conditions. On the occurrence of a fault the current through the capacitor increases, giving rise to an increase in the capacitor voltage. The MOV begins to conduct when this voltage approaches the protective level and acts to clamp the voltage to the protective level. This clamping action occurs each half cycle with alternate conduction between the capacitor and the MOV as shown in Figure 3.4. On removal of the fault, the MOV will cease to conduct except for the occasional peak voltage of the post fault transient. The energy duty of this transient is typically small in comparison with the energy requirements associated with the fault currents.

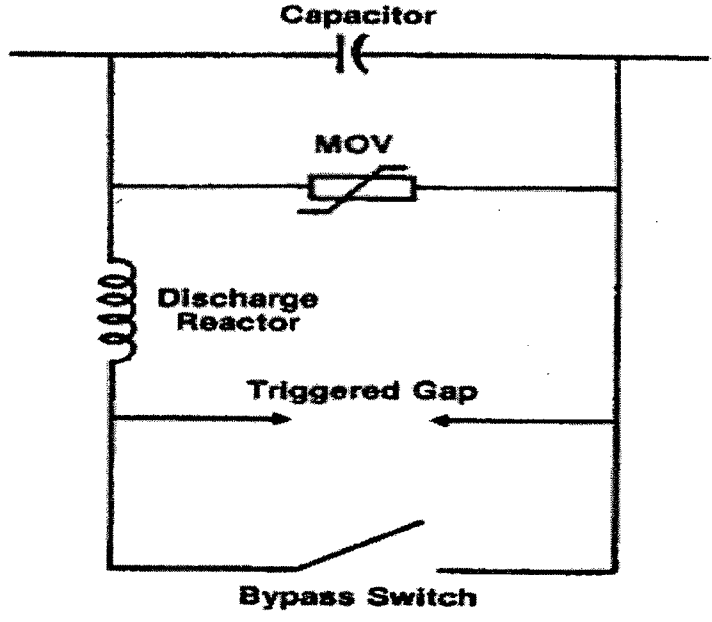


Fig.3.3 Simplified arrangement of MOV

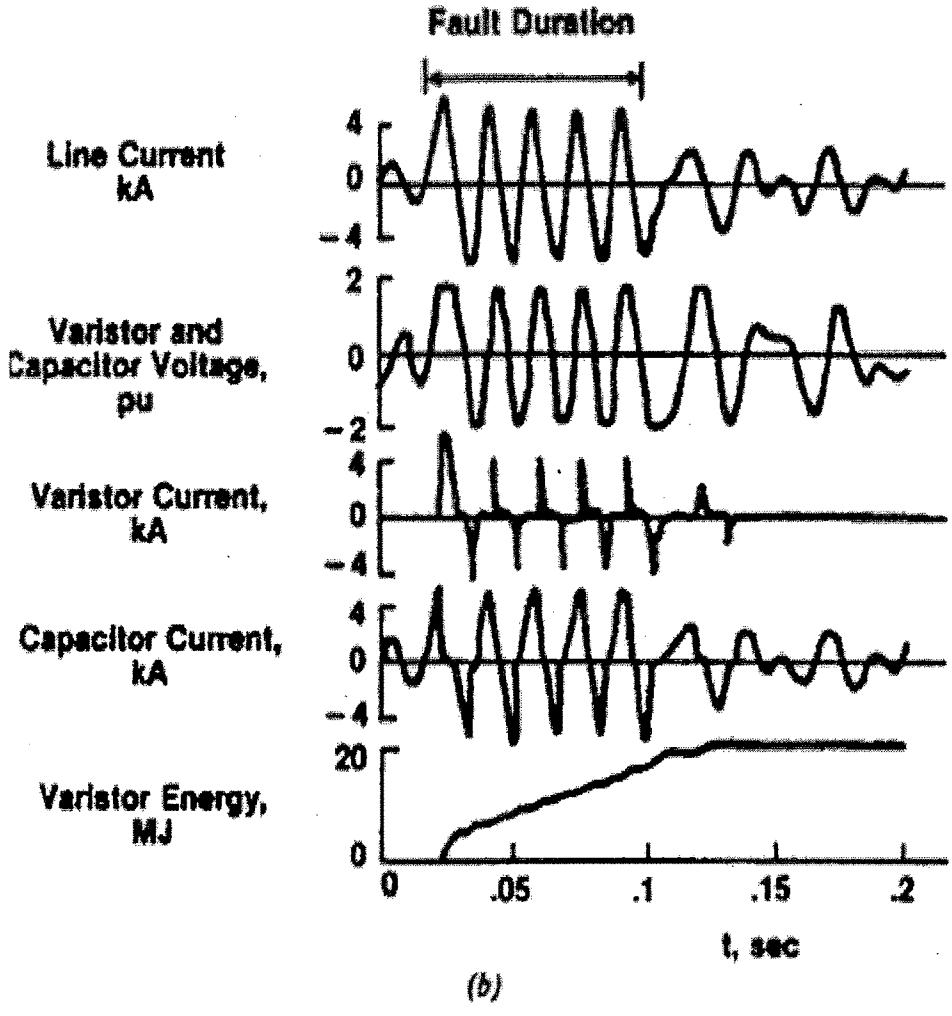


Fig.3.4 The clamping action due to MOV

The MOV has stable and defined voltage and energy characteristics upon which the MOV ratings are established for each application. Since the MOV has eliminated concerns for the recovery voltage withstand of the gap, protective levels have been reduced to a range of 2.0 to 2.5 times normal voltage. The protective level is usually specified to be above the system swings although it may conduct on some of the initial post fault transients as mentioned above. The specification of a MOV requires the definition of the system conditions for which the energy rating of the MOV will be established. The MOV is usually required to have sufficient energy capability to ride through worst case external fault scenarios thus allowing the capacitor to remain in service at the time it is most needed. A parallel gap is provided to protect the MOV when its energy rating has been reached. This gap is triggered by protection circuits which monitor the energy duty of the MOV. When the energy rating is reached the gap is fired.

For internal line faults, there are a number of approaches available for the specification of the energy rating of the varistor. Obviously, the energy available is a function of the location of the capacitor bank and this will affect the type of system selected. The varistor protection circuit monitors the MOV and triggers the gap upon detection of a high level of current flow or high rate of rise of energy. Depending upon fault severity and fault initiation angle, the detection and triggering circuits bypasses the MOV in as little as 2 ms after fault initiation. However, bypassing may not occur if the fault is not severe enough to cause pickup of these circuits.

3.3 The Proposed Scheme

The following discussion closely reveals the possibilities of overreach of a distance relay during a fault on the transmission line.

The faults associated with series compensated transmission line, irrespective of their type (i.e. l-g, l-l-g, l-l, l-l-l-g,...open conductor and cross country), location (i.e. start, middle, or end of line), fault resistance, fault inception angle, compensation level, source impedance and relative source angles at the two ends of the line can be categorized under categories of low, medium and high current faults based on fault current magnitudes.

In the event of low current faults the voltage drop across series capacitor will not be up to MOV's protection level and hence during these faults the complete capacitor remains there in series with the line and as such the traditional distance function reach setting can always be done considering the percentage series compensation, the relay may marginally overreach or may not over reach at all for these faults.

The medium current faults are faults with the current magnitudes sufficient enough to raise the voltage across series capacitors up to MOV's protection level but not sufficient enough to raise the energy levels of MOV's to its protection level. Hence during these conditions the parallel combination of the capacitor and MOV will be in series with the line and total fault current will be partly shared by capacitor and partly by MOV. This is the case where the capacitor is trying to increase the fault current while the nonlinear resistor of MOV is trying to reduce the fault current. Due to this the dynamic characteristic of the distance relay experiences a continuous variation in the

measured impedance of the line and may result in to faulty decision making and will eventually overreach.

The conduction of MOVs during such faults and the clamping action due to them introduces a bulk amount of harmonics (i.e.3^{rd},5^{th},7^{th} ,9^{th}...) in the post fault signals. Hence when the MOV does operate, it creates a typical frequency signature which can be positively identified. Hence, when there is an operation of MOV one can conclude the presence of series capacitor in fault loop since only sufficient fault current would cause MOV to operate and clip the voltage waveforms seen by relay. Thus the detection of specific frequency signature full of harmonics gives relaying engineer the useful information about the presence of capacitor and MOV in the fault loop. The same concept will be utilized in order to develop the proposed scheme.

The high current faults are the faults with such a large magnitudes of the fault currents that not only quickly brings MOV in to the fault loop in order to protect the series capacitors but will raise the energy levels across MOV's very high enough to operate the bypass gap in order to protect the MOV who is infact protecting series capacitors (refer Figure 3.3) and hence within very short time period of say 2 to 5 millisecond the complete arrangement of parallel combination of MOV and series capacitor will be bye passed. The protective scheme with sufficient stability criteria (operating / decision making algorithms based on post fault analysis of half cycle or more time), will not likely to overreach for these faults.

The discussion can be concluded as there is an acute need of the protective scheme to be worked out for the case of medium current faults in order to prevent overreach of distance relays when they are adopted for protection of series compensated lines. (While the low current faults and high current faults will be taken care largely by properly set and stabilized distance protection scheme and there are very less chances of overreach/mal-operation of the protective scheme for such cases.)

Considering the above discussion, "A Current Controlled Harmonic Index based Protection Scheme" is proposed further in the chapter. Figure 3.5 presents the flow chart for the proposed scheme.

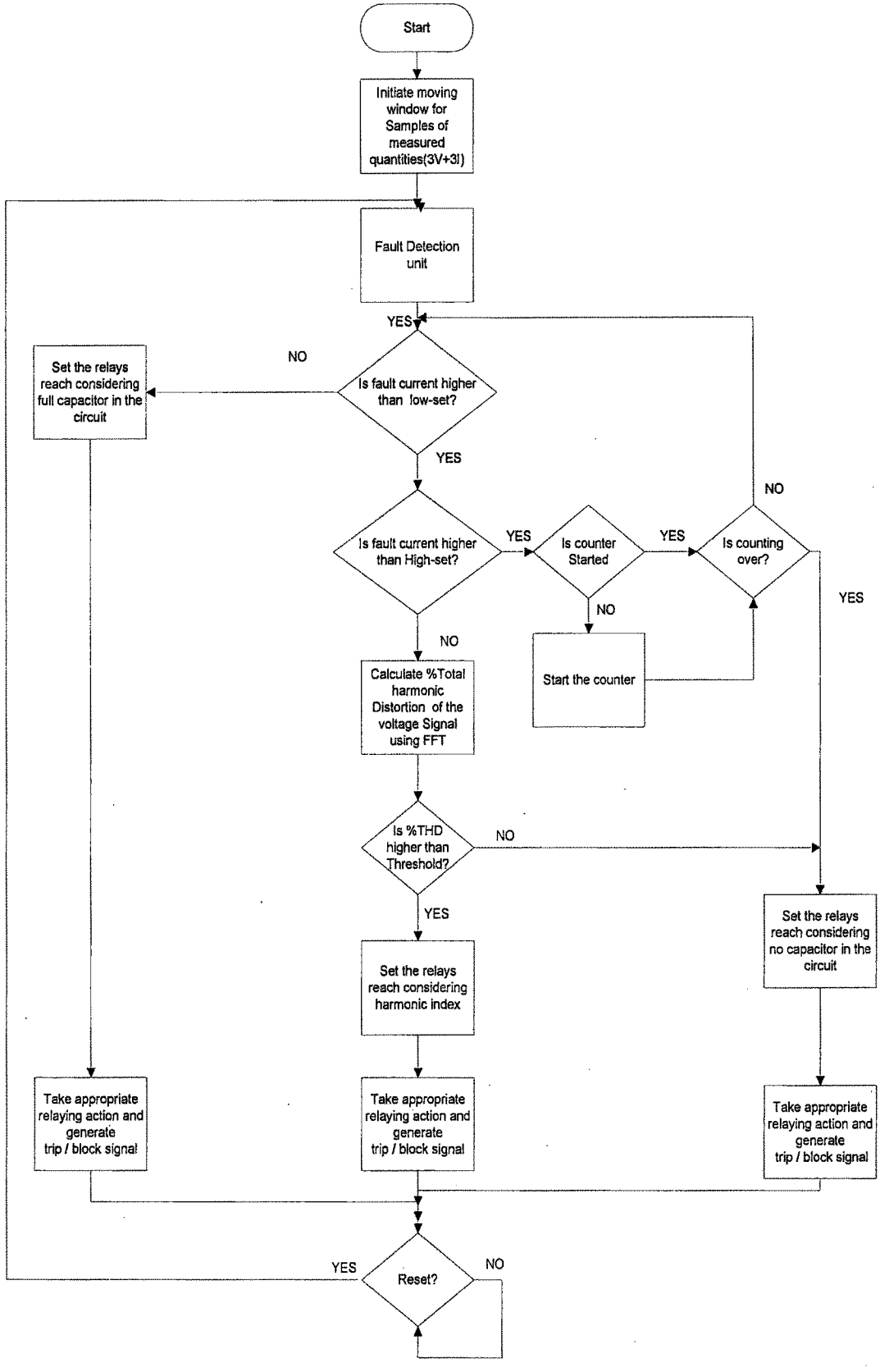


Fig.3.5 Flow Chart of Proposed Scheme

3.4 Working of the Scheme

The following section will briefly discuss the working of the proposed scheme referred in the form of flow chart in Figure 3.5;

1. The relay will initiate a moving window of sampled line currents and voltages at the relaying point.

2. Fault detection unit will detect a fault based on the current magnitude(i.e. when the sampled current magnitude in any line exceeds the normal set value, an simple over current starter unit may also be used for this purpose) and check for the proper direction of the fault current in order to prevent reverse reach.(normally MHO units with stepped characteristic are used and they are having inherently the directional sensitivity)

3. On confirmation of the fault in forward direction the scheme will check for the magnitude of fault current if it is higher than low-set or not. If the fault current is not higher than low set then relay will calculate its reach setting considering the full capacitor in the fault loop and then will take relaying action by calculating the present impedance using the latest samples of voltage and current.(i.e. will block if calculated impedance is more than the so set adaptive reach setting and will initiate a trip action if the calculated impedance is lower than so set adaptive reach setting)

4. If the fault current is higher than low set then relay will check for whether it is higher than high-set or not. If fault current is higher than high-set then relay will initiate a counter which counts for successive high-set sampled window events for the period of ¼ of cycle (normally for high currents the MOV protection operates within 2 to 5 cycles)and if still the current is higher than high-set then by this time the MOV protection have by-passed the complete capacitor-MOV setup from the line (Due to thermal limits of the MOV) and relay will now calculate its reach setting considering no capacitor in the circuit and compare it with the measured impedance calculated from the latest samples of voltage and current and will take appropriate relaying decision as depicted in flow chart. (i.e.

will block the operation of the relay if calculated impedance is more than the so set reach setting and will initiate a trip action if the calculated impedance is lower than so set reach setting)

5. In the event of fault current is higher than low-set but lower than high-set the relay will calculate the % total harmonic distortion (%THD)(utilizing harmonic present in post fault voltage window at relaying point) by using full cycle FFT. Further based on harmonic index calculated the relay will calculate its reach (Higher the harmonic index lower the capacitor present in fault loop and vice versa) and compare it with measured impedance calculated from latest samples of voltage and current and will take appropriate relaying decision as shown in flow chart . (i.e. will block if calculated impedance is more than the so set reach setting and will initiate a trip action if the calculated impedance is lower than so set reach setting)

3.5 Simulation Studies

In order to evaluate the robustness of the proposed scheme extensive simulation studies are carried out on a two terminal transmission line model using MATLAB with a variable series compensation placed at the middle of the line. The transient fault studies are carried out using the well-known MATLAB (SIMPOWERSYSTEMS BLOCKSET) program. The performance of the proposed technique is analyzed for a large test data set (28,800) considering a wide variation in system condition along with a change in the source impedance. The simulation studies carried out in this work is based on the ideas, methods and parameters used for simulation studies in the work reported in [67].

3.5.1 Simulation Model

The model used for simulation studies in MATLAB is shown in Figure 3.6.The transmission line has been represented using the distributed parameters line. The power system comprises of two sources, series capacitor (located at midpoint of the line) and its associated components. The system parameters used has been given in Table 3.1. Over-voltage protection of series capacitor is provided by MOV and parallel power gap. The MOV is protected by C.B. operation against its energy dissipation capacity. The Series capacitor is designed to vary its compensation between 25% minimum to a maximum of 75%.

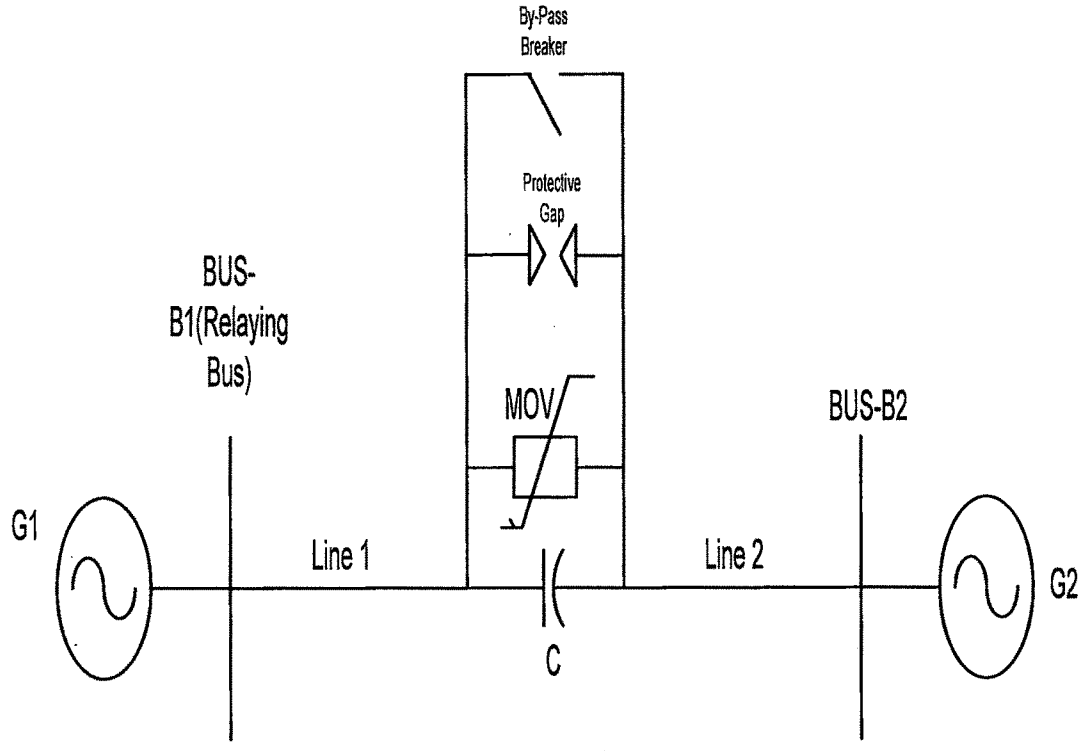


Fig.3.6 Model used for simulation studies

Table 3.1 System parameters

Line Length	300 KM
Voltage	400 KV
Compensation degree	25% to 75%
Location of Series Capacitors	150 KM
Positive Sequence Impedance of Line	8.25 + j94.5 Ω
Zero Sequence Impedance of Line	82.5 + j308 Ω
Positive Sequence Capacitance of Line	13 nF/KM
Zero Sequence Capacitance of Line	8.5 nF/KM
System Frequency	50 HZ
Positive Sequence Impedance of the G1-G2	1.31 + j15 Ω
Zero Sequence Impedance of the G1-G2	2.33 + j 26.6 Ω

To test the suggested scheme the simulation studies have been carried out under wide variation of load angle, fault inception angle, fault resistance and fault locations. The different values of fault type, load angle, fault inception angle, fault resistance and fault positions (before and after the Series Capacitor), which have been chosen for this study, are as follows:

(i) Fault Type: a-g, b-g, c-g, a-b, b-c, c-a, a-b-g, b-c-g, c-a-g, a-b-c/a-b-c-g

(ii) Load angle: 10°, 20°, and 30°

(iii)Fault inception angle: 0°, 45°, 80°, 115°

(iv) Fault resistance: 0.01Ω, 1Ω, 50Ω, 100 Ω

(v) Fault Locations: 20% & 40% (Before the Series Capacitor)
60% & 80% (after the Series Capacitor)

Thus, 10×3×4×4×4 =1920 combinations of above mentioned parameters have been selected for a single compensation level (Xc) with a fixed value of source impedance ZG1 and ZG2 at two ends of the transmission line. A total of 15different cases have been generated by varying the said two parameters. Hence, 1920×15=28800 test cases are simulated. Table 3.2 shows different values of parameters used in generation of 15 cases.

Table 3.2 Range of Parameter Variation for Test Data Generation

Case No	ZG1 (%)	ZG2 (%)	Xc (%)
1-3	100	100	25,50,75
4-6	100	75	25,50,75
7-9	100	125	25,50,75
10-12	75	100	25,50,75
13-15	125	100	25,50,75

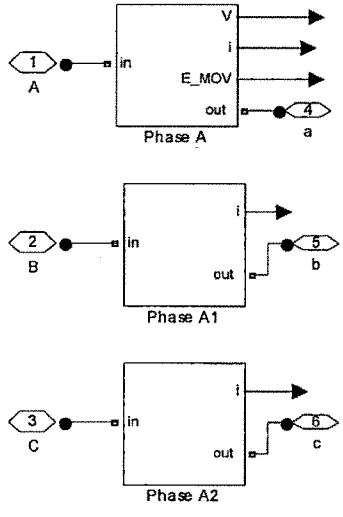
The performance of the proposed scheme has been checked for test cases so generated by simulation studies. It is to be noted that for each and every fault simulation study, simulation parameters as per Table 3.3 have been performed.

Table 3.3 Simulation Parameters

Simulation Time	0.1 Sec (Five Cycles)
Sampling Frequency	20 KHZ
Simulation Starts	T=0 Sec (0'th Sample)
Fault is Applied at	T=0.02 Sec (400'th Sample)
Fault is removed at	T=0.06 Sec (1200'th Sample)
Simulation Ends	T=0.1 Sec (2000'th Sample)

3.5.2 Series Capacitor Protection simulation Circuits

For the case of 50% line compensation the sample calculation of MOV parameters and Capacitor protection simulation circuit is shown in Figure 3.7 while Figure 3.8 shows the simulation circuit of Protection arrangement (Parallel gap) for MOV.



Three-phase series compensation module

Total line reactance in positive-sequence:
X1 = 94.5 ohms

Capacitance required for 50% compensation:

Required series capacitance:
Xc=0.5*94.5 = 47.25 ohms
or Cs= 67 uF

MOV protection level required to protect the capacitors
at 2.5 timesthe nominal capacitor voltage.
(The nominal capacitor voltage is taken at 2 kA rms line curent)

Uprot.= 2.5*2kA*47.25*sqrt(2)= 333 kV

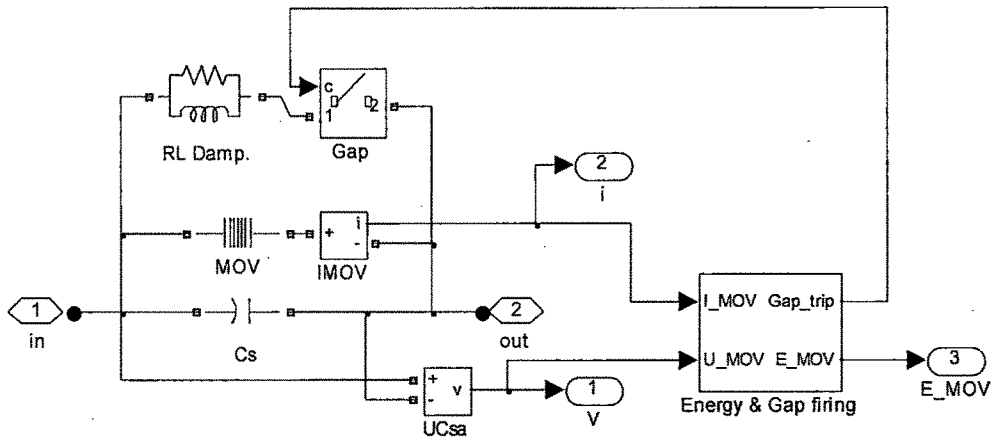


Fig.3.7 Sample calculation and Capacitor protection simulation

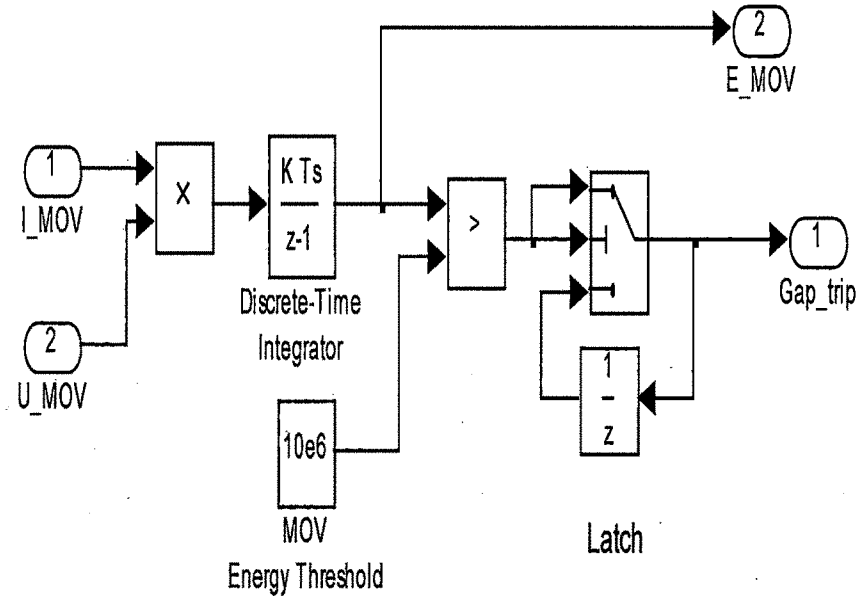


Fig.3.8 MOV Protection Simulation Circuit

It is evident from the sample calculations shown for the 50% line length compensation case that the MOV will start conducting and hence protecting the capacitor once the voltage across the capacitor rises above 333KV and that will be the case when the fault current magnitude hits 5KA level. Considering the same the decided thresholds for the scheme is;

I low-set: 5KA

I high-set: 30 KA

Harmonic Index = 1 (if % THD observed is more then 5% in post fault one cycle FFT of voltage signal at relaying point)

Next section will be demonstrating some case studies of fault simulations done considering the suggested scheme. The distance function with the suggested scheme is at Bus-B1.

3.5.3 Some case studies and related discussions

(1) Xc=50%, ZG1=100%, ZG2=100%, A-g Fault at 60KM from Bus-B1, Rf=1 Ω

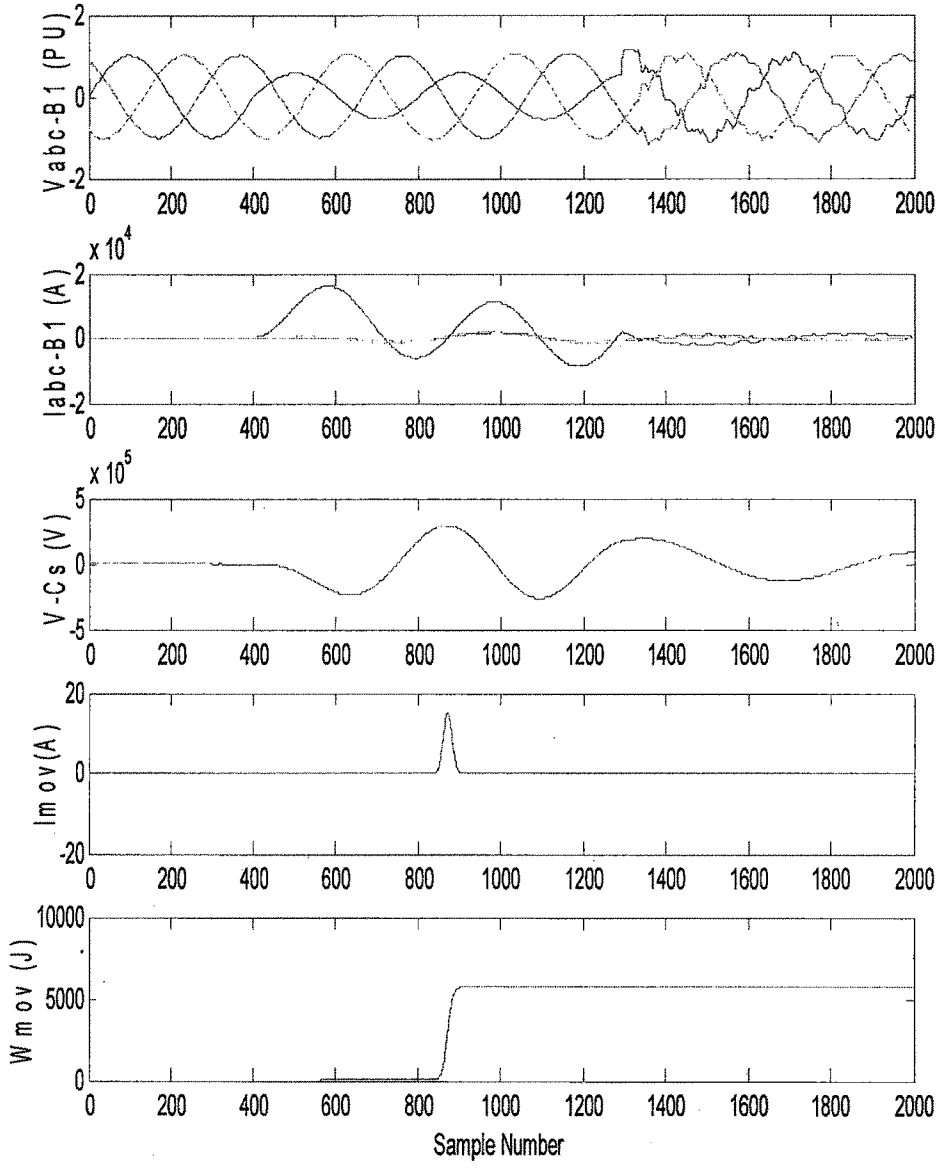


Fig.3.9 Plots for A-g Fault at 20% Line Length

(Vabc-B1: Three Phase Voltages Measured at bus B1,

Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,

Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.9) it's evident that the fault current in A-Phase exceeds I low-set and remains less than I high set and hence the scheme will look for the % THD (Harmonic Index) in the post fault relay voltage. The related FFT plot is shown in Figure 3.10.

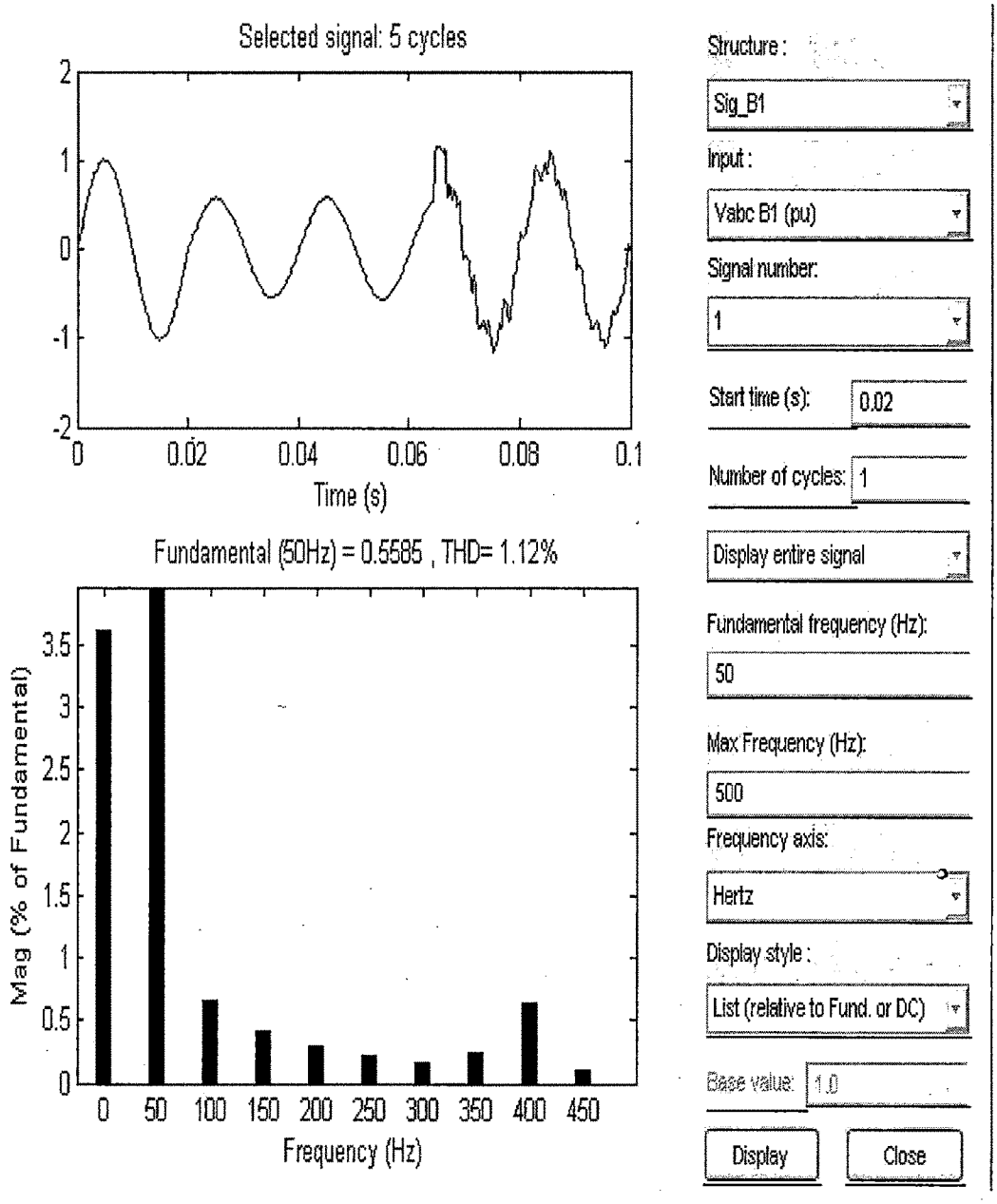


Fig.3.10 FFT Plots for A-g Fault at 20% Line Length

As the % THD is 1.12% only the proposed scheme concludes absence of the capacitor (which is true also) in the fault loop and takes further relaying decisions accordingly.

(2) Xc=50%, ZG1=100%, ZG2=100%, A-B-C-g Fault at 60 KM from Bus-B1, Rf=0.01 Ω

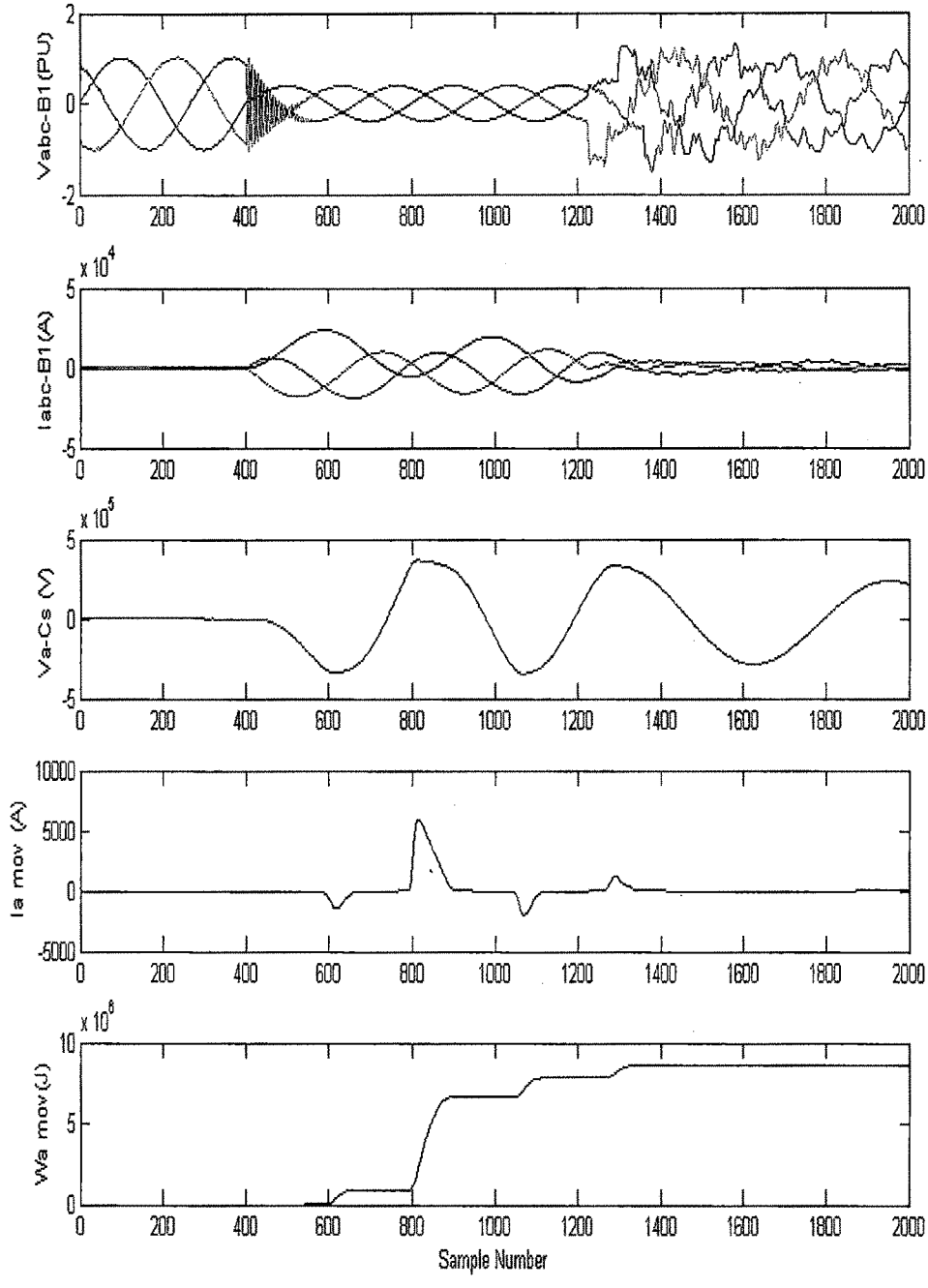


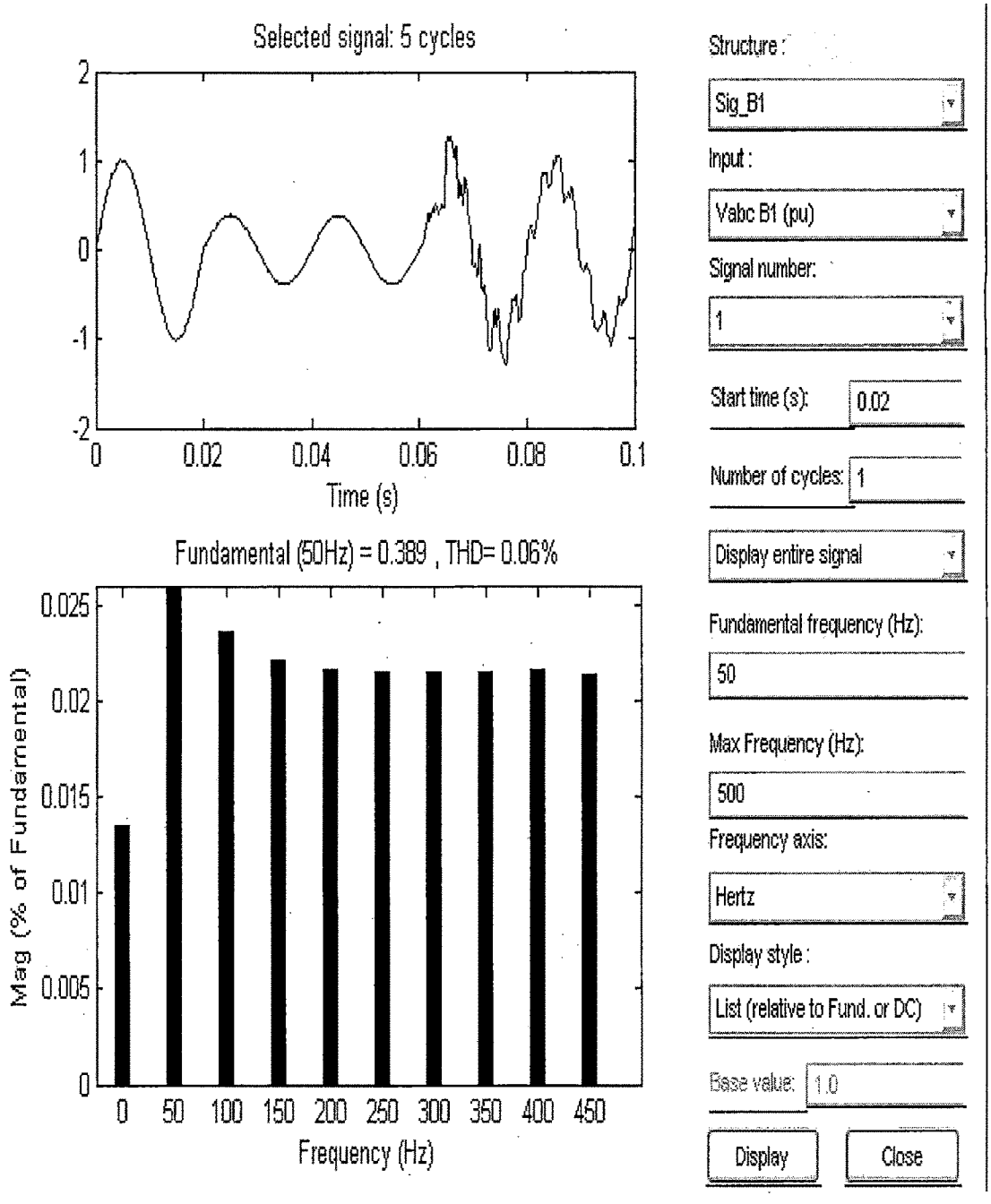
Fig.3.11 Plots for A-B-C-g Fault at 20% Line Length

(Vabc-B1: Three Phase Voltages Measured at bus B1,

Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,

Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.11) it's evident that the fault current in All Phases exceeds I low-set and remains less than I high-set and hence the scheme will look for the % THD (Harmonic Index) in the post fault relay voltage. The related FFT plot is shown in Figure 3.12.



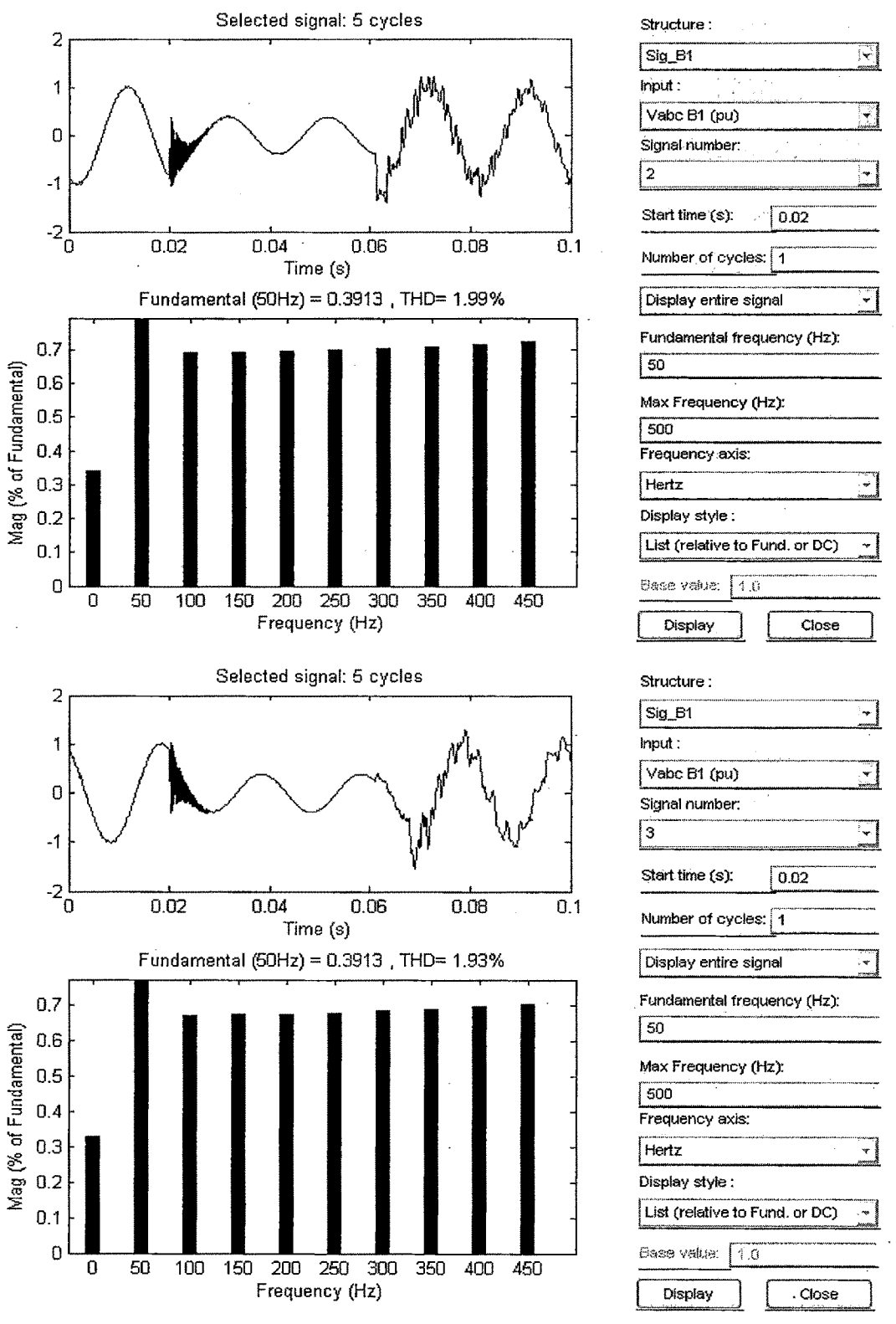


Fig.3.12 FFT Plots for A-B-C-g Fault at 20% Line Length

As the % THD is lower than set threshold in all the phases the proposed scheme concludes absence of the capacitor (which is true also) in the fault loop and takes further relaying decisions accordingly.

(3) Xc=50%, ZG1=100%, ZG2=100%,A-B-C-g Fault at 120 KM from Bus-B1, Rf=50 Ω

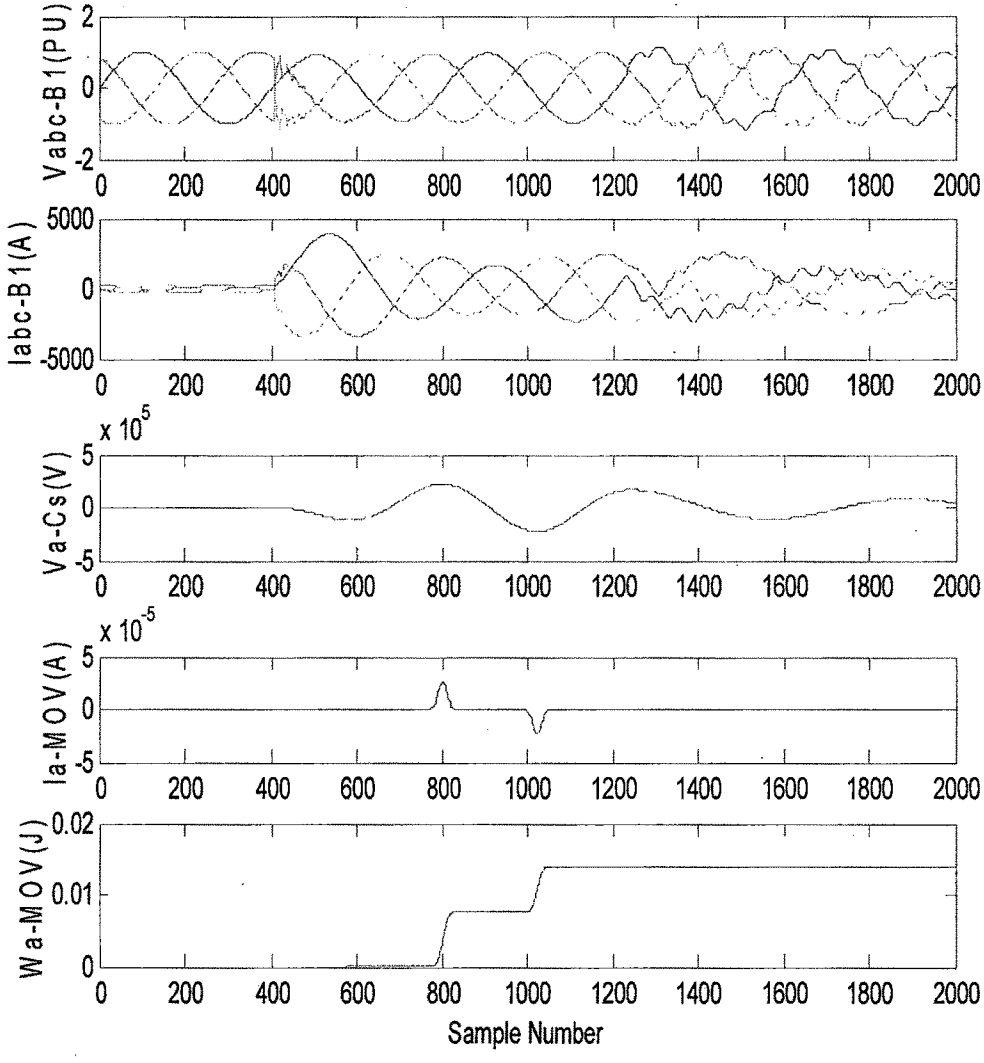


Fig.3.13 Plots for A-B-C-g Fault at 40% Line Length

(Vabc-B1: Three Phase Voltages Measured at bus B1,

Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,

Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.13) its evident that the fault current in All Phases remains lower than I low-set and hence the scheme will not look for the % THD (Harmonic Index) in the post fault relay voltage and scheme does relay reach setting considering presence of full capacitor in line irrespective of its presence in fault loop and takes further relaying decisions accordingly.

(4) Xc=50%, ZG1=100%, ZG2=100%, A-B-g Fault at 150 KM (Before Cs-MOV Unit) from Bus-B1, Rf=0.01 Ω

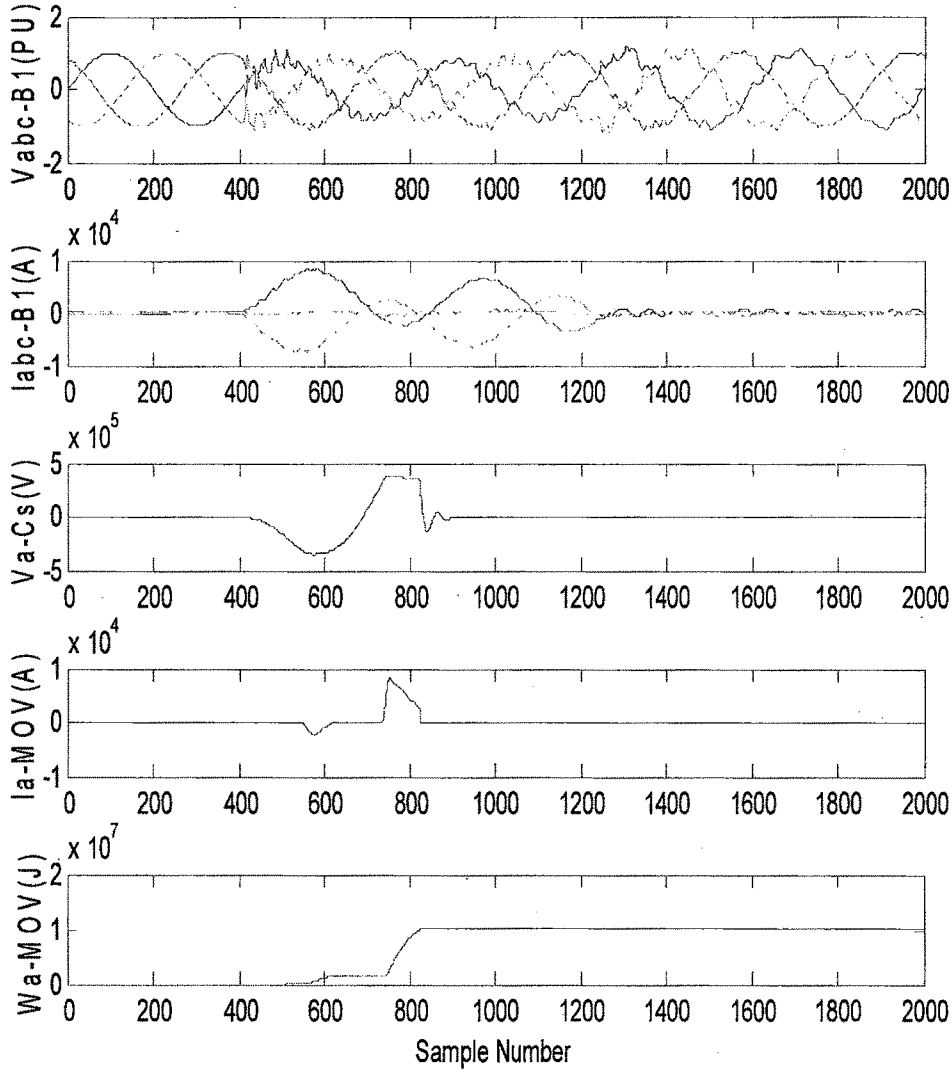


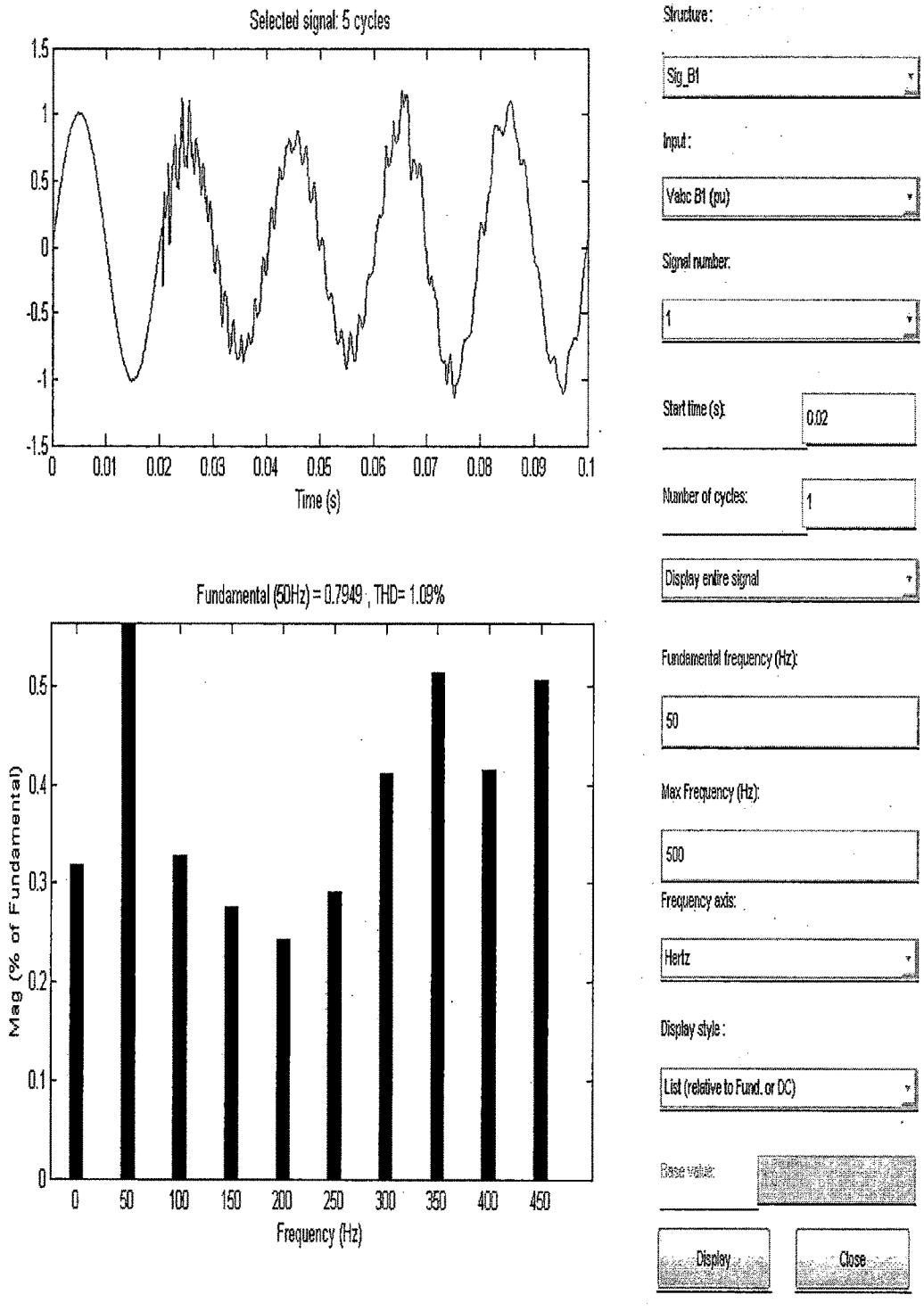
Fig.3.14 Plots for A-B-g Fault at 50% Line Length

(Vabc-B1: Three Phase Voltages Measured at bus B1,

Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,

Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.14) it's evident that the fault current in Phases A, B exceeds I low-set and remains less than I high-set and hence the scheme will look for the % THD (Harmonic Index) in the post fault relay voltage. The related FFT plot is shown in Figure 3.15.



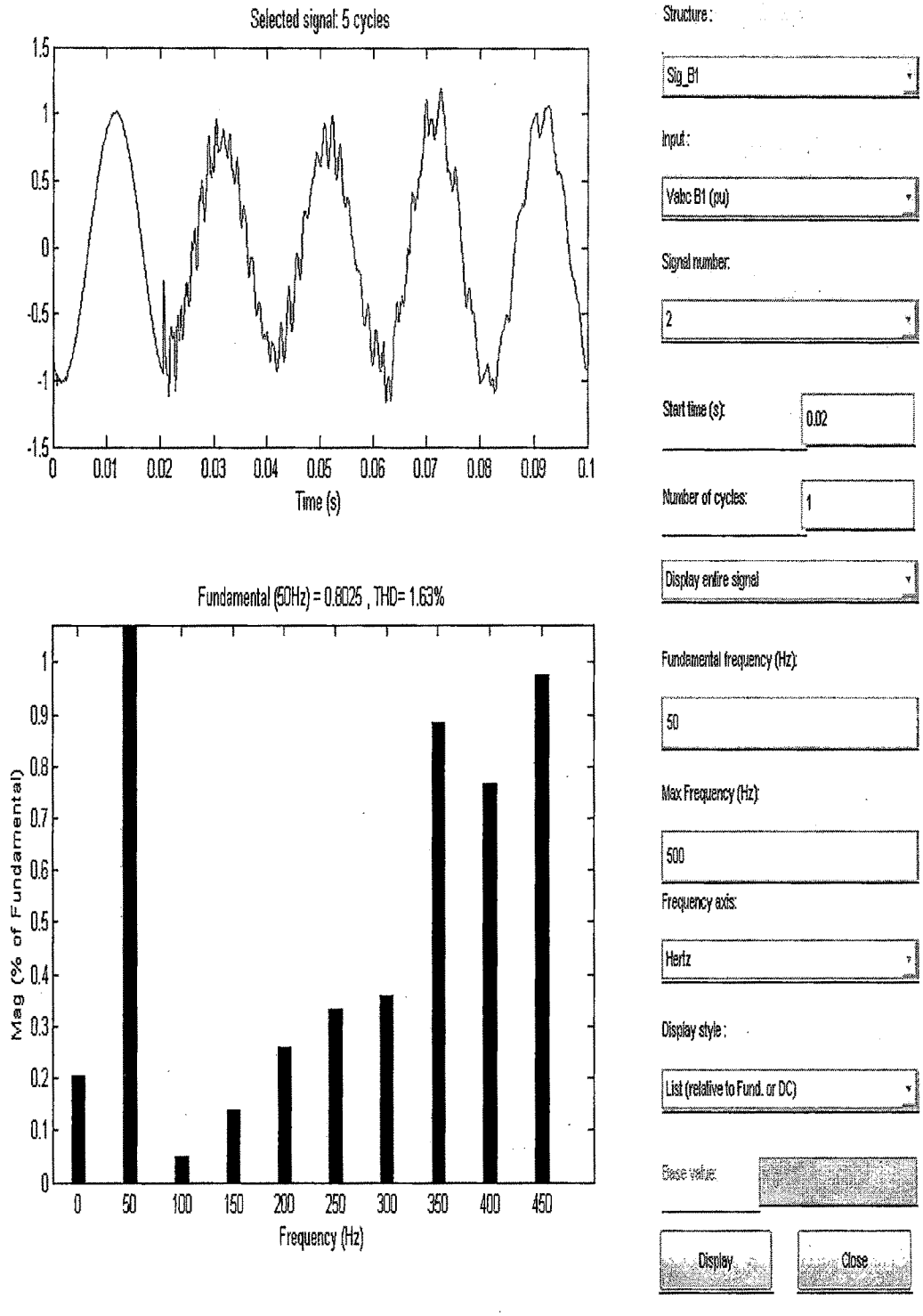


Fig.3.15 FFT Plots for A-B-g Fault at 50% Line Length

As the % THD is lower than set threshold in Phase A and Phase B the proposed scheme concludes absence of the capacitor (which is true also) in the fault loop and takes further relaying decisions accordingly.

(5) Xc=50%, ZG1=100%, ZG2=100%, A-B-g Fault at 150 KM (After Cs-MOV Unit) from Bus-B1, Rf=0.01 Ω

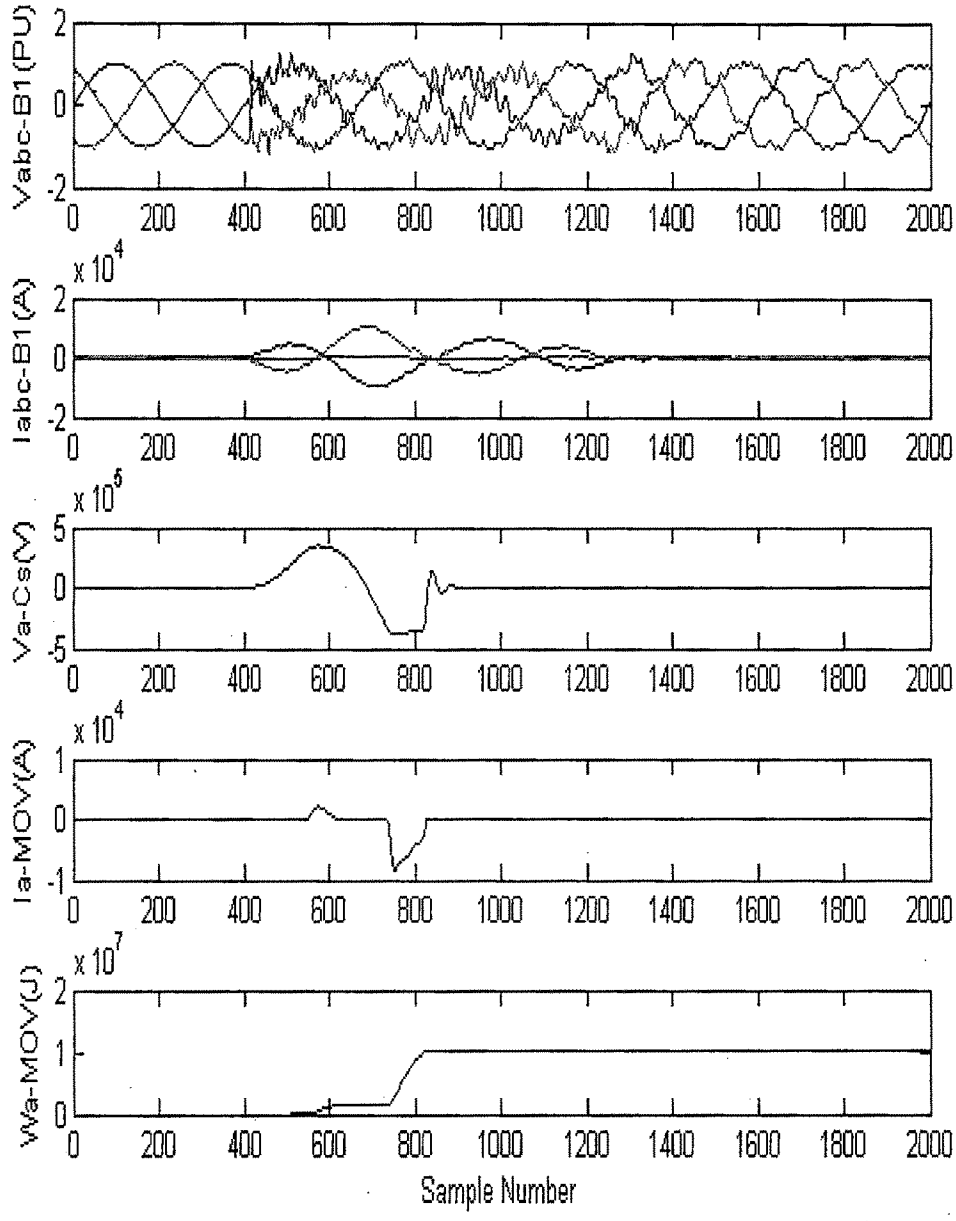
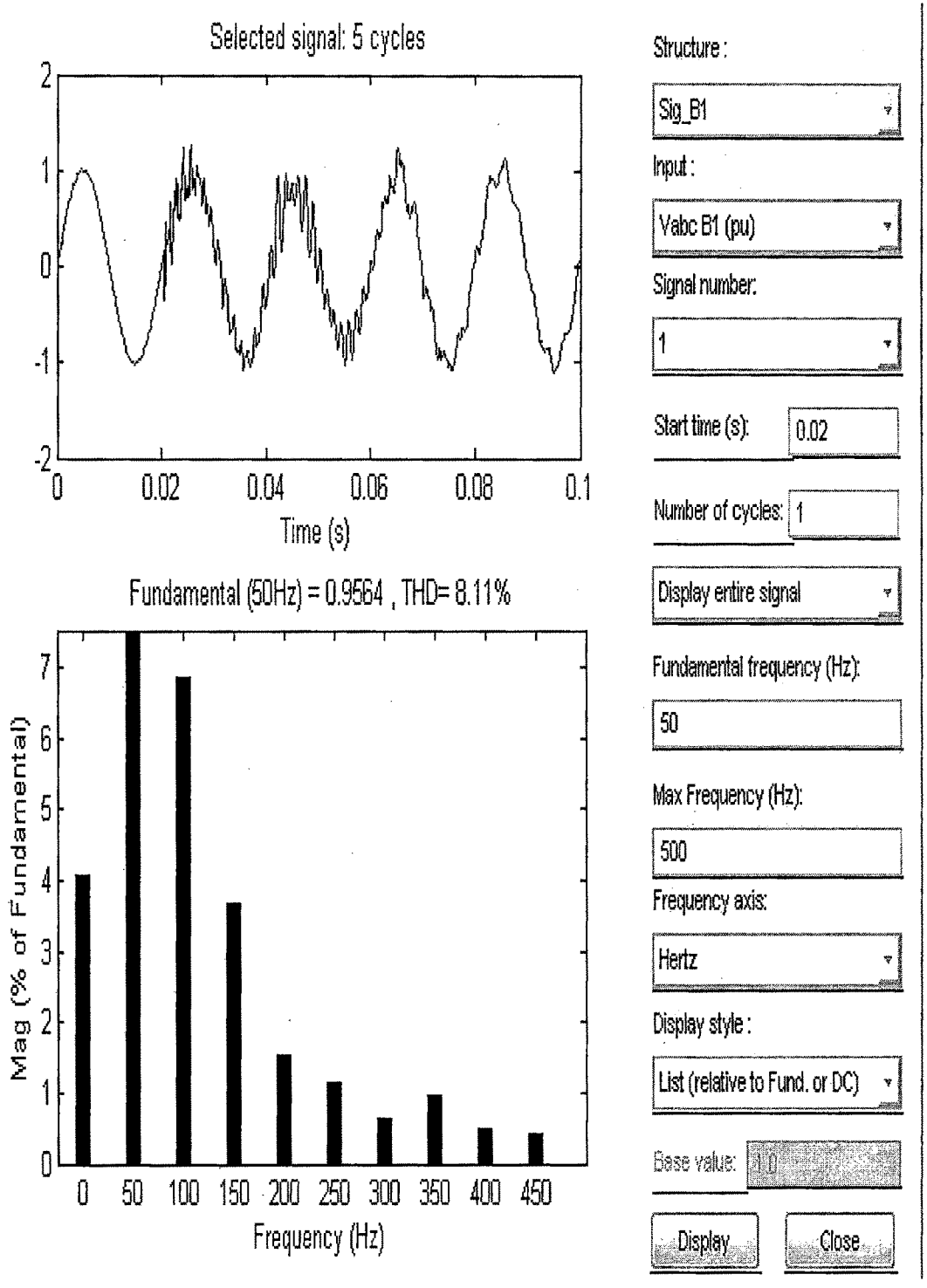


Fig.3.16 Plots for A-B-g Fault at 50% Line Length
(Vabc-B1: Three Phase Voltages Measured at bus B1,
Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,
Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.16) it's evident that the fault current in Phases A, B exceeds I low-set and remains less than I high-set and hence the scheme will look for the % THD (Harmonic Index) in the post fault relay voltage. The related FFT plot is shown in Figure 3.17.



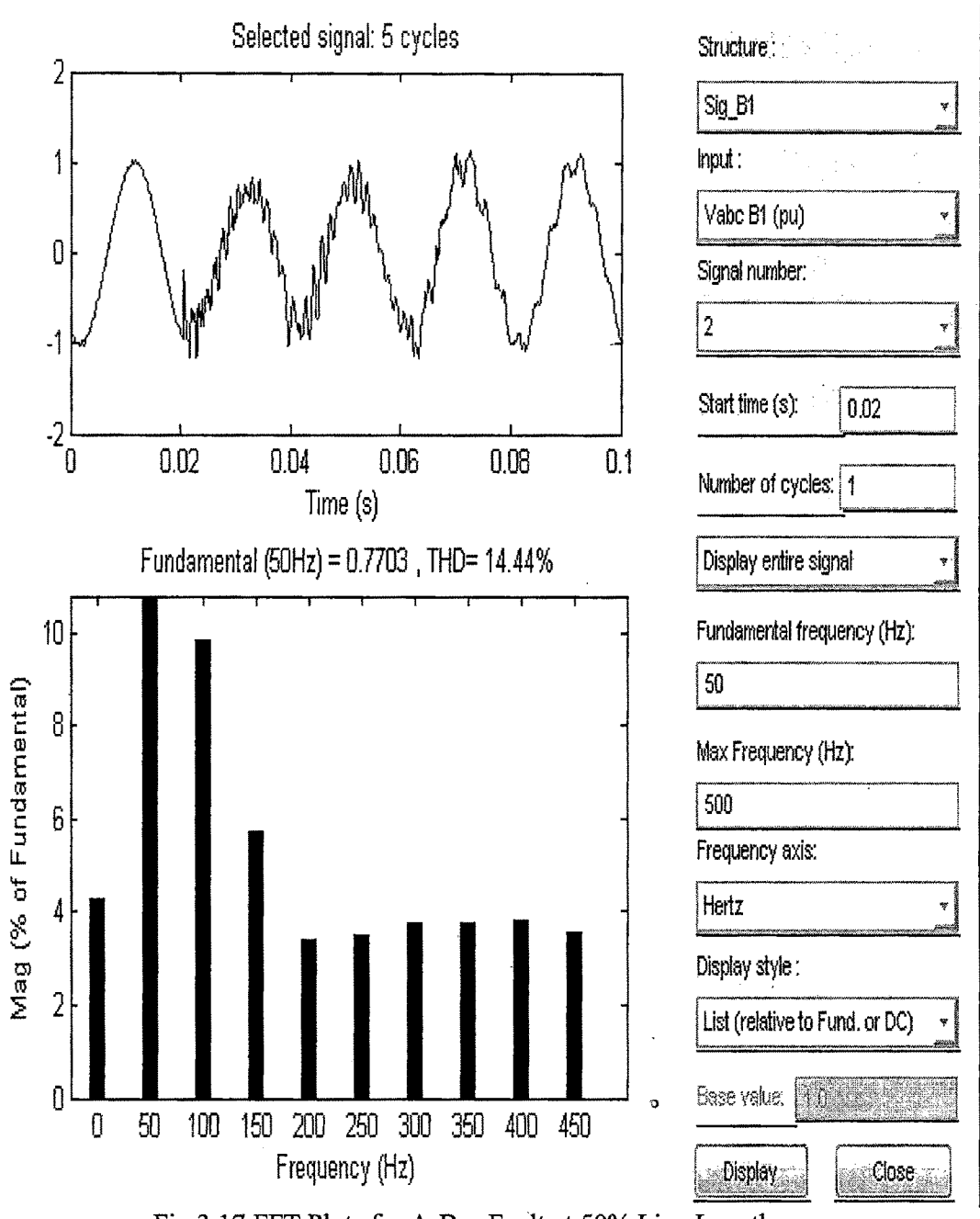


Fig.3.17 FFT Plots for A-B-g Fault at 50% Line Length

As the % THD is higher than set threshold in Phase A and Phase B the proposed scheme concludes presence of the capacitor (which is true also) in the fault loop and takes further relaying decisions accordingly. Also, it is observed that (Figure 3.16) MOV takes only 15 ms of time to reach its protection energy level after starting conduction and after that practically no capacitor is present in fault loop. (Also during conduction stage MOV starts conducting total fault current practically bye passing capacitor from fault loop measurements during the negative half of its conduction)

(6) Xc=50%, ZG1=100%, ZG2=100%, A-g Fault at 150 KM (After Cs-MOV Unit) from Bus-B1, Rf=50 Ω

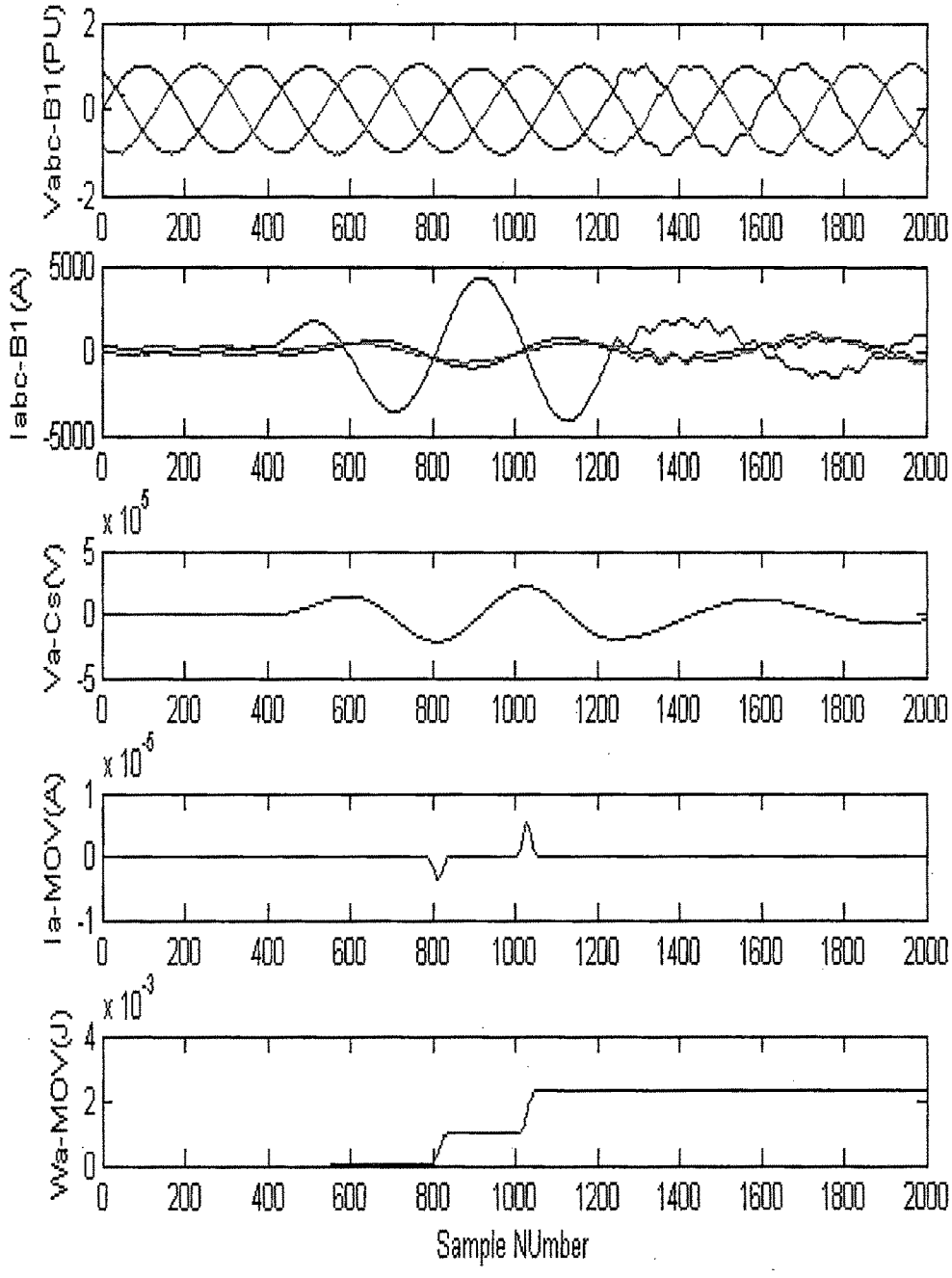


Fig.3.18 Plots for A-g Fault at 50% Line Length
(Vabc-B1: Three Phase Voltages Measured at bus B1,
Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,
Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.18) its evident that the fault current in A- Phase remains lower than I low set and hence the scheme will not look for the % THD (Harmonic Index) in the post fault relay voltage and scheme does relay reach setting considering presence of full capacitor in line irrespective of its presence in fault loop and takes further relaying decisions accordingly.

(7) Xc=50%, ZG1=100%, ZG2=100%, A-B Fault at 180 KM from Bus-B1, Rf=1 Ω

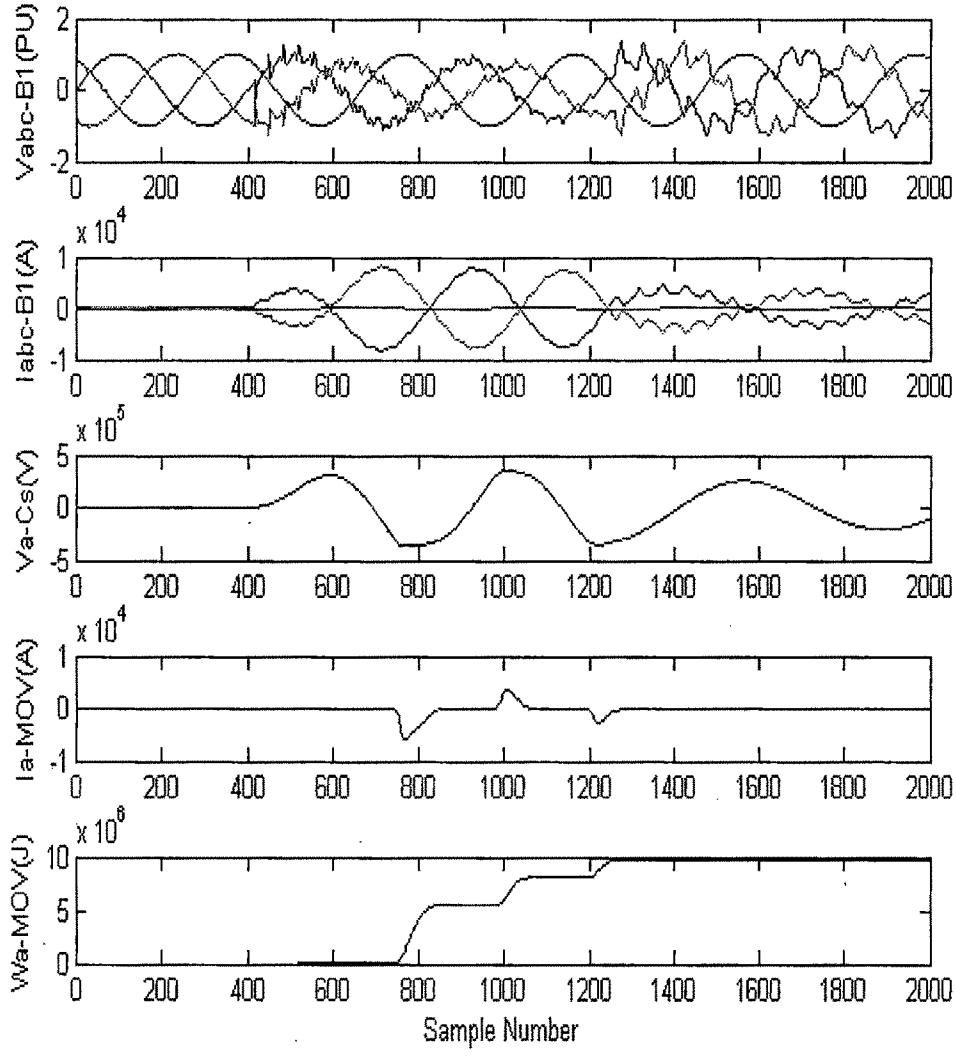
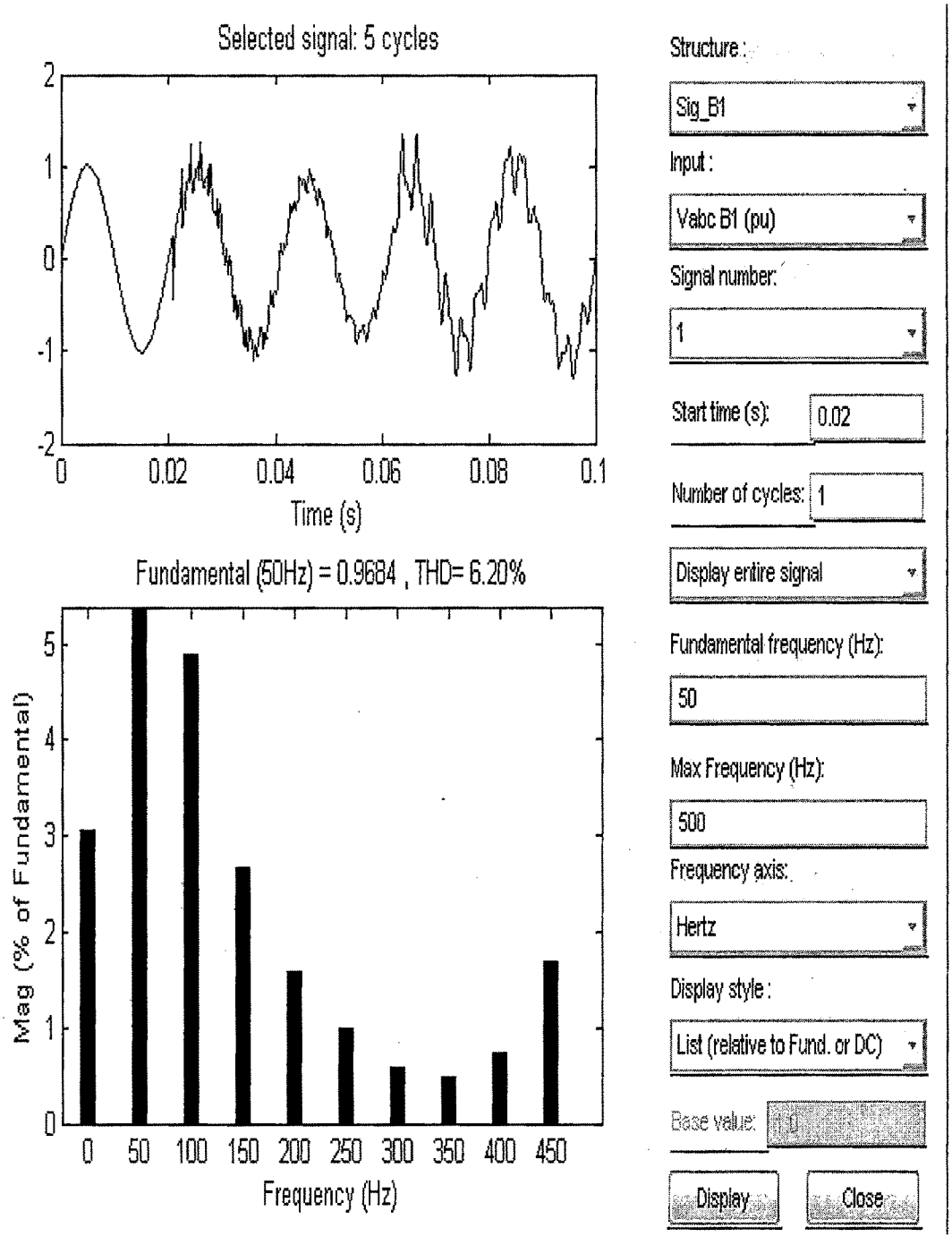


Fig.3.19 Plots for A-B Fault at 60% Line Length
(Vabc-B1: Three Phase Voltages Measured at bus B1,
Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,
Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.19) it's evident that the fault current in Phases A, B exceeds I low-set and remains less than I high-set and hence the scheme will look for the % THD (Harmonic Index) in the post fault relay voltage. The related FFT plot is shown in Figure 3.20.



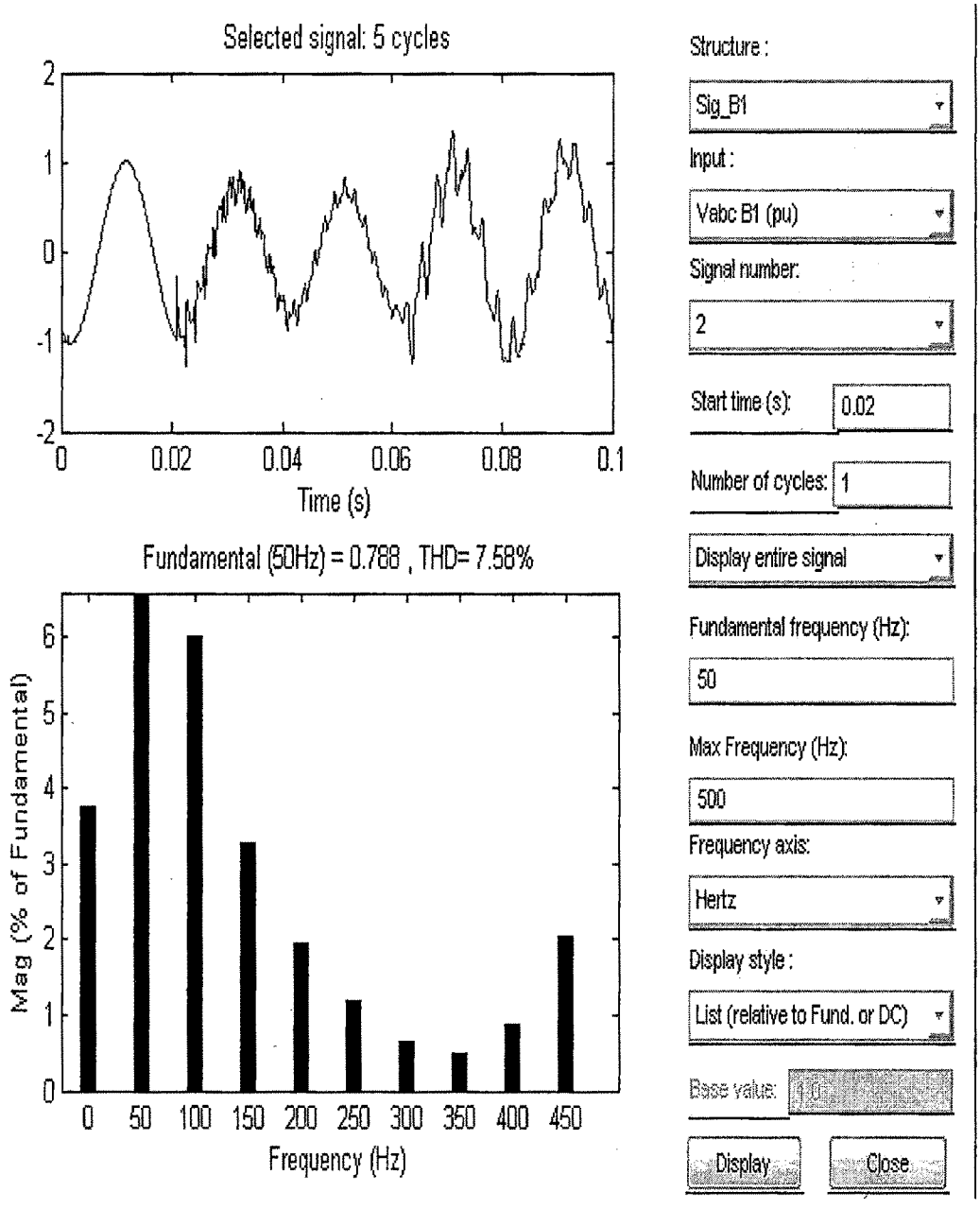


Fig.3.20 FFT Plots for A-B Fault at 60% Line Length

As the % THD is higher than set threshold in Phase A and Phase B the proposed scheme concludes presence of the capacitor (which is true also) in the fault loop and takes further relaying decisions accordingly. Also, it is observed that (Figure 3.19) MOV takes more then 20 ms of time to reach its protection energy level after starting conduction and after that practically no capacitor is present in fault loop. (Also during conduction stage MOV starts conducting only some amount of total fault current practically keeping parallel combination of Cs-MOV in the fault loop measurements.)

(8) Xc=50%, ZG1=100%, ZG2=100%, A-B-C Fault at 180 KM from Bus-B1, Rf=0.01 Ω

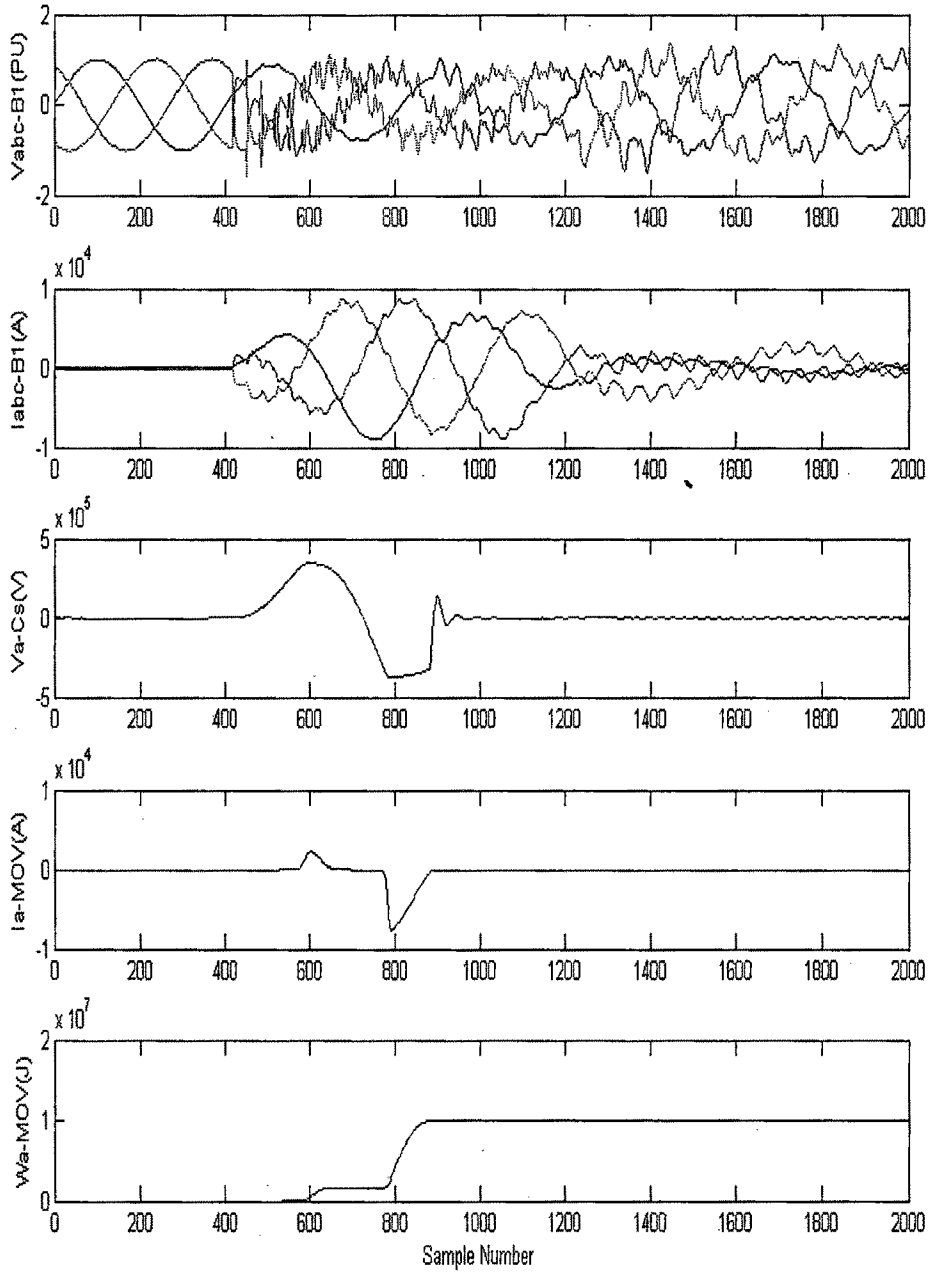
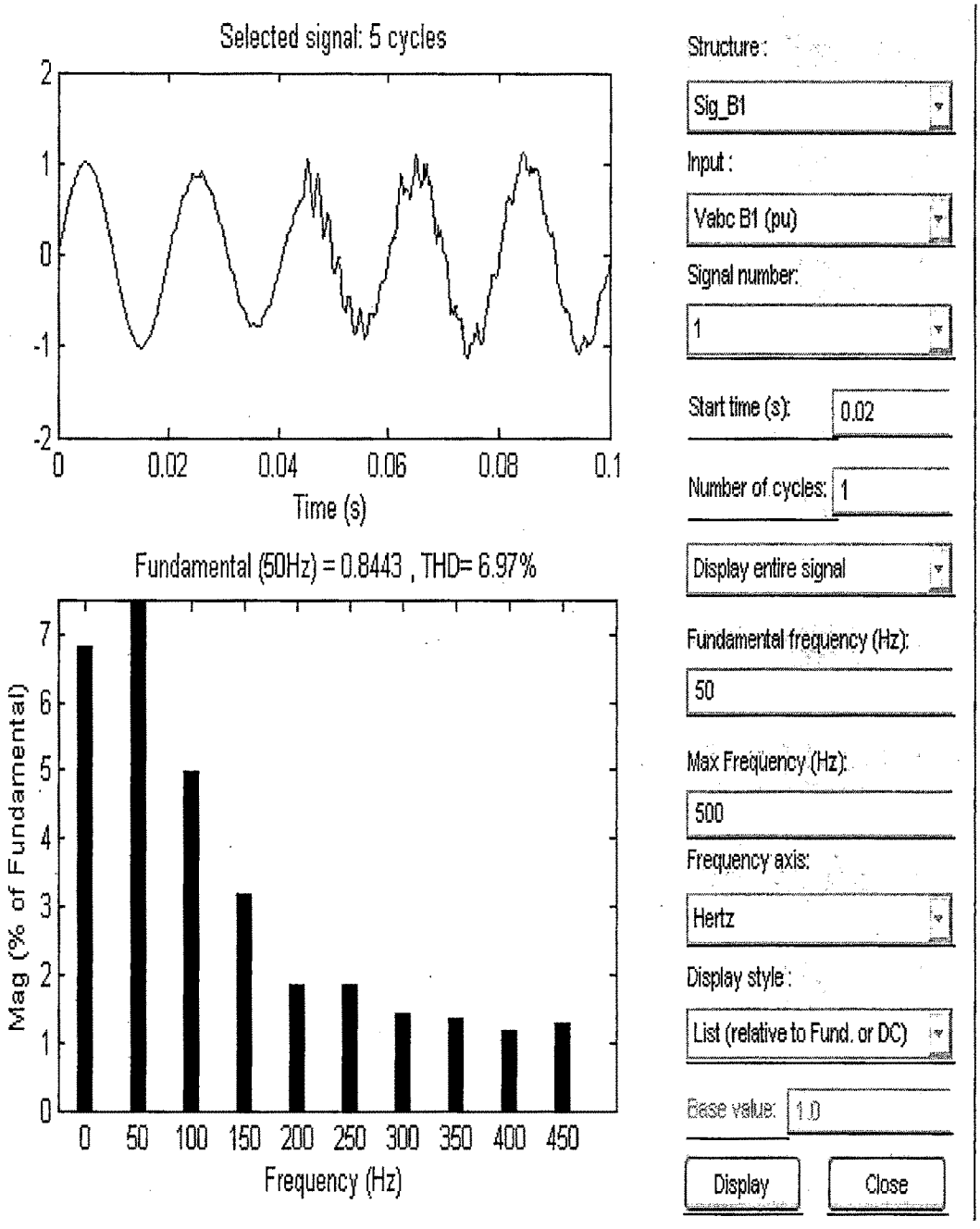


Fig.3.21 Plots for A-B-C Fault at 60% Line Length
(Vabc-B1: Three Phase Voltages Measured at bus B1,
Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,
Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.21) it's evident that the fault current in all the Phases exceeds I low-set and remains less than I high-set and hence the scheme will look for the % THD (Harmonic Index) in the post fault relay point voltage. The related FFT plot is shown in Figure 3.22.



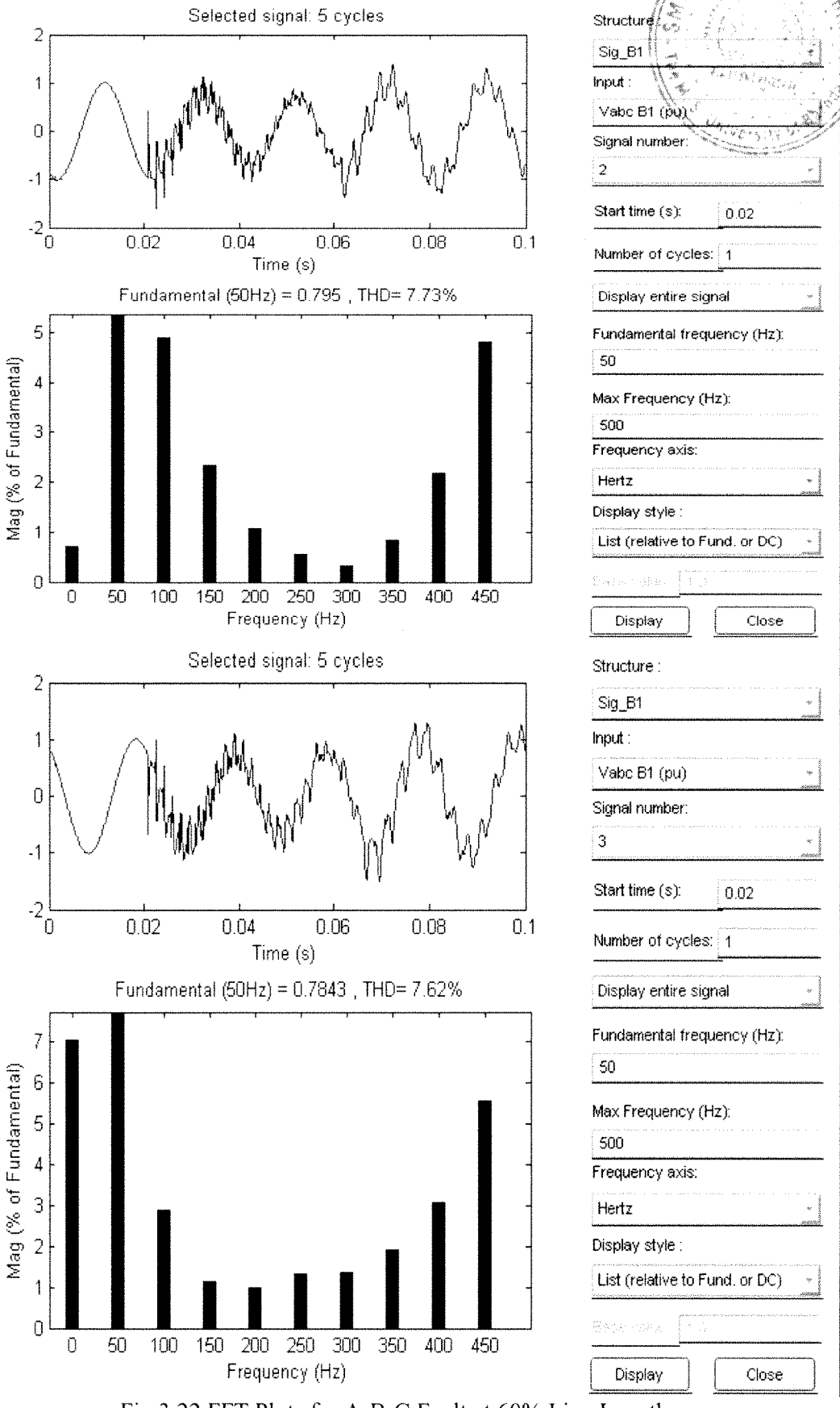


Fig.3.22 FFT Plots for A-B-C Fault at 60% Line Length

As the % THD is higher than set threshold in all the phases the proposed scheme concludes presence of the capacitor (which is true also) in the fault loop and takes further relaying decisions accordingly. Also observe that (Figure 3.21) MOV takes less than 20 ms of time(375 samples approximately) to reach its protection energy level after starts conducting and after that practically no capacitor is there in fault loop.

(9) Xc=50%, ZG1=100%, ZG2=100%, A-C-g Fault at 240 KM from Bus-B1,Rf=50 Ω

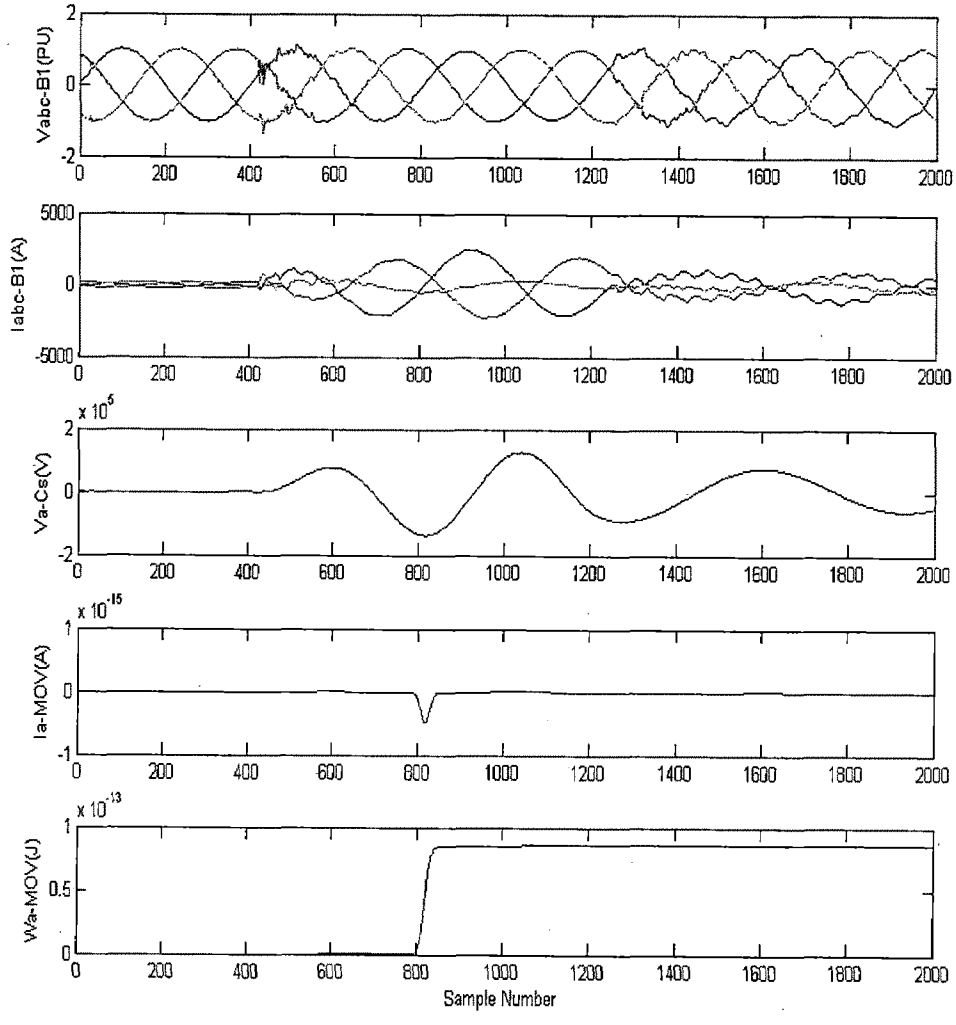


Fig.3.23 Plots for A-C-g Fault at 80% Line Length
(Vabc-B1: Three Phase Voltages Measured at bus B1,
Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,
Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.23) it's evident that the fault current in phase A and Phase C remains lower than I low-set and hence the scheme will not look for the % THD (Harmonic Index) in the post fault relay voltage and scheme does relay reach setting considering presence of full capacitor in line irrespective of its presence in fault loop and takes further relaying decisions accordingly.

(10) Xc=50%, ZG1=100%, ZG2=100%, A-B-C-g Fault at 240 KM from Bus-B1, Rf=0.01 Ω

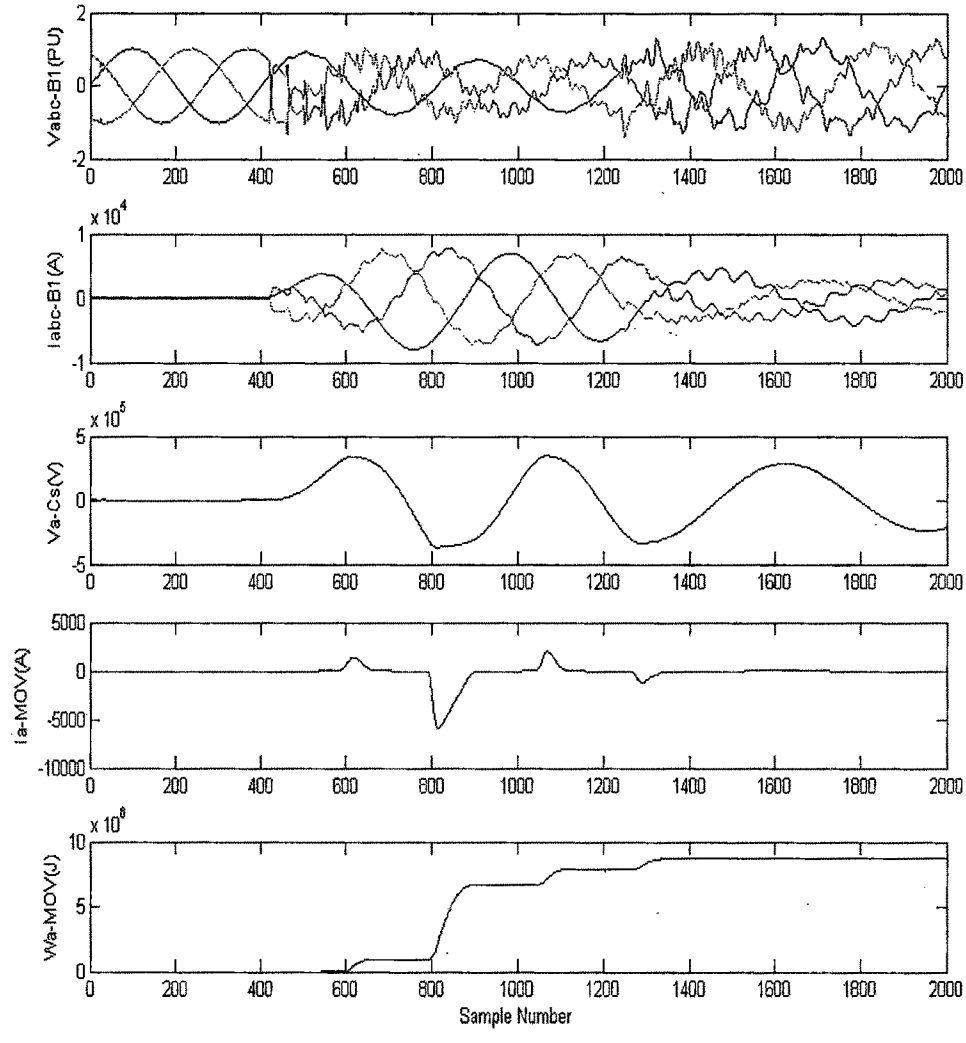
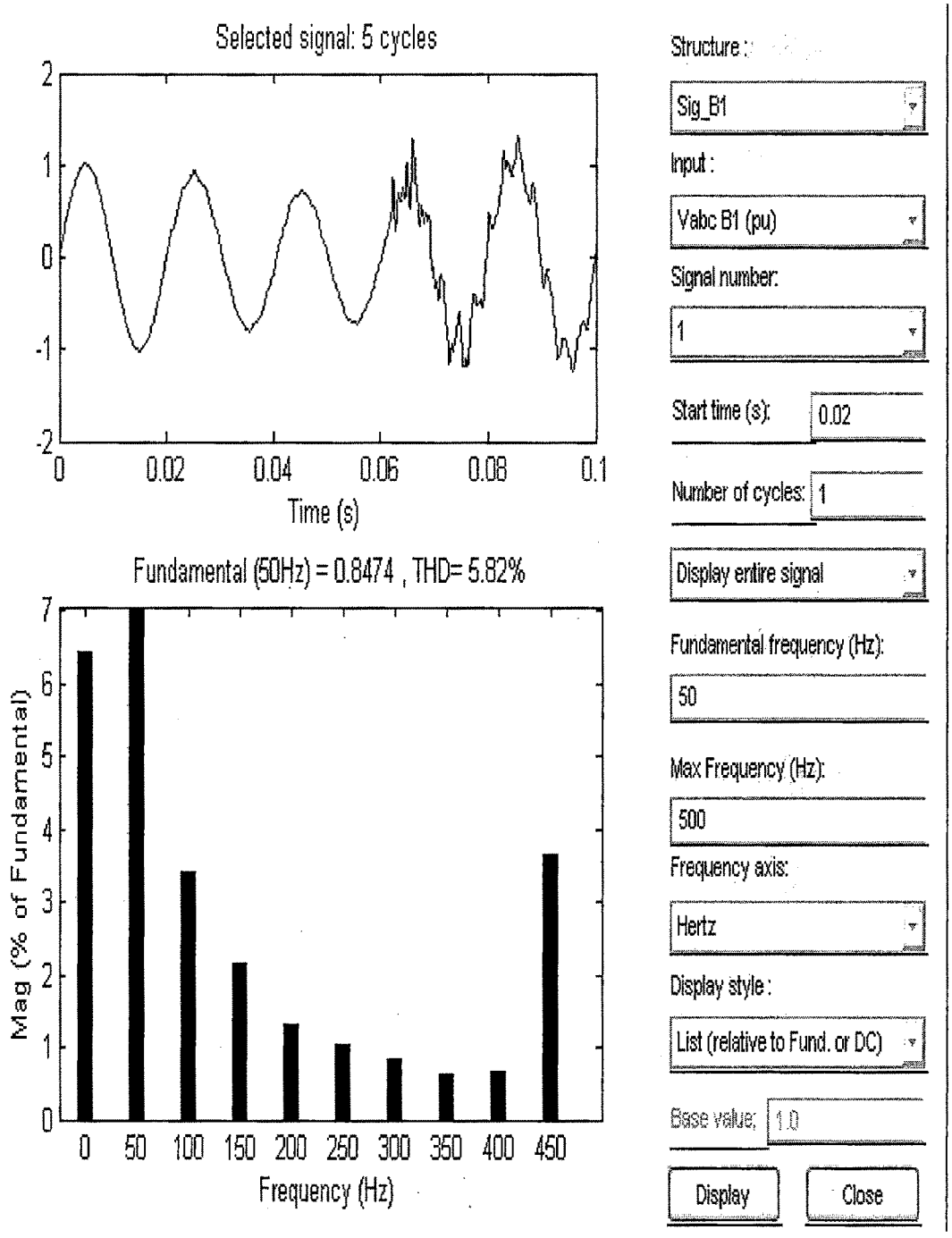


Fig.3.24 Plots for A-B-C-g Fault at 80% Line Length
(Vabc-B1: Three Phase Voltages Measured at bus B1,
Iabc-B1: Line Currents at bus-B1, V-Cs: Voltage across Series Capacitors,
Imov: Current Passing through MOV, Wmov: Energy across MOV)

From the plots (Figure 3.24) it's evident that the fault current in all the Phases exceeds I low-set and remains less than I high-set and hence the scheme will look for the % THD (Harmonic Index) in the post fault relay point voltage. The related FFT plot is shown in Figure 3.25.



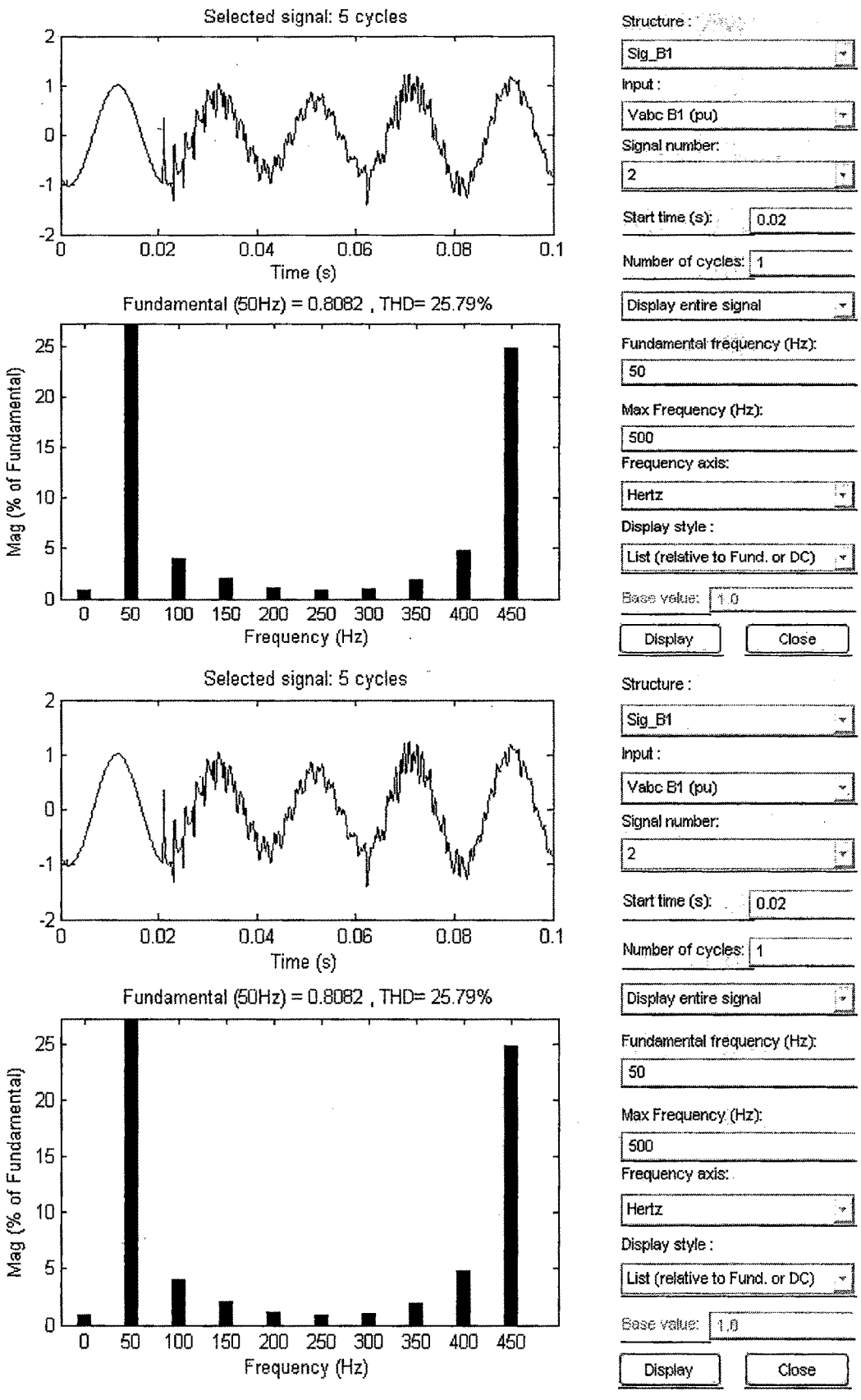


Fig.3.25 FFT Plots for A-B-C-g Fault at 80% Line Length

As the % THD is higher than set threshold in all the phases the proposed scheme concludes presence of the capacitor (which is true also) in the fault loop and takes further relaying decisions accordingly. (Also during conduction stage parallel combination of MOV and Series capacitor conducts almost equal amount of total fault current, practically keeping parallel combination of Cs-MOV in the fault loop measurements.)

3.6 Summary of Simulation Results

Table 3.4 depicts the performance of the proposed technique for different types of faults. It is observed from Table 3.4 that the proposed technique gives satisfactory results for all the type of faults (with and without ground). However, percentage incorrect relaying decisions taken in each type of fault is investigated and it was found that the faults near to Bus-B1 (at 20% of the line length and with the values of fault resistance 0.01, 1 Ω) resulting in sudden collapse in bus voltages at relaying point resulting in to higher %THD than set threshold and the scheme is mal-operating.

Table 3.4 Performance of Proposed Scheme for Different Types of Faults

Fault Type	No. of Test Cases	True Relaying Decision	Incorrect Relaying Decision	Accuracy (%)
L-g	8640	7791	849	89.699
L-L-g	8640	8018	622	92.326
L-L-L / L-L-L-g	2880	2521	359	87.500
L-L	8640	7994	646	91.585
Total	28800	26324	2476	91.402

Moreover, the performance of the proposed technique is analyzed with varying compensation level (25% to 75%). The results are shown in Table 3.5. It is observed from Table 3.5 that the proposed scheme is accurate for a compensation level of 50%. Moreover, it provides appreciable results in case of 25% and 75% compensation levels and hence, can be used for protection of series compensated lines.

Table 3.5 Performance of Proposed Scheme for Different Compensation Levels

Case No.	Xc (%)	No. of Test Cases	True Relaying Decision	Incorrect Relaying Decision	Accuracy (%)
1	50	9600	8860	740	92.291
2	25	9600	8887	713	92.572
3	75	9600	8577	1023	89.343
Total		28800	26324	2476	91.402

Table 3.6 Performance of Proposed Scheme with Different Parameters

Case No.	Xc %	ZG1 %	ZG2 %	No. of Test Cases	True Relaying Decision	Incorrect Relaying Decision	Accuracy (%)
1	50	100	100	1920	1801	119	93.802
2		75	100	1920	1707	213	88.906
3		125	100	1920	1810	110	94.270
4		100	75	1920	1728	192	90.000
5		100	125	1920	1814	106	94.479
6	25	100	100	1920	1808	112	94.166
7		75	100	1920	1710	210	89.062
8		125	100	1920	1817	103	94.635
9		100	75	1920	1733	187	90.260
10		100	125	1920	1819	101	94.739
11	75	100	100	1920	1751	169	91.197
12		75	100	1920	1643	277	85.572
13		125	100	1920	1760	160	91.666
14		100	75	1920	1660	260	86.458
15		100	125	1920	1763	157	91.822
Total				28800	26324	2476	91.402

Lastly, the performance of the proposed scheme is also analyzed for wide variations in the source impedance at both ends of the transmission line along with varying compensation level. Table 3.6 shows accuracy of the proposed scheme for different test cases for the said condition. From Table 3.6, it can be said that the proposed technique is quite effective in case of wide variations in the source impedance along with the change in compensation level.